FC9Y-B1268(1)

FC5A SERIES

MICROSmart pentra

User's Manual Basic Volume

IDEC CORPORATION

MICROSMART FC4A VS. FC5A

Comparison between FC4A and FC5A CPU Module Functions

CPU Module	FC4A	FC5A
Program Capacity	31,200 bytes maximum (5,200 steps)	62,400/127,800 bytes maximum (10,400/21,300 steps) (Note 1)
I/O Points	264 points maximum	512 points maximum
Advanced Instruction	72 maximum	152 maximum
32-bit Processing	—	Possible
Floating Point Data Processing	—	Possible
Trigonometric/Logarithm	—	Possible
Processing Time		
LOD Instruction	1 µs	0.056 µs minimum
MOV Instruction	66 µs	0.167 µs minimum
Basic Instruction	1.65 ms (1000 steps)	83 µs (1000 steps)
END Processing (Note 2)	0.64 ms	0.35 ms
Internal Relay	1,584 maximum	2,048 maximum
Shift Register	128 maximum	256 maximum
Data Register	7,600 maximum	48,000 maximum
Bit Addressing in Basic Instruction	—	Possible
Counter	100 maximum	256
Timer	100 maximum	256
Catch Input / Interrupt Input	Minimum turn on pulse width / Minimum turn off pulse width	
Four Inputs (I2 through I5)	40 µs / 150 µs	40 µs / 150 µs (I2 and I5) 5 µs / 5 µs (I3 and I4)
High-speed Counter		
Counting Frequency	20 kHz maximum	100 kHz maximum
Counting Range	0 to 65535 (16 bits)	0 to 4,294,967,295 (32 bits)
Multi-stage Comparison	—	Possible
Comparison Action	Comparison output	Comparison output Interrupt program
Frequency Measurement	—	Possible
Pulse Output		
Output Points	2 points maximum	3 points maximum
Output Pulse Frequency	20 kHz maximum	100 kHz maximum
Communication		
Baud Rate	19,200 bps maximum (Data link: 38,400 bps maximum)	115,200 bps maximum (Note 3)
Modbus Master/Slave Communication	—	Possible
Quantity of AS-Interface Modules	1 maximum	2 maximum
PID Advanced Auto Tuning	—	Possible
Edit / Test Program Download	—	Possible
Run-Time Program Download Size	600 bytes maximum	Without limit
System Program Download	—	Possible
Program Download from Memory Cartridge	Possible	Possible

Note 1: For FC5A-D12K1E and FC5A-D12S1E, it is possible to select whether to use a program capacity of 62,400 bytes or 127,800 bytes. If 127,800 bytes is selected, the run-time program download cannot be used.

Note 2: END processing does not include expansion I/O service, clock function processing, data link processing, and interrupt processing.

Note 3: To use 115200 bps, CPU modules with system program version 220 or higher and FC5A-SIF4 or FC5A-SIF2 (version 200 or higher) are required.

SAFETY PRECAUTIONS

- Read this user's manual to make sure of correct operation before starting installation, wiring, operation, maintenance, and inspection of the MicroSmart.
- All MicroSmart modules are manufactured under IDEC's rigorous quality control system, but users must add a backup or failsafe provision to the control system when using the MicroSmart in applications where heavy damage or personal injury may be caused in case the MicroSmart should fail.
- In this user's manual, safety precautions are categorized in order of importance to Warning and Caution:

⚠ Warning **Warning notices are used to emphasize that improper operation may cause severe personal injury or death.**

- Turn off power to the MicroSmart before installation, removal, wiring, maintenance, and inspection of the MicroSmart. Failure to turn power off may cause electrical shocks or fire hazard.
- Special expertise is required to install, wire, program, and operate the MicroSmart. People without such expertise must not use the MicroSmart.
- Emergency stop and interlocking circuits must be configured outside the MicroSmart. If such a circuit is configured inside the MicroSmart, failure of the MicroSmart may cause disorder of the control system, damage, or accidents.
- Install the MicroSmart according to the instructions described in this user's manual. Improper installation will result in falling, failure, or malfunction of the MicroSmart.

⚠ Caution **Caution notices are used where inattention might cause personal injury or damage to equipment.**

- The MicroSmart is designed for installation in a cabinet. Do not install the MicroSmart outside a cabinet.
- Install the MicroSmart in environments described in this user's manual. If the MicroSmart is used in places where the MicroSmart is subjected to high-temperature, high-humidity, condensation, corrosive gases, excessive vibrations, and excessive shocks, then electrical shocks, fire hazard, or malfunction will result.
- The environment for using the MicroSmart is "Pollution degree 2." Use the MicroSmart in environments of pollution degree 2 (according to IEC 60664-1).
- Prevent the MicroSmart from falling while moving or transporting the MicroSmart, otherwise damage or malfunction of the MicroSmart will result.
- Prevent metal fragments and pieces of wire from dropping inside the MicroSmart housing. Put a cover on the MicroSmart modules during installation and wiring. Ingress of such fragments and chips may cause fire hazard, damage, or malfunction.
- Use a power supply of the rated value. Use of a wrong power supply may cause fire hazard.
- Use an IEC 60127-approved fuse on the power line outside the MicroSmart. This is required when equipment containing the MicroSmart is destined for Europe.
- Use an IEC 60127-approved fuse on the output circuit. This is required when equipment containing the MicroSmart is destined for Europe.
- Use an EU-approved circuit breaker. This is required when equipment containing the MicroSmart is destined for Europe.
- Make sure of safety before starting and stopping the MicroSmart or when operating the MicroSmart to force outputs on or off. Incorrect operation on the MicroSmart may cause machine damage or accidents.
- If relays or transistors in the MicroSmart output modules should fail, outputs may remain on or off. For output signals which may cause heavy accidents, provide a monitor circuit outside the MicroSmart.
- Do not connect the ground wire directly to the MicroSmart. Connect a protective ground to the cabinet containing the MicroSmart using an M4 or larger screw. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not disassemble, repair, or modify the MicroSmart modules.
- Dispose of the battery in the MicroSmart modules when the battery is dead in accordance with pertaining regulations. When storing or disposing of the battery, use a proper container prepared for this purpose. This is required when equipment containing the MicroSmart is destined for Europe.
- When disposing of the MicroSmart, do so as an industrial waste.

Revision Record

The table below summarizes the changes to this manual since the first printing of FC9Y-B927-0 in April, 2006.

Upgraded and new functions listed below have been implemented in the FC5A MicroSmart CPU modules. The availability of these functions depends on the model and the system program version of the FC5A MicroSmart CPU modules.

To confirm the system program version of the MicroSmart CPU module, use WindLDR on a computer connected with the CPU module. The system program version is indicated on the PLC Status dialog box. See page 13-1.

To confirm the WindLDR version, select the WindLDR application button at the upper-left corner of the WindLDR screen, followed by **WindLDR Options** > **Resources**. The WindLDR version is found under **About WindLDR**.

Upgraded and New Functions List

CPU Module	All-In-One Type		Slim Type	WindLDR	Page
	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	**FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D**	**FC5A-D16RK1 FC5A-D16RS1 FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E** (Note 1)		
HMI Module Upgrade (Note 2)	110 or higher	110 or higher	101 or higher	—	5-60
FC5A-SIF2 Expansion RS232C Communication Module Compatibility (Note 3)	—		110 or higher	5.1 or higher	2-86, Advanced Vol. 25-1
Modbus Master Upgrade (Note 4)		—			12-6
Modbus Slave Upgrade (Note 4)	110 or higher	110 or higher			12-14
32-bit Data Storage Setting				5.2 or higher	5-46
Forced I/O	200 or higher	200 or higher	200 or higher		5-72
RUN LED Flashing Mode					5-49
Memory Cartridge Upload Function (Note 5)					2-93
Off-Delay Timer Instructions (TMLO, TIMO, TMHO, and TMSO)					7-11
Double-Word Counter Instructions (CNTD, CDPD, and CUDD)					7-15
MOV and IMOV Instructions Upgrade (New data type F)					Advanced Vol. 3-1
N Data Set and N Data Repeat Set Instructions (NSET and NRS)					Advanced Vol. 3-13, Advanced Vol. 3-14
Timer/Counter Current Value Store Instruction (TCCST)					Advanced Vol. 3-16
CMP Instructions Upgrade					Advanced Vol. 4-4
Load Comparison Instructions (LC=, LC<>, LC<, LC>, LC<=, and LC>=)					Advanced Vol. 4-8
BTOA and ATOB Instructions Upgrade (New data type D)					Advanced Vol. 8-9 Advanced Vol. 8-12
Data Divide, Combine, and Swap Instructions (DTDV, DTCB, and SWAP)					Advanced Vol. 8-21, Advanced Vol. 8-22, Advanced Vol. 8-23
User Communication Instructions Upgrade (TXD and RXD)					10-6, 10-15
File Data Processing Instructions (FIFOF, FIEX, and FOEX)					Advanced Vol. 19-1, Advanced Vol. 19-3

CPU Module	All-In-One Type		Slim Type	WindLDR	Page
	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	**FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D**	**FC5A-D16RK1 FC5A-D16RS1 FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E** (Note 1)		
Key Matrix Input (Note 6)	—	210 or higher	210 or higher	5.3 or higher	5-38
User Program Protection Upgrade	210 or higher				5-44
Exchange Instruction (XCHG)					Advanced Vol. 3-15
Increment Instruction (INC)					Advanced Vol. 5-13
Decrement Instruction (DEC)					Advanced Vol. 5-13
Sum Instruction (SUM)					Advanced Vol. 5-16
Random Instruction (RNDM)	210 or higher	210 or higher	210 or higher	5.3 or higher	Advanced Vol. 5-19
Decrement Jump Non-zero (DJNZ)					Advanced Vol. 11-5
N Data Search Instruction (NDSRC)					Advanced Vol. 19-5
Clock Instructions (TADD, TSUB, HTOS, STOH, and HOUR)					Advanced Vol. 20-1
All-in-one 12V DC Power CPU Modules	—	—	—		2-1
Analog I/O Modules Upgrade (Version 200 or higher)	—	Any	Any	Any	2-56
Modbus TCP Communication	210 or higher	210 or higher	210 or higher	5.3 or higher	Advanced Vol. 23-1
Modbus Slave Communication for Port 1 (Note 4)					12-11
Run/Stop Selection at Power Up	220 or higher	220 or higher	220 or higher	6.2 or higher	5-4
FC5A-SIF4 Expansion RS485 Communication Module Compatibility (Note 3)	—				2-86, Advanced Vol. 25-1
Data Link and Modbus Communication for Port 3 to Port 7 (Note 4)					11-1, 12-1
Communication Refresh Selection for Port 3 to Port 7					5-43
PID Upgrade (Integral Start Coefficient Support for Proportional Band)	—	246 or higher	246 or higher (FC5A-D16Rx1 or FC5A-D32x3) 131 or higher (FC5A-D12x1E)	7.2 or higher	Advanced Vol. 14-9

Note 1: All functions are available on FC5A-D12K1E and FC5A-D12S1E with system program version 100.

Note 2: Optional HMI module (FC4A-PH1) is needed to use this function.

Note 3: Expansion RS232C and RS485 communication modules (FC5A-SIF2 and FC5A-SIF4) cannot be used with the FC5A-C24R2D CPU module.

Note 4: Modbus Master communication can be used on port 2 through port 7. Modbus Slave communication can be used on port 1 through port 7. Optional communication adapter (FC4A-PC1 or FC4A-PC3) or communication module (FC4A-HPC1 or FC4A-HPC3) is needed to use port 2. Expansion RS232C or RS485 communication modules (FC5A-SIF2 or FC5A-SIF4) are needed to use port 3 through port 7.

Note 5: Memory cartridge (FC4A-PM32, FC4A-PM64, or FC4A-PM128) is required to use this function.

Note 6: Key matrix inputs cannot be used on the FC5A-C24R2D CPU module.

Revision History

Date	Manual No.	Description
March, 2011	B-1268(0)	First print
August, 2014	B-1268(1)	Updated the type number list for accessories

Slim Type CPU Module Instruction Execution Time

Execution times of some instructions have been reduced on slim type CPU modules with Logic Engine version 200 or higher and system program version 210 or higher as shown below.

Instruction	Conditions for Reduced Execution Time	Execution Time (µs)	
		New	Old
TML, TIM, TMH, TMS	T0 through T127 with preset values designated by constants	0.389	17
CC=, CC≥	Preset values designated by devices valid for Logic Engine	0.111	8
DC=, DC≥	Data register numbers and preset values designated by devices valid for Logic Engine	0.167	8
ADD (W, I)	Without repeat designation, and S1, S2, and D1 designated by devices valid for Logic Engine	0.278	44
SUB (W, I)			60

Note 1: Devices valid for Logic Engine are constants, data registers D0 through D1999, special data registers D8000 through D8399, timer/counter preset values, and timer/counter current values.

Note 2: The new instruction execution time applies to FC5A-D12K1E and FC5A-D12S1E regardless of its system program version.

- If the control system performance is affected by the reduced scan time, the scan time can be adjusted using the constant scan time (D8022, 1 to 1,000 ms). For details about constant scan time, see page 5-50. The DISP or DGRD instruction may not operate correctly due to the reduced scan time. If this is the case, adjust the scan time using the constant scan time (D8022, 1 to 1,000 ms), as required. For minimum scan times required for the DISP and DGRD instructions, see pages 10-1 and 10-3 (Advanced Vol.).
- Logic Engine version is found in the lower right corner of the label on the side of the slim type CPU module. To confirm the system program version of the MicroSmart CPU module, use WindLDR on a computer connected with the CPU module. The system program version is indicated on the PLC Status dialog box. See page 13-1.

About This Manual

This user's manual primarily describes entire functions, installation, and programming of the MicroSmart CPU, I/O, and all other modules. Also included are powerful communications of the MicroSmart and troubleshooting procedures.

Chapter 1: General Information

General information about the MicroSmart, features, brief description on special functions, and various system setup configurations for communication.

Chapter 2: Module Specifications

Specifications of CPU, input, output, mixed I/O, analog I/O, and other optional modules.

Chapter 3: Installation and Wiring

Methods and precautions for installing and wiring the MicroSmart modules.

Chapter 4: Operation Basics

General information about setting up the basic MicroSmart system for programming, starting and stopping MicroSmart operation, and simple operating procedures from creating a user program using WindLDR on a PC to monitoring the MicroSmart operation.

Chapter 5: Special Functions

Stop/reset inputs, run/stop selection at memory backup error, keep designation for internal relays, shift registers, counters, and data registers. Also included are high-speed counter, frequency measurement, catch input, interrupt input, timer interrupt, input filter, user program protection, constant scan time, online edit, and many more special functions.

Chapter 6: Device Addresses

Device addresses available for the MicroSmart CPU modules to program basic and advanced instructions. Special internal relays and special data registers are also described.

Chapter 7: Basic Instructions

Programming of the basic instructions, available devices, and sample programs.

Chapter 8: Advanced Instructions Reference

General rules of using advanced instructions, terms, data types, and formats used for advanced instructions.

Chapter 9 through Chapter 12:

Analog I/O control and various communication functions such as user, data link, and Modbus communication.

Chapter 13: Troubleshooting

Procedures to determine the cause of trouble and actions to be taken when any trouble occurs while operating the MicroSmart.

Appendix

Additional information about execution times for instructions, I/O delay time, and MicroSmart type list.

Index

Alphabetical listing of key words.

IMPORTANT INFORMATION

Under no circumstances shall IDEC Corporation be held liable or responsible for indirect or consequential damages resulting from the use of or the application of IDEC PLC components, individually or in combination with other equipment.

All persons using these components must be willing to accept responsibility for choosing the correct component to suit their application and for choosing an application appropriate for the component, individually or in combination with other equipment.

All diagrams and examples in this manual are for illustrative purposes only. In no way does including these diagrams and examples in this manual constitute a guarantee as to their suitability for any specific application. To test and approve all programs, prior to installation, is the responsibility of the end user.

RELATED MANUALS

The following manuals related to the FC5A series MicroSmart are available. Refer to them in conjunction with this manual.

Type No.	Manual Name	Description
FC9Y-B1268	FC5A Series MicroSmart Pentra User's Manual Basic Volume (this manual)	Describes module specifications, installation instructions, wiring instructions, basic operation, special function, device addresses, instruction list, basic instructions, analog modules, user communication, data link communication, Modbus ASCII/RTU communication, and troubleshooting.
FC9Y-B1273	FC5A Series MicroSmart Pentra User's Manual Advanced Volume	Describes instruction list, move instructions, data comparison instructions, binary arithmetic instructions, boolean computation instructions, shift/rotate instructions, data conversion instructions, week programmer instructions, interface instructions, program branching instructions, refresh instructions, interrupt control instructions, coordinate conversion instructions, average instructions, pulse output instructions, PID instructions, dual/teaching timer instructions, intelligent module access instructions, trigonometric function instructions, logarithm/power instructions, file data processing instructions, clock instructions, computer link communication, modem communication, Modbus TCP communication, expansion RS232C/RS485 communication modules, and AS-Interface master modules.
FC9Y-B1278	FC5A Series MicroSmart Pentra User's Manual Web Server CPU Module Volume	Describes FC5A Slim Type Web Server CPU Module specifications and functions.
FC9Y-B1283	FC5A Series PID Module User's Manual	Describes PID Module specifications and functions.

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CHAPTER 5: Special Functions

CHAPTER 6: Device Addresses

CHAPTER 7: Basic Instructions

1: GENERAL INFORMATION

Introduction

This chapter describes general information about the powerful capabilities of the upgraded FC5A series MicroSmart micro programmable logic controllers and system setups to use the MicroSmart in various ways of communication.

About the MicroSmart

IDEC's FC5A MicroSmart is an upgraded family of micro programmable logic controllers available in two styles of CPU modules; all-in-one and slim types.

The all-in-one type CPU module has 10, 16, or 24 I/O terminals and is equipped with a built-in universal power supply to operate on 100 to 240V AC, or 24 or 12V DC. Using four optional 16-point I/O modules, the 24-I/O type CPU module (except 12V DC power type) can expand the I/O points up to a total of 88 points. Program capacity of the all-in-one type CPU modules is 13,800 bytes (2,300 steps) on the 10-I/O type CPU module, 27,000 bytes (4,500 steps) on the 16-I/O type, and 54,000 bytes (9,000 steps) on the 24-I/O type.

The slim type CPU module has 16 or 32 I/O terminals and operates on 24V DC. The total I/O points can be expanded to a maximum of 512. When using two AS-Interface master modules, a maximum of 1,380 I/O points can be connected. The program capacity of slim type CPU modules is 62,400 bytes (10,400 steps).

Slim type CPU modules feature Logic Engine for superior ladder processing capabilities to achieve fast execution of instructions — 0.056 µs for a basic instruction (LOD) and 0.167 µs for an advanced instruction (MOV).

User programs for the MicroSmart can be edited using WindLDR on a Windows PC. Since WindLDR can load existing user programs made for IDEC's previous PLCs such as OpenNet Controller and FC4A MicroSmart, your software assets can be used in the new control system.

Features

Powerful Communication Functions

The MicroSmart features five powerful communication functions.

Maintenance Communication (Computer Link)	When a MicroSmart CPU module is connected to a computer, operating status and I/O status can be monitored on the computer, data in the CPU can be monitored or updated, and user programs can be downloaded and uploaded. All CPU modules can set up a 1:N computer link system to connect a maximum of 32 CPU modules to a computer.
User Communication	All MicroSmart CPU modules can be linked to external RS232C devices such as computers, printers, and barcode readers on port 1 to port 7, using the user communication function. RS485 user communication is also available on port 2 to port 7. Expansion communication modules (FC5A-SIF2/-SIF4) can be used with all-in-one 24-I/O (except 12V DC power type) and slim type CPU modules to expand up to five or seven communication ports, respectively.
Modem Communication	All MicroSmart CPU modules can communicate through modems using the built-in modem protocol. Modem communication is available through port 2.
Data Link	All MicroSmart CPU modules can be used as data link master or slave station. One CPU module at the master station can communicate with 31 slave stations through an RS485 line to exchange data and perform distributed control effectively.
Modbus Communication	All MicroSmart CPU modules can be used as Modbus master or slave, and can be connected to other Modbus devices. Modbus Master communication is available on port 2 to port 7. Modbus Slave communication is available on port 1 to port 7.

Communication Adapter (All-in-one type CPU modules)
Communication Module (Slim type CPU modules)

In addition to the standard RS232C port 1, all-in-one type CPU modules feature a port 2 connector to install an optional RS232C or RS485 communication adapter. Any slim type CPU module can be used with an optional RS232C or RS485 communication module to add communication port 2. With an optional HMI base module mounted with a slim type CPU module, an optional RS232C or RS485 communication adapter can also be installed on the HMI base module.

RS232C Communication Adapter **RS232C Communication Module**	Used for computer link 1:1 communication, user communication, and modem communication.
RS485 Communication Adapter **RS485 Communication Module**	Available in mini DIN connector and terminal block styles. Used for computer link 1:1 or 1:N communication, user communication, data link communication, and Modbus communication.

Expansion RS232C/RS485 Communication Module (slim CPU modules and all-in-one 24-I/O types except 12V DC type)

All-in-one 24-I/O type CPU modules (except 12V DC power type) can be used with a maximum of three expansion RS232C/RS485 communication modules (FC5A-SIF2/-SIF4) to expand up to five communication ports. Slim type CPU modules can be used with a maximum of five expansion RS232C/RS485 communication modules to expand up to seven communication ports. Expansion RS232C/RS485 communication modules can be used for computer link communication, user communication, data link, and Modbus communication.

HMI Module (all CPU modules)

An optional HMI module can be installed on any all-in-one type CPU module, and also on the HMI base module mounted next to any slim type CPU module. The HMI module makes it possible to manipulate the RAM data in the CPU module without using the Online menu options in WindLDR.

HMI module functions include:

- Displaying timer/counter current values and changing timer/counter preset values
- Displaying and changing data register values
- Setting and resetting bit device statuses, such as inputs, outputs, internal relays, and shift register bits
- Displaying and clearing error data
- Starting and stopping the PLC
- Displaying and changing calendar/clock data (only when using the clock cartridge)
- Confirming changed timer/counter preset values

Clock Cartridge (all CPU modules)

An optional clock cartridge can be installed on the CPU module to store real time calendar/clock data for use with advanced instructions to perform time-scheduled control.

Memory Cartridge (all CPU modules)

A user program can be stored on an optional memory cartridge using WindLDR. The memory cartridge can be installed on another CPU module to replace user programs without the need for connecting to a computer. The original user program in the CPU module is restored after removing the memory cartridge.

The user program can be downloaded to the CPU module. Memory cartridge upload is also available on upgraded CPU modules with system program version 200 or higher. The upload and download options are selected using WindLDR.

Analog I/O Modules (slim CPU modules and all-in-one 24-I/O types except 12V DC power type)

The analog input channel can accept either voltage (0 to 10V DC) and current (4 to 20 mA) signals or thermocouple (types K, J, and T) and resistance thermometer (Pt100, Pt1000, Ni100, and Ni1000) signals. The output channel generates voltage (0 to 10V DC or –10 to +10V DC) and current (4 to 20 mA) signals.

AS-Interface Master Module (slim CPU modules and all-in-one 24-I/O types except 12V DC power type)

One or two AS-Interface master modules can be mounted to communicate with a maximum of 124 slaves, or 496 inputs and 372 outputs, such as actuators and sensors, through the AS-Interface bus.

Web Server Module (all CPU modules)

The web server module is used to connect the MicroSmart to Ethernet. Remote monitoring is made possible, sending E-mail messages to personal computers or mobile phones.

Special Functions

The MicroSmart features various special functions packed in the small housing as described below. For details about these functions, see the following chapters.

Stop and Reset Inputs

Any input terminal on the CPU module can be designated as a stop or reset input to control the MicroSmart operation.

RUN/STOP Selection at Startup when "Keep" Data is Broken

When data to be kept such as "keep" designated counter values are broken while the CPU is powered down, the user can select whether the CPU starts to run or not to prevent undesirable operation at the next startup.

"Keep" or "Clear" Designation of CPU Data

Internal relays, shift register bits, counter current values, and data register values can be designated to be kept or cleared when the CPU is powered down. All or a specified range of these devices can be designated as keep or clear types.

High-speed Counter

The MicroSmart has four built-in high-speed counters to count high-speed pulses which cannot be counted by the normal user program processing. All-in-one type CPU modules can count up to 65,535 pulses at 50 kHz. Slim type CPU modules can count up to 4,294,967,295 pulses at 100 kHz. Both CPU modules can use either single-phase or two-phase high-speed counters. The high-speed counters can be used for simple positioning control and simple motor control.

Frequency Measurement

The pulse frequency of input signals to four input terminals can be counted using the high-speed counter function at a maximum of 50 kHz (all-in-one type CPU modules) or 100 kHz (slim type CPU modules).

Catch Input

Four inputs can be used as catch inputs. The catch input makes sure to receive short input pulses from sensors without regard to the scan time — rising and falling pulse widths of 40 µs and 150 µs (all-in-one type CPU modules) or 5 µs and 5 µs (slim type CPU modules).

Interrupt Input

Four inputs can be used as interrupt inputs. When a quick response to an external input is required, such as positioning control, the interrupt input can call a subroutine to execute an interrupt program.

Timer Interrupt

In addition to the interrupt input, all CPU modules have a timer interrupt function. When a repetitive operation is required, the timer interrupt can be used to call a subroutine repeatedly at predetermined intervals of 10 through 140 ms.

Input Filter

The input filter can be adjusted for eight inputs to reject input noises. Selectable input filter values to pass input signals are 0 ms, and 3 through 15 ms in 1-ms increments. The input filter rejects inputs shorter than the selected input filter value minus 2 ms. This function is useful for eliminating input noises and chatter in limit switches.

User Program Read/Write Protection

The user program in the CPU module can be protected against reading and/or writing by including a password in the user program. This function is effective for security of user programs. Upgraded CPU modules with system program version 210 or higher have an option for read protection without a password, making it possible to inhibit reading completely.

Constant Scan Time

The scan time may vary whether basic and advanced instructions are executed or not depending on input conditions to these instructions. When performing repetitive control, the scan time can be made constant by entering a required scan time value into a special data register reserved for constant scan time.

Online Edit, Run-Time Program Download, and Test Program Download

Normally, the CPU module has to be stopped before downloading a user program. All CPU modules have online edit, run-time program download, and test program download capabilities to download a user program containing small changes while the CPU is running in either 1:1 or 1:N computer link system. This function is particularly useful to make small modifications to the user program and confirm the changes while the CPU is running.

Analog Potentiometer

All CPU modules have an analog potentiometer, except the all-in-one 24-I/O type CPU module has two analog potentiometers. The values (0 through 255) set with analog potentiometers 1 and 2 are stored to special data registers. The analog potentiometer can be used to change the preset value for a timer or counter.

Analog Voltage Input

Every slim type CPU module has an analog voltage input connector. When an analog voltage of 0 through 10V DC is applied to the analog voltage input connector, the signal is converted to a digital value of 0 through 255 and stored to a special data register. The data is updated in every scan.

Pulse Output

Slim type CPU modules have pulse output instructions to generate high-speed pulse outputs from transistor output terminals used for simple position control applications, illumination control, trapezoidal control, and zero-return control.

PID Control

All CPU modules (except the all-in-one 10- and 16-I/O types) have the PID instruction, which implements a PID (proportional, integral, and derivative) algorithm with built-in auto tuning or advanced auto tuning to determine PID parameters. This instruction is primarily designed for use with an analog I/O module to read analog input data, and turns on and off a designated output to perform PID control in applications such as temperature control. In addition, the PID instruction can also generate an analog output using an analog I/O module.

Expansion Data Register

Slim type CPU modules have expansion data registers D2000 through D7999. Numerical data can be set to expansion data registers using WindLDR. When downloading the user program, the preset values of the expansion data registers are also downloaded to the ROM in the CPU module. Since the data in the ROM is non-volatile, the preset values of the expansion data registers are maintained semi-permanently and loaded to the RAM each time the CPU is powered up.

32-bit and Floating Point Data Types

Some advanced instructions can select 32-bit data types from D (double word), L (long), and F (float) in addition to W (word) and I (integer).

System Setup

This section illustrates system setup configurations for using powerful communication functions of the MicroSmart.

User Communication and Modem Communication System

The all-in-one type MicroSmart CPU modules have port 1 for RS232C communication and port 2 connector. An optional RS232C or RS485 communication adapter can be installed on the port 2 connector. With an RS232C communication adapter installed on port 2, the MicroSmart CPU module can communicate with two RS232C devices at the same time.

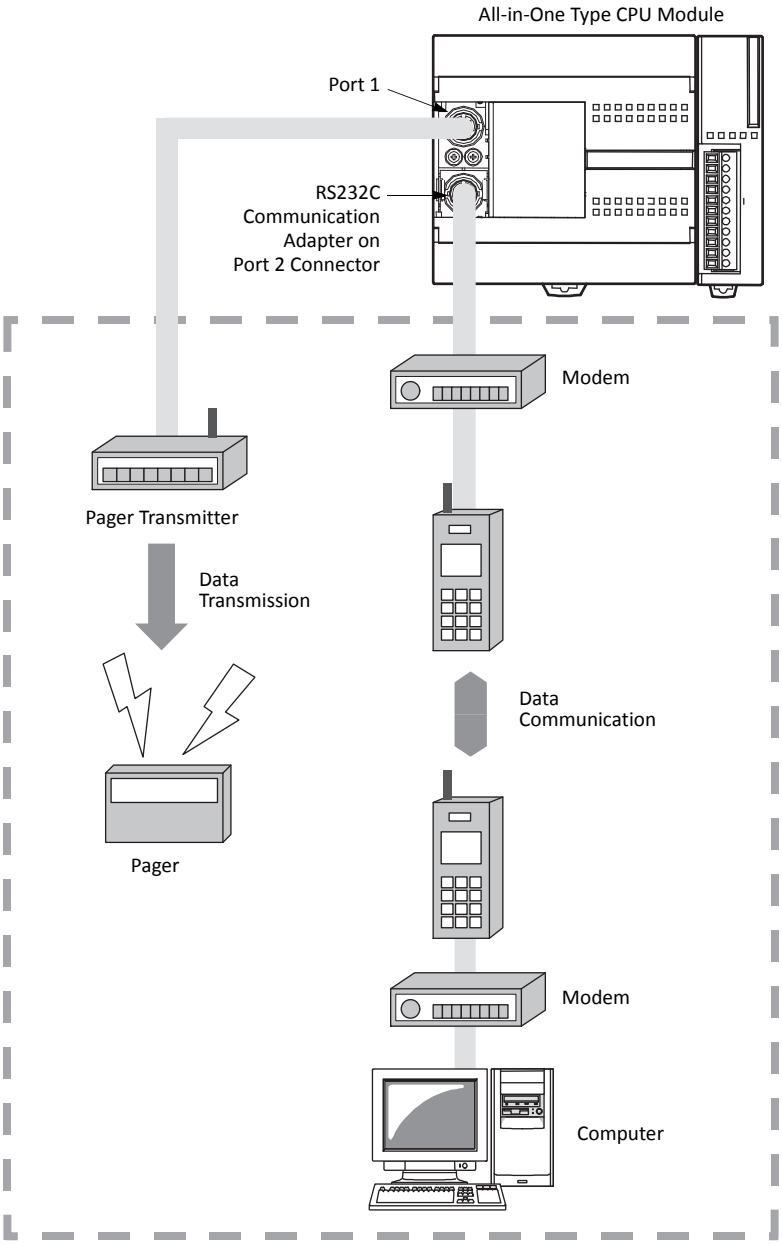
Expansion RS232C/RS485 communication modules (FC5A-SIF2/-SIF4) can also be mounted to the CPU modules to add port 3 to port 5, so that MicroSmart CPU module can communicate with more RS232C/RS485 devices at the same time.

The figure below illustrates a system setup of user communication and modem communication. In this example, the operating status of a remote machine is monitored on a computer through modems connected to port 2 and the data is transferred through port 1 to a pager transmitter using the user communication.

The same system can be set up using any slim type CPU module and an optional RS232C communication module.

For details about the user communication, see page 10-1.

For details about the modem mode, see page 21-1 (Advanced Vol.).

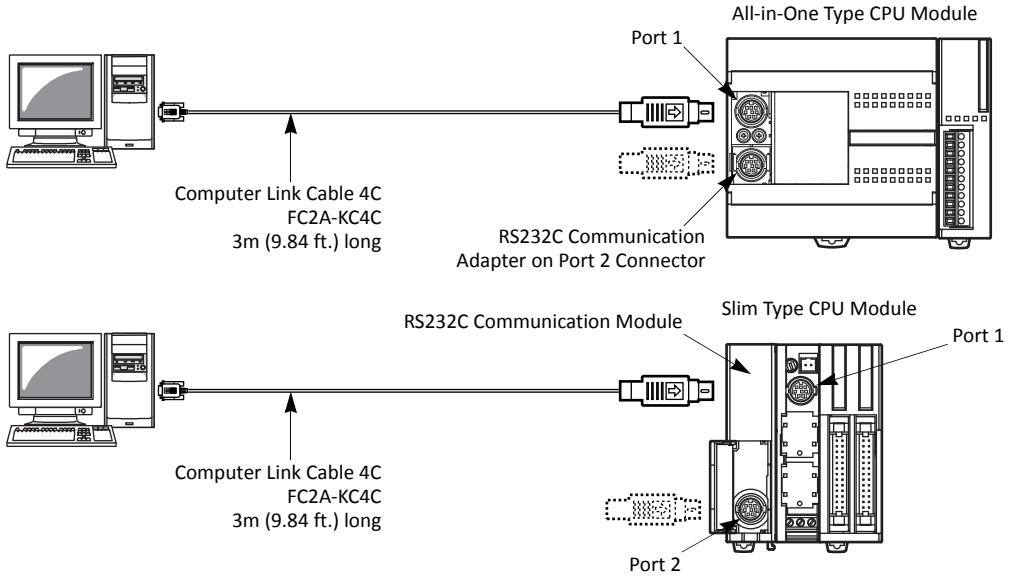


Computer Link System

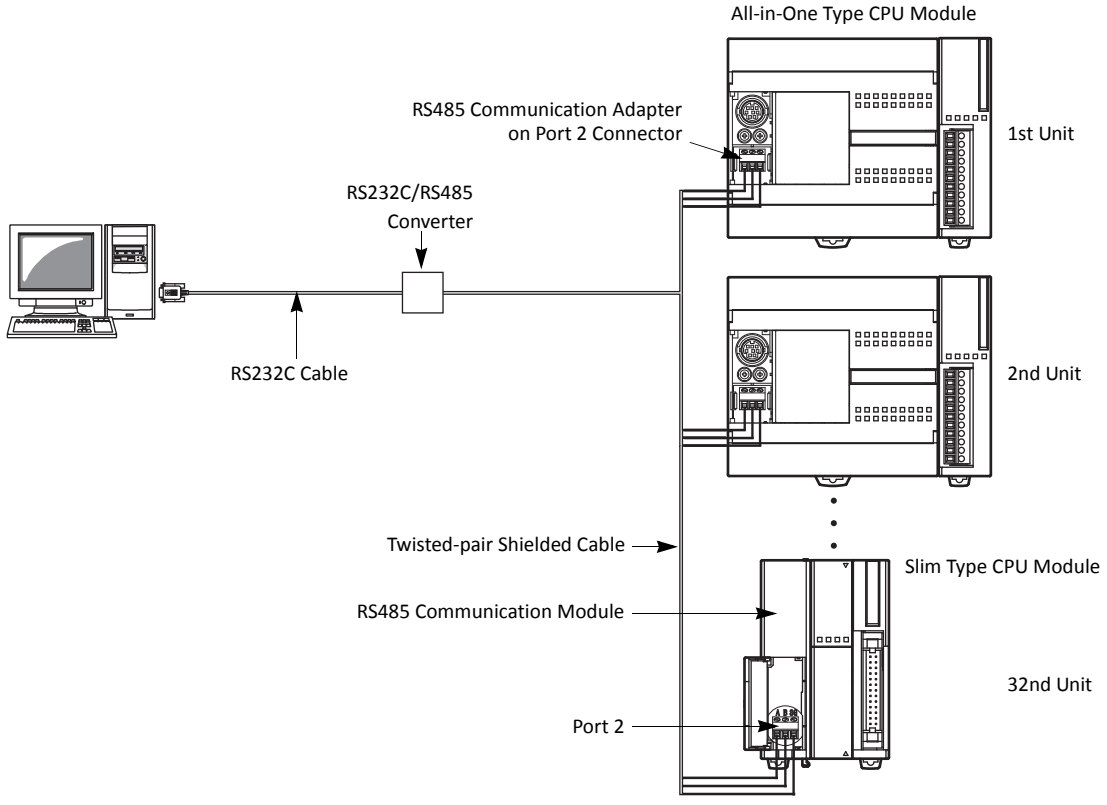
When the MicroSmart is connected to a computer, operating status and I/O status can be monitored on the computer, data in the CPU module can be monitored or updated, and user programs can be downloaded and uploaded. When an optional RS485 communication adapter is installed on the port 2 connector of the all-in-one type CPU modules or when an optional RS485 communication module is mounted with any slim type CPU modules, a maximum of 32 CPU modules can be connected to one computer in the 1:N computer link system. FC5A-SIF4 expansion RS485 communication modules can also be mounted to the CPU modules to add port 3 through port 7, so that the CPU modules can be added in the 1:N computer link system.

For details about the computer link communication, see pages 4-1 (this manual) and 21-1 (Advanced Vol.).

Computer Link 1:1 Communication



Computer Link 1:N Communication

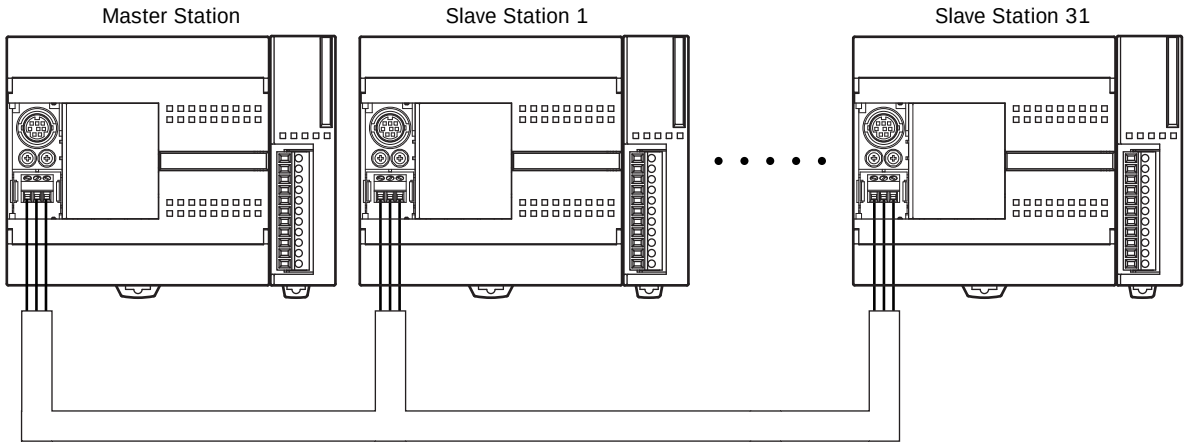


Data Link System

With an optional RS485 communication adapter installed on the port 2 connector or an FC5A-SIF4 expansion RS485 communication module mounted, one CPU module at the master station can communicate with 31 slave stations through the RS485 line to exchange data and perform distributed control effectively. The RS485 terminals are connected with each other using a 2-core twisted pair cable.

The same data link system can also be set up using any slim type CPU modules mounted with RS485 communication modules.

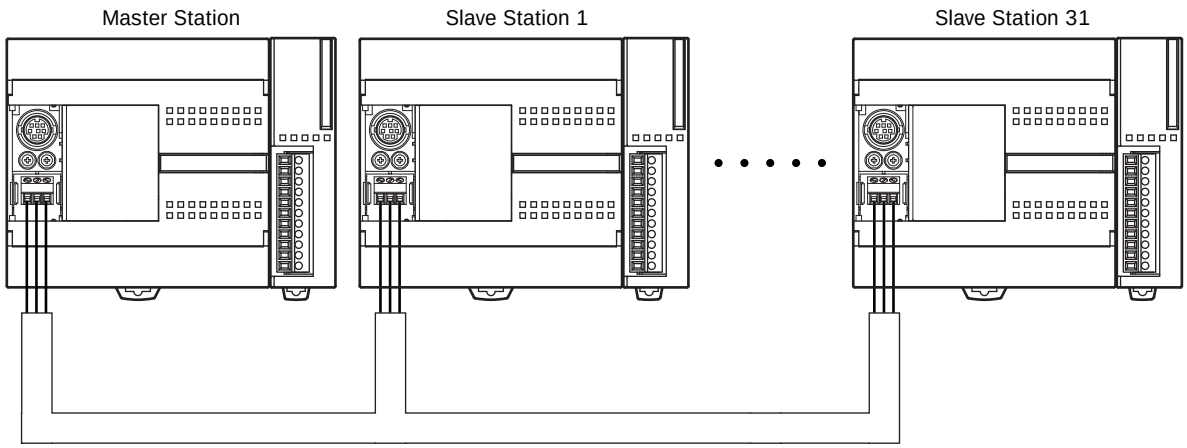
For details about the data link communication, see page 11-1.



Modbus Communication System

With an optional RS232C/RS485 communication adapter installed on the port 2 connector or an FC5A-SIF4 expansion RS485 communication module mounted, any FC5A MicroSmart CPU module can be used as a Modbus master or slave station. Using the Modbus communication, the MicroSmart CPU module can exchange data with other Modbus devices.

For details about the Modbus communication, see page 12-1.

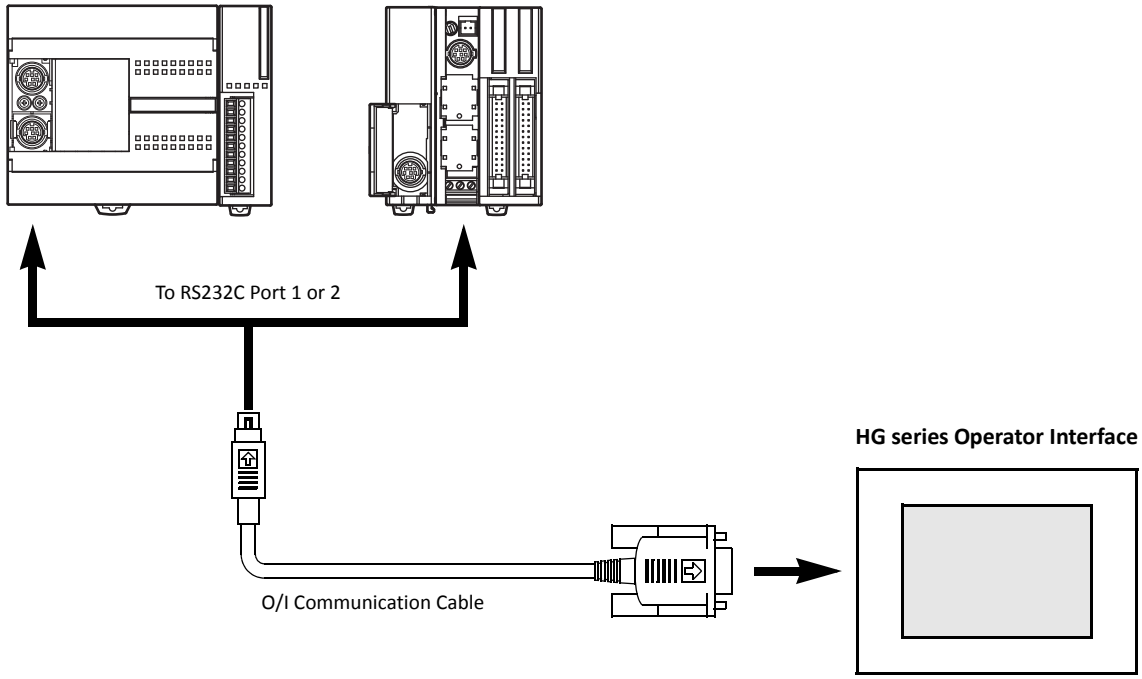


Operator Interface Communication System

The MicroSmart can communicate with IDEC's HG series operator interfaces through RS232C or RS485 port. When using the expansion RS232C/RS485 communication modules (FC5A-SIF2/-SIF4), the all-in-one 24-I/O CPU module, except the 12V DC type, can expand up to port 5 and the slim type CPU module can expand up to port 7. For the expansion RS232C/RS485 communication, see page 25-1 (Advanced Vol.).

Optional cables are available for connection between the MicroSmart and HG series operator interfaces. When installing an optional RS232C communication adapter on the all-in-one type CPU module or an optional RS232C communication module on the slim type CPU module, two operator interfaces can be connected to one MicroSmart CPU module.

For details about communication settings, see the user's manual for the operator interface.



Applicable Cables to Operator Interfaces

Operator Interface	O/I Communication Cable	For Use on MicroSmart	
		All-in-one 24-I/O CPU Module (except 12V DC type)	Slim CPU Module
HG1B, HG2A Series	FC4A-KC1C	Port 1 to port 5 (RS232C)	Port 1 to port 7 (RS232C)
	HG9Z-XC183 (Note)	Port 2 (RS232C)	Port 2 (RS232C)
	Shielded twisted-pair cable	Port 2 to port 5 (RS485)	Port 2 to port 7 (RS485)
HG2F, HG3F, HG4F Series	FC4A-KC2C	Port 1 to port 5 (RS232C)	Port 1 to port 7 (RS232C)
	HG9Z-3C125 (Note)	Port 2 (RS232C)	Port 2 (RS232C)
	Shielded twisted-pair cable	Port 2 to port 5 (RS485)	Port 2 to port 7 (RS485)
HG1F	FC4A-KC1C	Port 1 to port 5 (RS232C)	Port 1 to port 7 (RS232C)
	Shielded twisted-pair cable	Port 2 to port 5 (RS485)	Port 2 to port 7 (RS485)
HG2G	FC4A-KP1C	Port 1 to port 2 (RS232C)	Port 1 to port 2 (RS232C)
	Shielded twisted-pair cable	Port 3 to port 5 (RS232C) Port 2 to port 5 (RS485)	Port 3 to port 7 (RS232C) Port 2 to port 7 (RS485)

Note: HG series communication cables HG9Z-XC183 and HG9Z-3C125 can be used on port 2 only.

AS-Interface Network

Actuator-Sensor-Interface, abbreviated AS-Interface

The MicroSmart can be connected to the AS-Interface network using the AS-Interface master module (FC4A-AS62M).

AS-Interface is a type of field bus that is primarily intended to be used to control sensors and actuators. AS-Interface is a network system that is compatible with the IEC62026 standard and is not proprietary to any one manufacturer. A master device can communicate with slave devices such as sensors, actuators, and remote I/Os, using digital and analog signals transmitted over the AS-Interface bus.

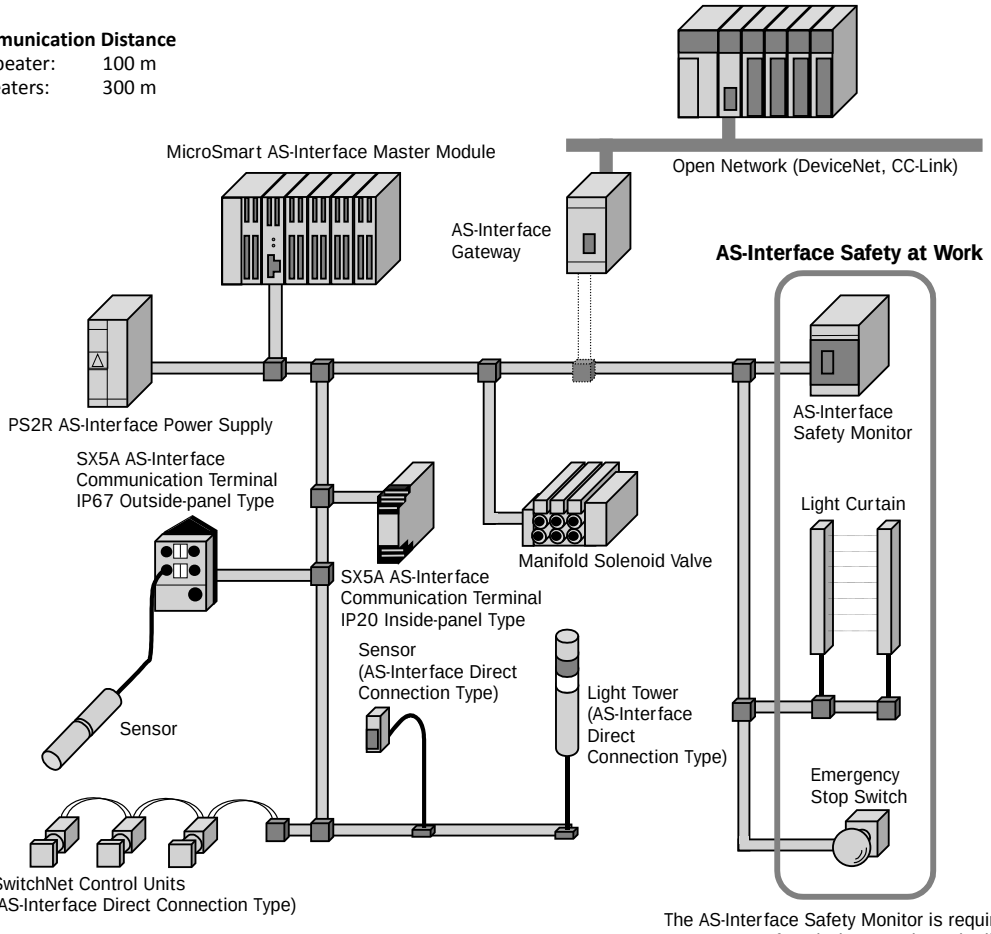
The AS-Interface system is comprised of the following three major components:

- One master, such as the MicroSmart AS-Interface master module
- One or more slave devices, such as sensors, actuators, switches, and indicators
- Dedicated 30V DC AS-Interface power supply (26.5 to 31.6V DC)

These components are connected using a two-core cable for both data transmission and AS-Interface power supply. AS-Interface employs a simple yet efficient wiring system and features automatic slave address assignment function, while installation and maintenance are also very easy.

For details about AS-Interface communication, see pages 2-78 and 24-1 (Advanced Vol.).

Maximum Communication Distance
Without repeater: 100 m
With 2 repeaters: 300 m



SwitchNet™ SwitchNet is an IDEC trademark for pushbuttons, pilot lights, and other control units capable of direct connection to the AS-Interface. SwitchNet devices are completely compatible with AS-Interface Ver. 2.1.

Expansion RS232C/RS485 Communication Module

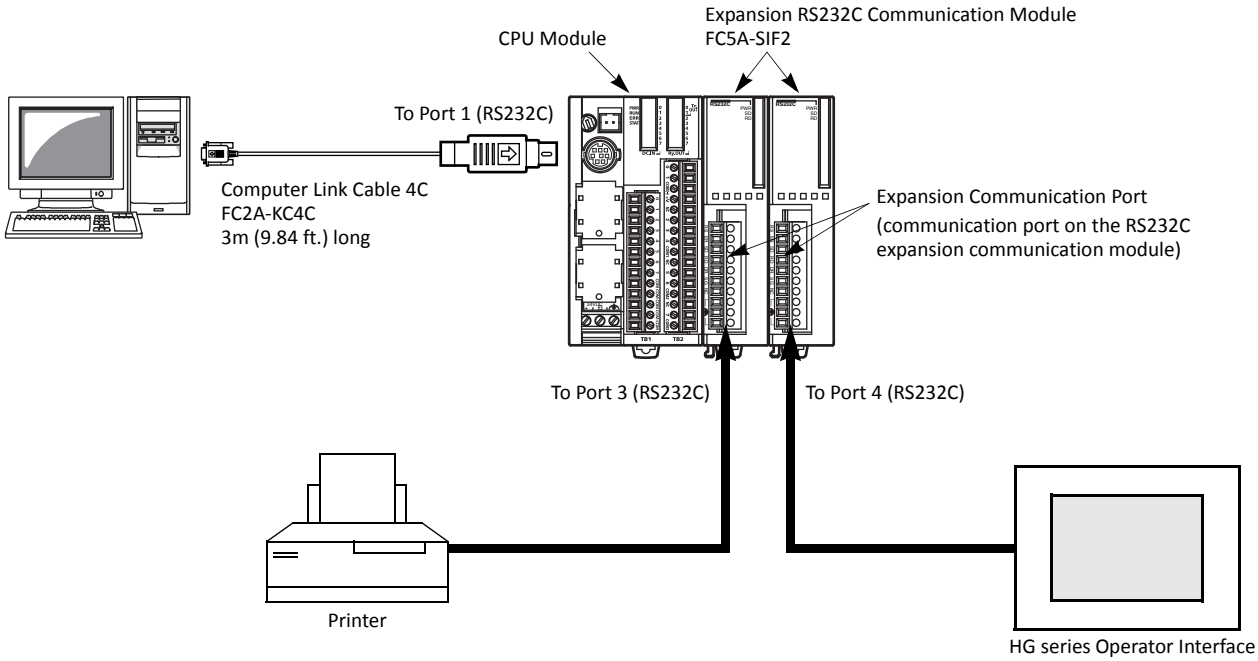
The FC5A-SIF2 expansion RS232C communication module and the FC5A-SIF4 expansion RS485 communication module are expansion modules used for the FC5A series micro programmable controller.

The expansion RS232C/RS485 communication module is mounted on the right of all-in-one 24-I/O type (except 12V DC power type) or slim type CPU modules. All-in-one 24-I/O type CPU modules can be used with a maximum of three expansion RS232C/RS485 communication modules to expand up to five communication ports. Slim type CPU modules can be used with a maximum of five expansion RS232C/RS485 communication modules to expand up to seven communication ports.

For example, the expansion RS232C communication module can be used in the following system. When the CPU module is connected to a PC and also mounted with expansion RS232C communication modules, the PC can be used to monitor the CPU operation while the CPU module communicates with multiple RS232C devices, such as printers, operator interfaces, and measuring instruments.

For details about these communication functions, see page 25-1 (Advanced Vol.).

System Setup Example



Features

The expansion communication module has four communication functions.

Maintenance Communication (Computer Link)	When a MicroSmart CPU module is connected to a computer, operating status and I/O status can be monitored on the computer, data in the CPU can be monitored or updated, and user programs can be downloaded and uploaded. Run-time program download cannot be used.
User Communication	CPU modules can be linked to remote RS232C or RS485 devices such as computers, printers, and barcode readers through expansion communication modules, using the user communication function.
Data Link (Note)	All MicroSmart CPU modules can set up a data link system. One CPU module at the master station can communicate with 31 slave stations through an RS485 line to exchange data and perform distributed control effectively.
Modbus Communication (Note)	All MicroSmart CPU modules can be used as a Modbus master or slave, and can be connected to other Modbus devices.

Note: CPU modules with system program version 220 or higher and FC5A-SIF4 are needed to use data link or Modbus communication. For the combination of the version numbers and supported protocols, see page A-17.

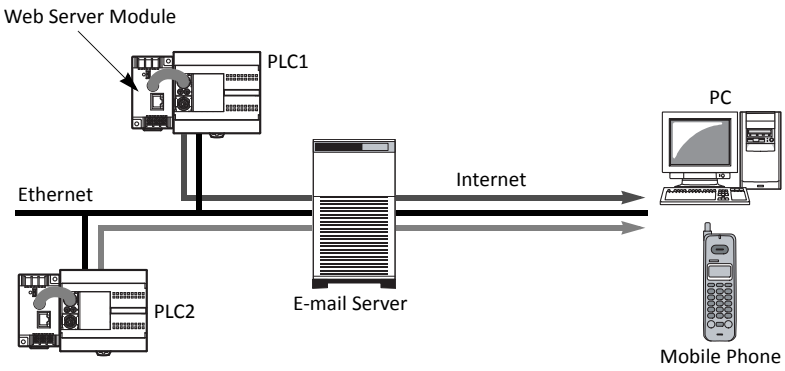
Web Server Module FC4A-SX5ES1E

A New Powerful Tool for the MicroSmart to communicate through Ethernet

- E-mail messages can be sent to PCs and mobile phones to alert a user by programming the MicroSmart to receive inputs of abnormal machine conditions.
- Ethernet communication between the MicroSmart and PC enables remote maintenance.
- User communication enables 1:1 communication between MicroSmart CPU modules via Ethernet.
- Allows for access to data within the MicroSmart using a standard web browser.
- Connect to the MicroSmart and as well as any operator interface with an ethernet interface and a TCP/IP client function.

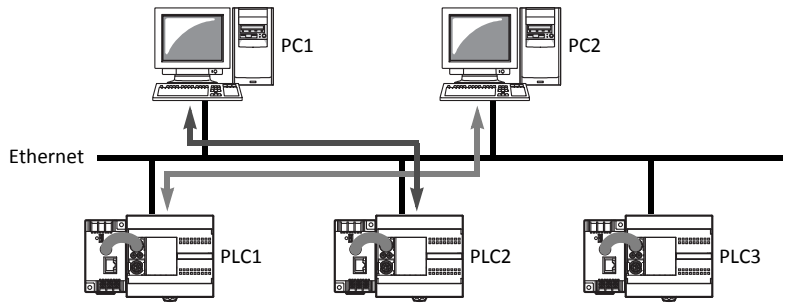
For details about the web server module, see the separate brochure and user's manual.

Sending E-mail messages



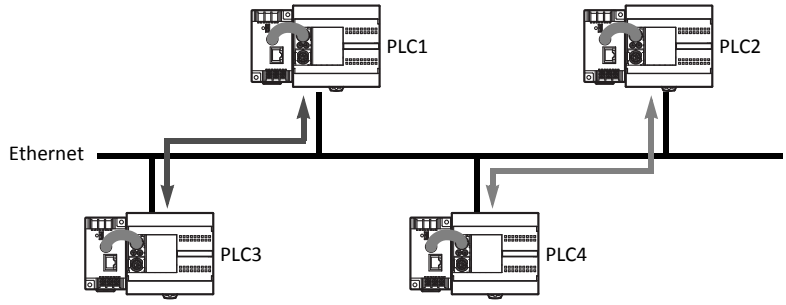
- The MicroSmart is programmed to detect abnormal conditions of machines. When an error occurs, an mail message is sent to the address of PCs and mobile phones registered within the web server module.

Remote monitoring and control



- Operating conditions of machines can be easily monitored and changed from remote places.
- WindLDR functions can be used on a MicroSmart installed in remote places, for monitoring of machines, configuration, and to upload user programs. The MicroSmart does not need special user programs to communicate with a PC. Also, not only WindLDR but standard SCADA software applicable to Ethernet enables graphical displays of monitoring and maintenance status.

Data exchange between two MicroSmart CPU modules

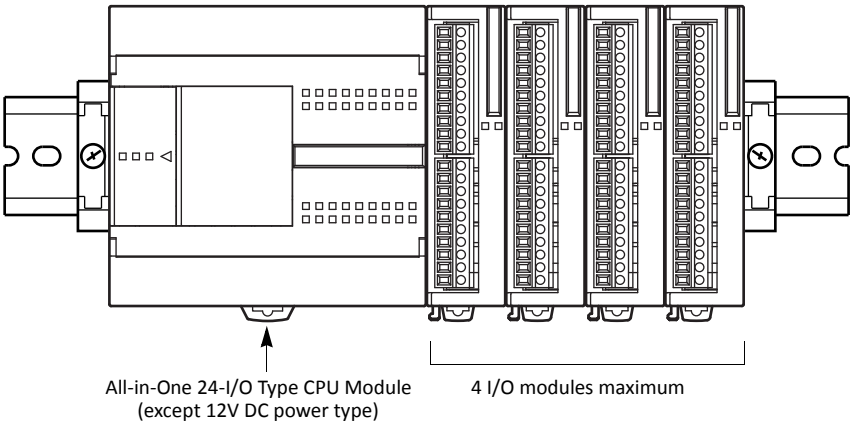


- Data can be exchanged between MicroSmart CPU modules connected with web server modules using the user communication function.

Basic System

The all-in-one 10-I/O type CPU module has 6 input terminals and 4 output terminals. The 16-I/O type CPU module has 9 input terminals and 7 output terminals. The 24-I/O type CPU module has 14 input terminals and 10 output terminals. Only the 24-I/O type CPU module (except 12V DC power type) has an expansion connector to connect I/O modules. When four 16-point input or output modules are connected to the 24-I/O type CPU module, the I/O points can be expanded to a maximum of 88 points.

Any slim type CPU module can add a maximum of seven expansion I/O modules. When using an expansion interface module, eight more expansion I/O modules can be added. For details, see page 2-72.



2: MODULE SPECIFICATIONS

Introduction

This chapter describes MicroSmart modules, parts names, and specifications of each module.

Available modules include all-in-one type and slim type CPU modules, digital input modules, digital output modules, mixed I/O modules, analog I/O modules, HMI module, HMI base module, communication adapters, communication modules, memory cartridge, and clock cartridge.

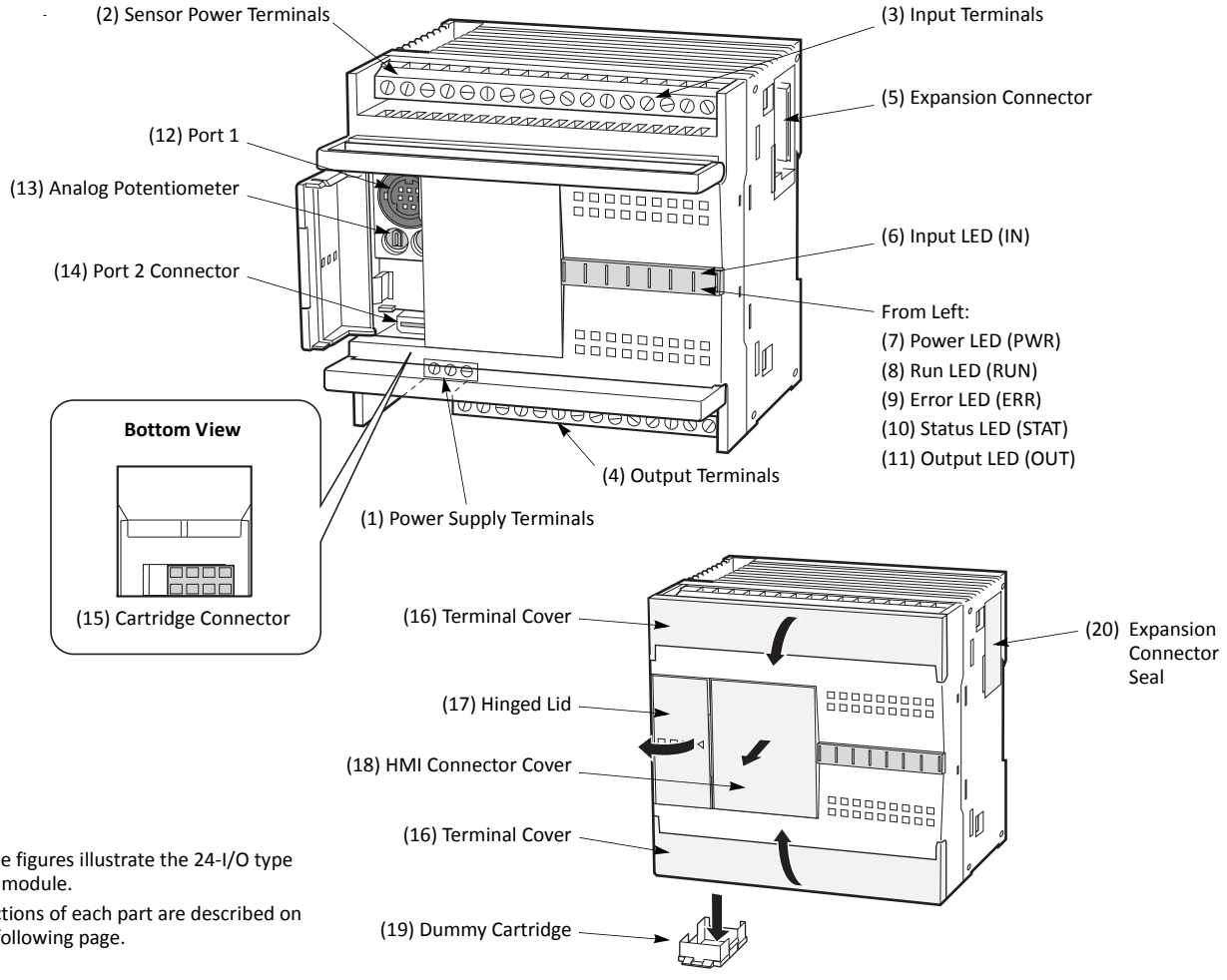
CPU Modules (All-in-One Type)

All-in-one type CPU modules are available in 10-, 16-, and 24-I/O types. The 10-I/O type has 6 input and 4 output terminals, the 16-I/O type 9 input and 7 output terminals, and the 24-I/O type 14 input and 10 output terminals. Every all-in-one type CPU module has communication port 1 for RS232C communication and port 2 connector to install an optional RS232C or RS485 communication adapter for 1:N computer link, modem communication, or data link communication. Every all-in-one type CPU module has a cartridge connector to install an optional memory cartridge or clock cartridge.

CPU Module Type Numbers (All-in-One Type)

Power Voltage	10-I/O Type	16-I/O Type	24-I/O Type
100 -240V AC (50/60 Hz)	FC5A-C10R2	FC5A-C16R2	FC5A-C24R2
24V DC	FC5A-C10R2C	FC5A-C16R2C	FC5A-C24R2C
12V DC	FC5A-C10R2D	FC5A-C16R2D	FC5A-C24R2D

Parts Description (All-in-One Type)



These figures illustrate the 24-I/O type CPU module.

Functions of each part are described on the following page.

(1) Power Supply Terminals
Connect power supply to these terminals. Power voltage 100-240V AC or 24V DC. See page 3-18.

(2) Sensor Power Terminals (AC power type only)
For supplying power to sensors (24V DC, 250mA). These terminals can be used for supplying power to input circuits. Use the sensor power supply only for supplying power to input devices connected to the MicroSmart.

(3) Input Terminals
For connecting input signals from input devices such as sensors, pushbuttons, and limit switches. The input terminals accept both sink and source DC input signals.

(4) Output Terminals
For connecting output signals to output devices such as electromechanical relays and solenoid valves. The internal output relay is rated at 240V AC/2A or 30V DC/2A.

(5) Expansion Connector (only 24-I/O type CPU module except 12V DC power type)
For connecting digital and analog I/O modules to the 24-I/O type CPU module.

(6) Input LED (IN)
Turns on when a corresponding input is on.

(7) Power LED (PWR)
Turns on when power is supplied to the CPU module.

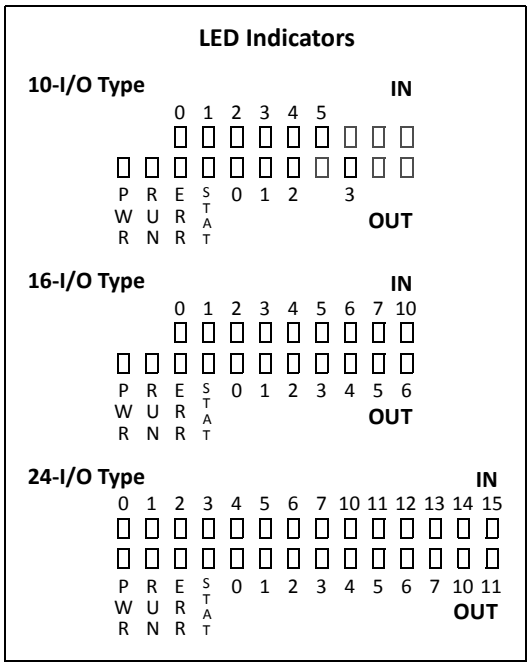
(8) Run LED (RUN)
Turns on when the CPU module is executing the user program.

(9) Error LED (ERR)
Turns on when an error has occurred in the CPU module.

(10) Status LED (STAT)
The status LED can be turned on or off using the user program to indicate a specified status.

(11) Output LED (OUT)
Turns on when a corresponding output is on.

(12) Port 1 (RS232C)
For connecting a computer to download a user program and monitor the PLC operation on a computer using WindLDR.



(13) Analog Potentiometer
Sets a value of 0 through 255 to a special data register. The 10- and 16-I/O types have one potentiometer. The 24-I/O type has two potentiometers. The analog potentiometer can be used to set a preset value for an analog timer.

(14) Port 2 Connector
For connecting an optional RS232C or RS485 communication adapter.

(15) Cartridge Connector
For connecting an optional memory cartridge or clock cartridge.

(16) Terminal Cover
For protecting the input and output terminals. When wiring the terminals, open the covers.

(17) Hinged Lid
Open the lid to gain access to the port 1, port 2 connector, and analog potentiometer.

(18) HMI Connector Cover
Remove the HMI connector cover when using an optional HMI module.

(19) Dummy Cartridge
Remove the dummy cartridge when using an optional memory cartridge or clock cartridge.

(20) Expansion Connector Seal (only 24-I/O type CPU module except 12V DC power type)
Remove the expansion connector seal when connecting an expansion module.

General Specifications (All-in-One Type CPU Module)

Normal Operating Conditions

CPU Module	**AC Power Type**	**FC5A-C10R2**	**FC5A-C16R2**	**FC5A-C24R2**
	24V DC Power Type	**FC5A-C10R2C**	**FC5A-C16R2C**	**FC5A-C24R2C**
	12V DC Power Type	**FC5A-C10R2D**	**FC5A-C16R2D**	**FC5A-C24R2D**
Operating Temperature		0 to 55°C (operating ambient temperature)		
Storage Temperature		–25 to +70°C (no freezing)		
Relative Humidity		10 to 95% (non-condensing, operating and storage humidity)		
Pollution Degree		2 (IEC 60664-1)		
Degree of Protection		IP20 (IEC 60529)		
Corrosion Immunity		Atmosphere free from corrosive gases		
Altitude		Operation: 0 to 2,000m (0 to 6,565 feet) Transport: 0 to 3,000m (0 to 9,840 feet)		
Vibration Resistance		When mounted on a DIN rail or panel surface: 5 to 8.4 Hz amplitude 3.5 mm, 8.4 to 150 Hz acceleration 9.8 m/s^2 (1G) 2 hours per axis on each of three mutually perpendicular axes (IEC 61131-2)		
Shock Resistance		147 m/s^2 (15G), 11 ms duration, 3 shocks per axis on three mutually perpendicular axes (IEC 61131-2)		
ESD Immunity		Contact discharge: ±4 kV, Air discharge: ±8 kV (IEC 61000-4-2)		
Weight	**AC Power Type**	230g	250g	305g
	DC Power Type	240g	260g	310g

Power Supply (AC Power Type)

CPU Module	**FC5A-C10R2**	**FC5A-C16R2**	**FC5A-C24R2**
Rated Power Voltage	100 to 240V AC		
Allowable Voltage Range	85 to 264V AC		
Rated Power Frequency	50/60 Hz (47 to 63 Hz)		
Maximum Input Current	250 mA (85V AC)	300 mA (85V AC)	450 mA (85V AC)
Maximum Power Consumption	30VA (264V AC), 20VA (100V AC) (Note 1)	31VA (264V AC), 22VA (100V AC) (Note 1)	40VA (264V AC), 33VA (100V AC) (Note 2)
Allowable Momentary Power Interruption	10 ms (at the rated power voltage)		
Dielectric Strength	Between power and ⏚ terminals: 1,500V AC, 1 minute Between I/O and ⏚ terminals: 1,500V AC, 1 minute		
Insulation Resistance	Between power and ⏚ terminals: 10 MΩ minimum (500V DC megger) Between I/O and ⏚ terminals: 10 MΩ minimum (500V DC megger)		
Noise Resistance	AC power terminals: 1.5 kV, 50 ns to 1 µs I/O terminals (coupling clamp): 1.5 kV, 50 ns to 1 µs		
Inrush Current	35A maximum	35A maximum	40A maximum
Grounding Wire	UL1007 AWG16		
Power Supply Wire	UL1015 AWG22, UL1007 AWG18		
Effect of Improper Power Supply Connection	Reverse polarity: Normal operation (AC) Improper voltage or frequency: Permanent damage may be caused Improper lead connection: Permanent damage may be caused		

Note 1: Power consumption by the CPU module, including 250mA sensor power

Note 2: Power consumption by the CPU module, including 250mA sensor power, and four I/O modules

Note: The maximum number of relay outputs that can be turned on simultaneously is 33 points (AC power type CPU module) including relay outputs on the CPU module.

Power Supply (DC Power Type)

CPU Module	FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2C FC5A-C24R2D
Allowable Voltage Range	24V DC power type: 20.4 to 28.8V DC 12V DC power type: 10.2 to 18.0V DC		
Maximum Input Current	160 mA (24V DC) 270 mA (10.2V DC)	190 mA (24V DC) 330 mA (10.2V DC)	360 mA (24V DC) 410 mA (10.2V DC)
Maximum Power Consumption	3.9W (24V DC type) (Note 1) 2.8W (12V DC type) (Note 1)	4.6W (24V DC type) (Note 1) 3.4W (12V DC type) (Note 1)	8.7W (24V DC type) (Note 2) 4.2W (12V DC type) (Note 1)
Allowable Momentary Power Interruption	10 ms (at the rated power voltage)		
Dielectric Strength	Between power and ⏚ terminals: 1,500V AC, 1 minute Between I/O and ⏚ terminals: 1,500V AC, 1 minute		
Insulation Resistance	Between power and ⏚ terminals: 10 MΩ minimum (500V DC megger) Between I/O and ⏚ terminals: 10 MΩ minimum (500V DC megger)		
Noise Resistance	IEC61131-2 Zone A compliant (reference values by noise simulator) DC power terminals: 1.0 kV, 50 ns to 1 µs I/O terminals (coupling clamp): 1.5 kV, 50 ns to 1 µs		
Inrush Current	35A max. (24V DC type) 20A max. (12V DC type)	35A max. (24V DC type) 20A max. (12V DC type)	40A max. (24V DC type) 20A max. (12V DC type)
Grounding Wire	UL1007 AWG16		
Power Supply Wire	UL1015 AWG22, UL1007 AWG18		
Effect of Improper Power Supply Connection	Reverse polarity: No operation, no damage Improper voltage or frequency: Permanent damage may be caused Improper lead connection: Permanent damage may be caused		

Note 1: Power consumption by the CPU module

Note 2: Power consumption by the CPU module and four I/O modules

Note: The maximum number of relay outputs that can be turned on simultaneously is 44 points (24V DC power type CPU module) including relay outputs on the CPU module.

Function Specifications (All-in-One Type CPU Module)

CPU Module Specifications

CPU Module		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D	
Program Capacity		13,800 bytes (2,300 steps)	27,000 bytes (4,500 steps)	54,000 bytes (9,000 steps)	
Expandable I/O Modules		—	—	4 modules (Note)	
I/O Points	**Input**	6	9	14	Expansion: 64 (Note)
	Output	4	7	10	
User Program Storage		EEPROM (10,000 rewriting life)			
RAM Backup	**Backup Duration**	Approx. 30 days (typical) at 25°C after backup battery fully charged			
	Backup Data	Internal relay, shift register, counter, data register			
	Battery	Lithium secondary battery			
	Charging Time	Approx. 15 hours for charging from 0% to 90% of full charge			
	Battery Life	5 years in cycles of 9-hour charging and 15-hour discharging			
	Replaceability	Not possible to replace battery			
Control System		Stored program system			
Instruction Words		42 basic 103 advanced	42 basic 103 advanced	42 basic 115 advanced	

CPU Module		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D
Processing Time	**Basic instruction**	1.16 ms (1000 steps) See page A-1.		
	END processing	0.64 ms (not including expansion I/O service, clock function processing, data link processing, and interrupt processing) See page A-5.		
Internal Relay		2048		
Shift Register		128		
Timer		256 (1-sec, 100-ms, 10-ms, 1-ms)		
Counter		256 (adding, dual pulse reversible, up/down selection reversible)		
Data Register		2,000		
Input Filter		Without filter, 3 to 15 ms (selectable in increments of 1 ms)		
Catch Input **Interrupt Input**		Four inputs (I2 through I5) can be designated as catch inputs or interrupt inputs Minimum turn on pulse width: 40 µs maximum Minimum turn off pulse width: 150 µs maximum		
Self-diagnostic Function		Power failure, watchdog timer, data link connection, user program EEPROM sum check, timer/counter preset value sum check, user program RAM sum check, keep data, user program syntax, user program writing, CPU module, clock IC, I/O bus initialize, user program execution		
Start/Stop Method		Turning power on and off Start/stop command in WindLDR Turning start control special internal relay M8000 on and off Turning designated stop or reset input off and on		
High-speed Counter		Total 4 points Single/two-phase selectable: 50 kHz (1 point) Single-phase: 5 kHz (3 points) Counting range: 0 to 65535 (16 bits) Operation mode: Rotary encoder mode and adding counter mode		
Analog Potentiometer		1 point	1 point	2 points
		Data range: 0 to 255		
Sensor Power Supply (AC power type only)		Output voltage/current: 24V DC (+10% to –15%), 250 mA Overload detection: Not available Isolation: Isolated from the internal circuit		
Communication Port		Port 1 (RS232C) Port 2 connector		
Cartridge Connector		1 point for connecting a memory cartridge (32KB or 64KB) or a clock cartridge		

Note: The 12V DC power type CPU module cannot connect expansion I/O modules.

System Statuses at Stop, Reset, and Restart

Mode	Output	Internal Relay, Shift Register, Counter, Data Register		Timer Current Value
		Keep Type	Clear Type	
Run	Operating	Operating	Operating	Operating
Stop (Stop input ON)	OFF	Unchanged	Unchanged	Unchanged
Reset (Reset input ON)	OFF	OFF/Reset to zero	OFF/Reset to zero	Reset to zero
Restart	Unchanged	Unchanged	OFF/Reset to zero	Reset to preset

Communication Function

Communication Port	Port 1	Port 2		
Communication Adapter	**—**	**FC4A-PC1**	**FC4A-PC2**	**FC4A-PC3**
Standards	EIA RS232C	EIA RS232C	EIA RS485	EIA RS485
Maximum Baud Rate	57,600 bps	57,600 bps	57,600 bps	57,600 bps
Maintenance Communication (Computer Link)	Possible	Possible	Possible	Possible
User Communication	Possible	Possible	—	Possible
Modem Communication	—	Possible	—	—
Data Link Communication	—	—	—	Possible (31 slaves max.)
Modbus Communication	—	Possible (Note 1)	—	Possible
Maximum Cable Length	Special cable (Note 2)	Special cable (Note 2)	Special cable (Note 2)	200m (Note 3)
Isolation between Internal Circuit and Communication Port	Not isolated	Not isolated	Not isolated	Not isolated

Note 1: 1:1 Modbus communication only

Note 2: For special cables, see page A-12.

Note 3: Recommended cable for RS485: Twisted-pair shielded cable with a minimum core wire of 0.3 mm^2.
Conductor resistance 85 Ω/km maximum, shield resistance 20 Ω/km maximum.

Memory Cartridge (Option)

Memory Type	EEPROM
Accessible Memory Capacity	32 KB, 64 KB, 128 KB The maximum program capacity depends on the CPU module. When using the 32 KB memory cartridge on the 24-I/O type CPU module, the maximum program capacity is limited to 30,000 bytes.
Hardware for Storing Data	CPU module
Software for Storing Data	WindLDR
Quantity of Stored Programs	One user program can be stored on one memory cartridge.
Program Execution Priority	When a memory cartridge is installed, the user program on the memory cartridge is executed. User programs can be downloaded from the memory cartridge to the CPU module. User programs can also be uploaded to the memory cartridge from upgraded CPU modules with system program version 200 or higher.

Clock Cartridge (Option)

Accuracy	±30 sec/month (typical) at 25°C
Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged
Battery	Lithium secondary battery
Charging Time	Approx. 10 hours for charging from 0% to 90% of full charge
Battery Life	Approx. 100 recharge cycles after discharging down to 10% of full charge
Replaceability	Not possible to replace battery

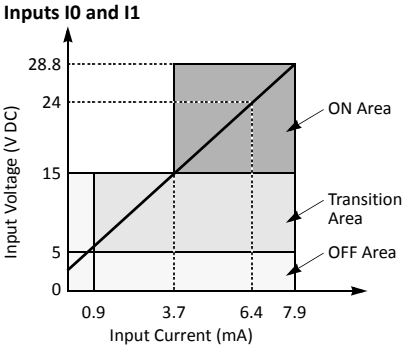
DC Input Specifications (All-in-One Type CPU Module: AC power and 24V DC power)

CPU Module	FC5A-C10R2 FC5A-C10R2C	FC5A-C16R2 FC5A-C16R2C	FC5A-C24R2 FC5A-C24R2C
Input Points and Common Line	6 points in 1 common line	9 points in 1 common line	14 points in 1 common line
Terminal Arrangement	See CPU Module Terminal Arrangement on pages 2-10 and 2-11.		
Rated Input Voltage	24V DC sink/source input signal		
Input Voltage Range	20.4 to 28.8V DC		
Rated Input Current	I0 and I1: 6.4 mA/point (24V DC) I2 to I7, I10 to I15: 7 mA/point (24V DC)		
Input Impedance	I0 and I1: 3.7 kΩ I2 to I7, I10 to I15: 3.4 kΩ		
Turn ON Time	I0 and I1: 2 µs + filter value I2 to I5: 35 µs + filter value I6, I7, I10 to I15: 40 µs + filter value		
Turn OFF Time	I0 and I1: 16 µs + filter value I2 to I5: 150 µs + filter value I6, I7, I10 to I15: 150 µs + filter value		
Isolation	Between input terminals: Not isolated Internal circuit: Photocoupler isolated		
Input Type	Type 1 (IEC 61131-2)		
External Load for I/O Interconnection	Not needed		
Signal Determination Method	Static		
Effect of Improper Input Connection	Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.		
Cable Length	3m (9.84 ft.) in compliance with electromagnetic immunity		

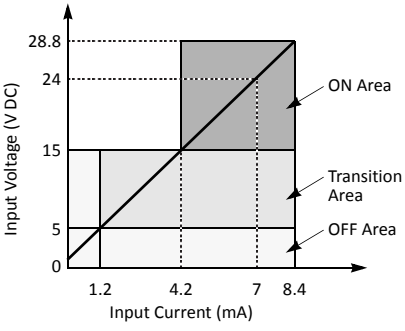
Input Operating Range

The input operating range of Type 1 (IEC 61131-2) input modules is shown below:

Inputs I0 and I1

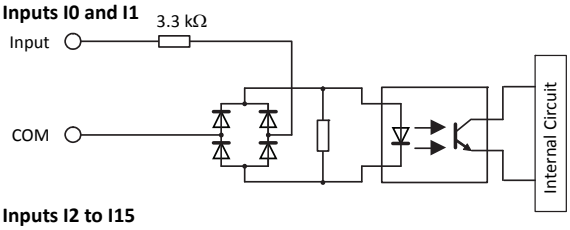


Inputs I2 to I15

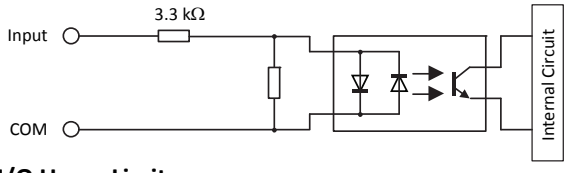


Input Internal Circuit

Inputs I0 and I1

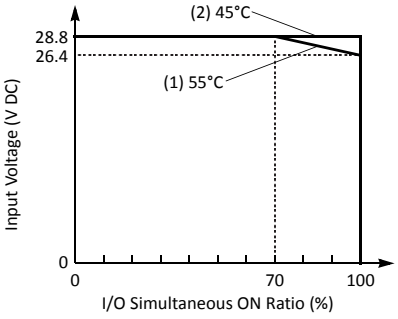


Inputs I2 to I15



I/O Usage Limits

When using the FC5A-C16R2/C or FC5A-C24R2/C at an ambient temperature of 55°C in the normal mounting direction, limit the inputs and outputs, respectively, which turn on simultaneously along line (1).



When using at 45°C, all I/Os can be turned on simultaneously at input voltage 28.8V DC as indicated with line (2).

When using the FC5A-C10R2/C, all I/Os can be turned on simultaneously at 55°C, input voltage 28.8V DC.

For other possible mounting directions, see page 3-14.

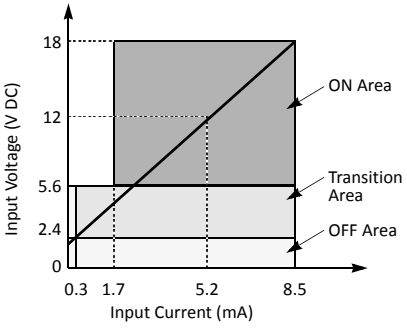
DC Input Specifications (All-in-One Type CPU Module: 12V DC power)

CPU Module	FC5A-C10R2D	FC5A-C16R2D	FC5A-C24R2D
Input Points and Common Line	6 points in 1 common line	9 points in 1 common line	14 points in 1 common line
Terminal Arrangement	See CPU Module Terminal Arrangement on page 2-12.		
Rated Input Voltage	12V DC sink/source input signal		
Input Voltage Range	10.2 to 18.0V DC		
Rated Input Current	I0 and I1: 6 mA/point (12V DC) I2 to I7, I10 to I15: 6 mA/point (12V DC)		
Input Impedance	I0 and I1: 1.8 kΩ I2 to I7, I10 to I15: 2.0 kΩ		
Turn ON Time	I0 and I1: 2 µs + filter value I2 to I5: 35 µs + filter value I6, I7, I10 to I15: 40 µs + filter value		
Turn OFF Time	I0 and I1: 16 µs + filter value I2 to I5: 150 µs + filter value I6, I7, I10 to I15: 150 µs + filter value		
Isolation	Between input terminals: Not isolated Internal circuit: Photocoupler isolated		
Input Type	Type 1 (IEC 61131-2)		
External Load for I/O Interconnection	Not needed		
Signal Determination Method	Static		
Effect of Improper Input Connection	Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.		
Cable Length	3m (9.84 ft.) in compliance with electromagnetic immunity		

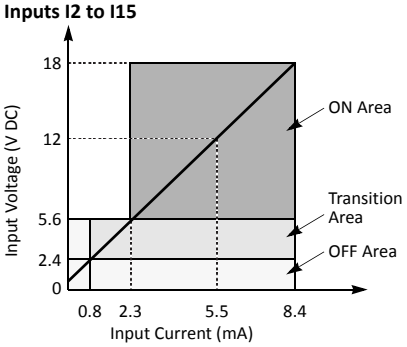
Input Operating Range

The input operating range of Type 1 (IEC 61131-2) input modules is shown below:

Inputs I0 and I1

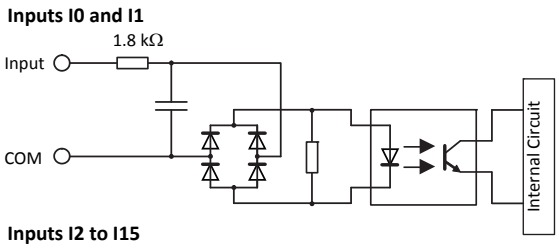


Inputs I2 to I15

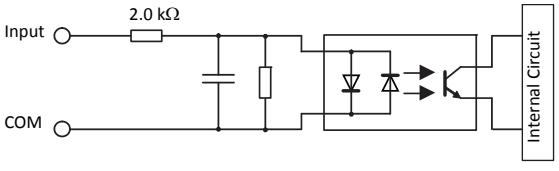


Input Internal Circuit

Inputs I0 and I1



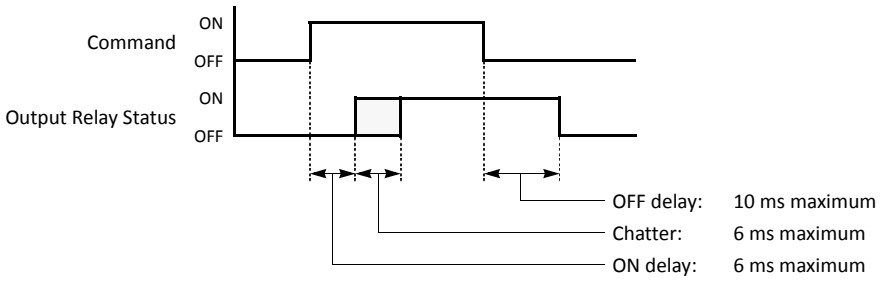
Inputs I2 to I15



Relay Output Specifications (All-in-One Type CPU Module)

CPU Module		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D
No. of Outputs		4 points	7 points	10 points
Output Points per Common Line	**COM0**	3 NO contacts	4 NO contacts	4 NO contacts
	COM1	1 NO contact	2 NO contacts	4 NO contacts
	COM2	—	1 NO contact	1 NO contact
	COM3	—	—	1 NO contact
Terminal Arrangement		See CPU Module Terminal Arrangement on pages 2-10 and 2-11.		
Maximum Load Current (resistive/inductive load)		2A per point 8A per common line		
Minimum Switching Load		1 mA/5V DC (reference value)		
Initial Contact Resistance		30 mΩ maximum		
Electrical Life		100,000 operations minimum (rated load 1,800 operations/hour)		
Mechanical Life		20,000,000 operations minimum (no load 18,000 operations/hour)		
Rated Load		240V AC/2A (resistive load, inductive load cos ø = 0.4) 30V DC/2A (resistive load, inductive load L/R = 7 ms)		
Dielectric Strength		Between output and ⏚ or ⏚ terminals: 1,500V AC, 1 minute Between output terminal and internal circuit: 1,500V AC, 1 minute Between output terminals (COMs): 1,500V AC, 1 minute		
Contact Protection Circuit for Relay Output		See page 3-17.		

Output Delay



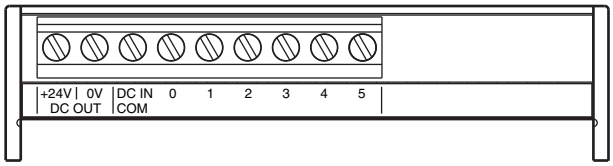
CPU Module Terminal Arrangement (All-in-One Type)

The input and output terminal arrangements of the all-in-one type CPU modules are shown below.

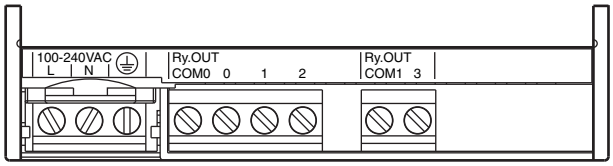
AC Power Type CPU Module

FC5A-C10R2

Sensor Power Terminals
Input Terminals

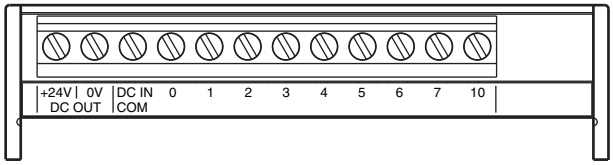


AC Power Terminals
Output Terminals

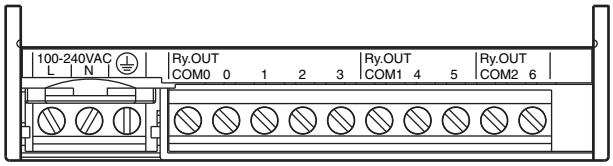


FC5A-C16R2

Sensor Power Terminals
Input Terminals

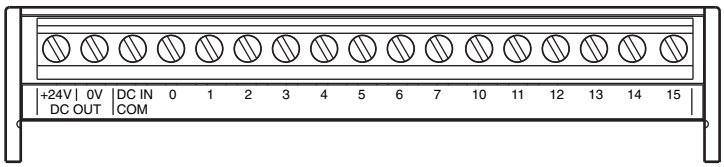


AC Power Terminals
Output Terminals

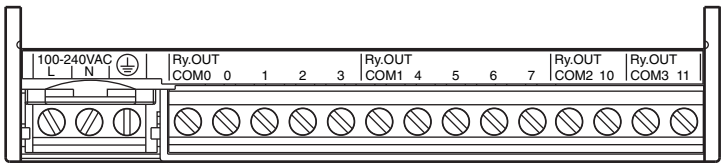


FC5A-C24R2

Sensor Power Terminals
Input Terminals



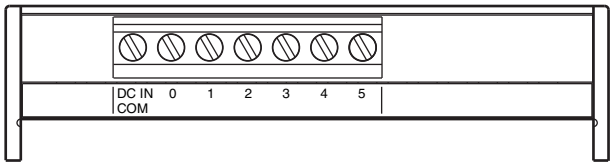
AC Power Terminals
Output Terminals



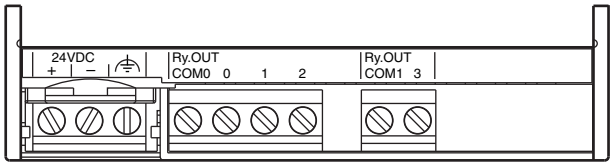
24V DC Power Type CPU Module

FC5A-C10R2C

Input Terminals

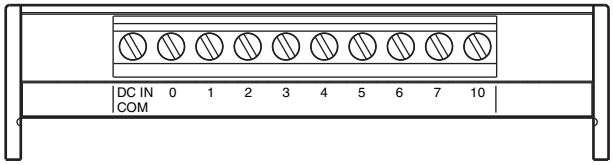


DC Power Terminals
Output Terminals

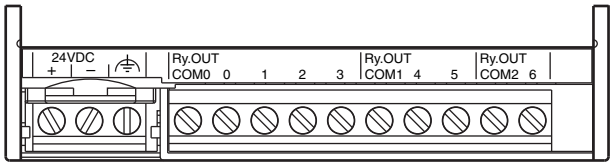


FC5A-C16R2C

Input Terminals

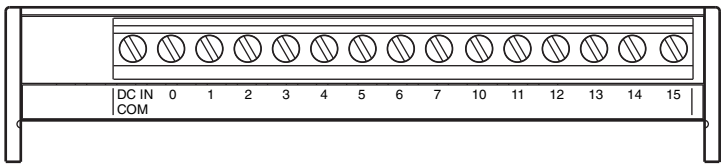


DC Power Terminals
Output Terminals

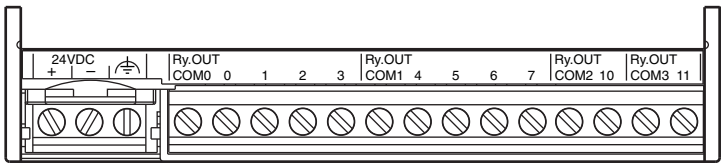


FC5A-C24R2C

Input Terminals



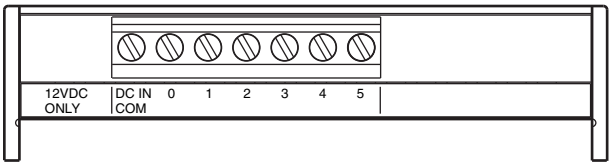
DC Power Terminals
Output Terminals



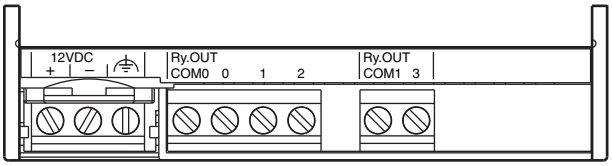
12V DC Power Type CPU Module

FC5A-C10R2D

Input Terminals

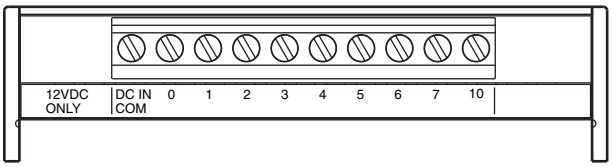


DC Power Terminals
Output Terminals

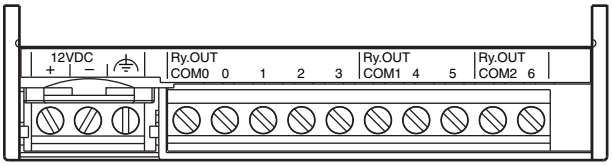


FC5A-C16R2D

Input Terminals

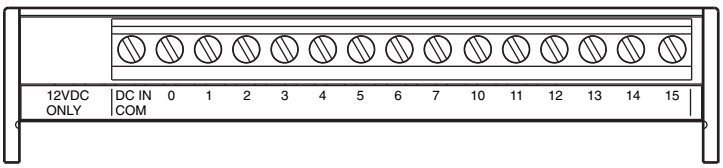


DC Power Terminals
Output Terminals

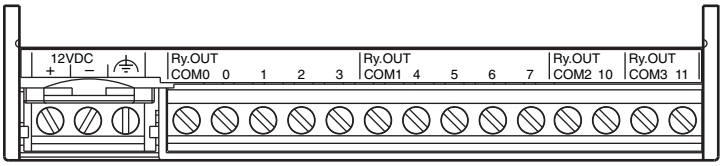


FC5A-C24R2D

Input Terminals

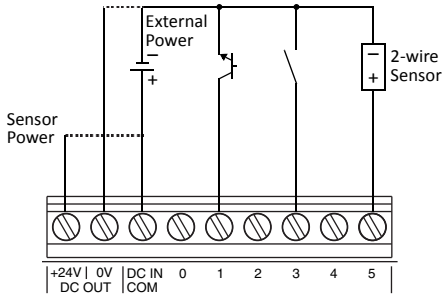
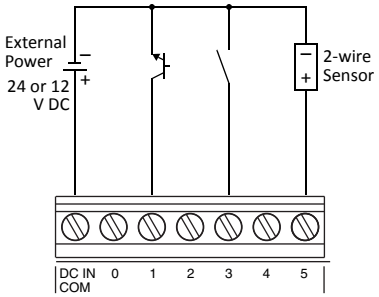
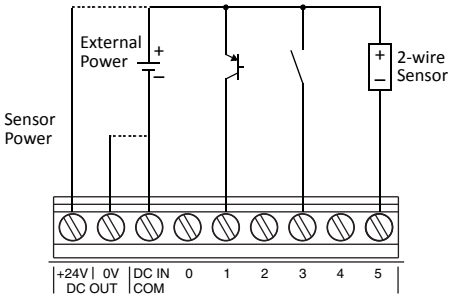
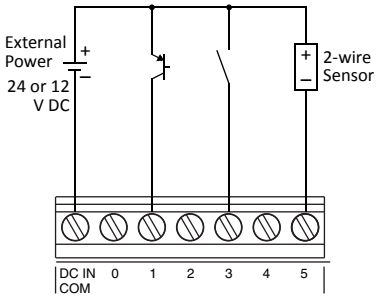
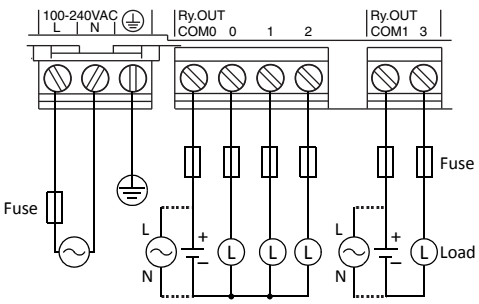
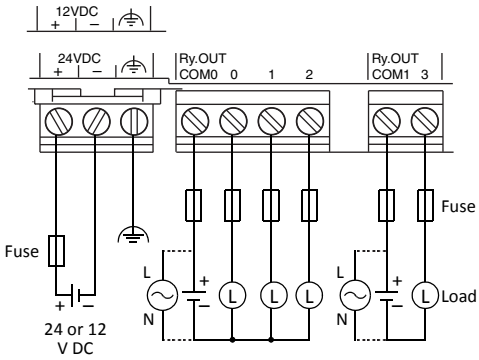


DC Power Terminals
Output Terminals



I/O Wiring Diagrams (All-in-One Type CPU Module)

The input and output wiring examples of the CPU modules are shown below. For wiring precautions, see pages 3-15 through 3-18.

AC Power Type CPU Module	24 or 12V DC Power Type CPU Module
DC Source Input Wiring	**DC Source Input Wiring**
	
DC Sink Input Wiring	**DC Sink Input Wiring**
	
AC Power and Relay Output Wiring	**DC Power and Relay Output Wiring**
	

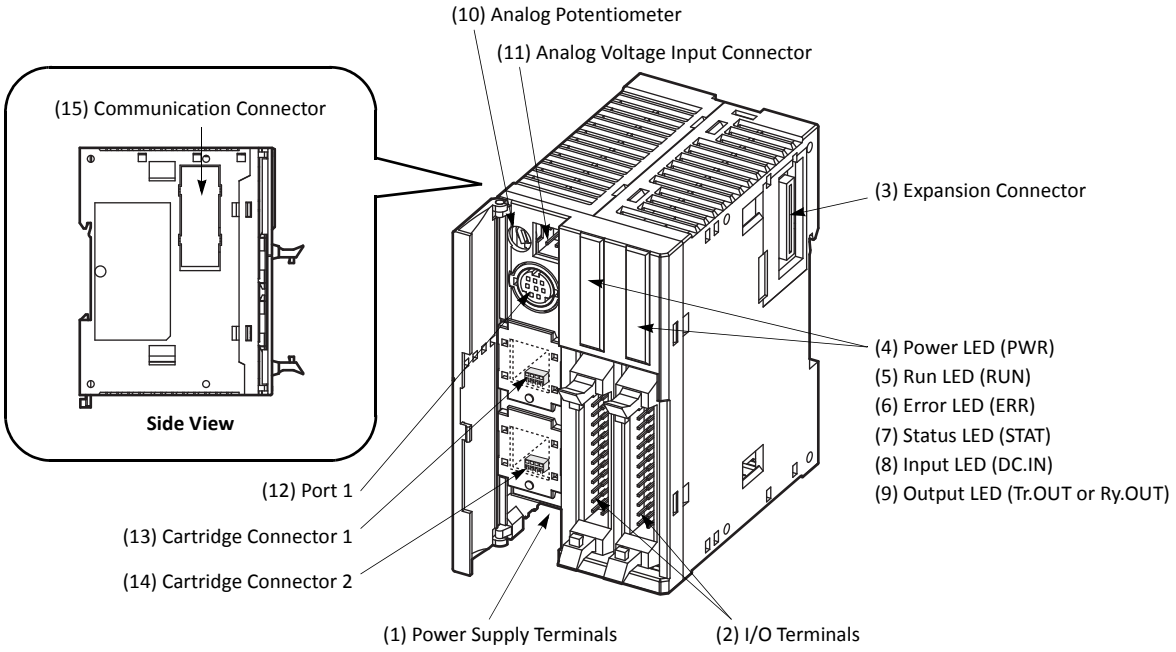
CPU Modules (Slim Type)

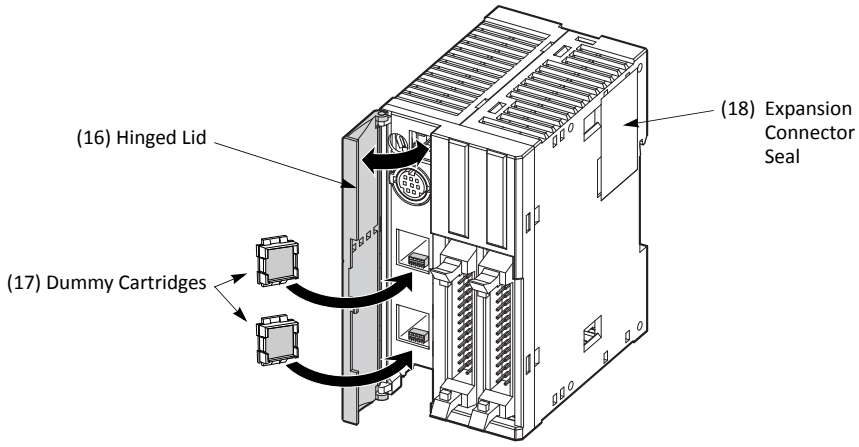
Slim type CPU modules are available in 16- and 32-I/O types. The 16-I/O type has 8 input and 8 output terminals, and the 32-I/O type has 16 input and 16 output terminals. The FC5A-D16RK1 and FC5A-D16RS1 have 2 transistor outputs used for high-speed outputs and pulse outputs in addition to 6 relay outputs. Every slim type CPU module has communication port 1 for RS232C communication, and can mount an optional RS232C or RS485 communication module for 1:N computer link, modem communication, and data link communication. The HMI base module can also be mounted to install an optional HMI module and a communication adapter. Every slim type CPU module has two cartridge connectors to install an optional memory cartridge and a clock cartridge.

CPU Module Type Numbers (Slim Type)

I/O Points	Output Type	High-speed Transistor Output (Q0 & Q1)	Type No.
16 (8 in / 8 out)	Relay Output 240V AC/30V DC, 2A	Sink Output 0.3A	FC5A-D16RK1
		Source Output 0.3A	FC5A-D16RS1
32 (16 in / 16 out)	Transistor Sink Output 0.3A		FC5A-D32K3
	Transistor Source Output 0.3A		FC5A-D32S3

Parts Description (Slim Type)





These figures illustrate the 32-I/O type CPU module.

Functions of each part are described on the following page.

(1) Power Supply Terminals

Connect power supply to these terminals. Power voltage 24V DC. See page 3-19.

(2) I/O Terminals

For connecting input and output signals. The input terminals accept both sink and source 24V DC input signals. Transistor and relay output types are available. Transistor output type has MIL connectors and relay output type has removable screw connectors.

(3) Expansion Connector

For connecting digital and analog I/O modules.

(4) Power LED (PWR)

Turns on when power is supplied to the CPU module.

(5) Run LED (RUN)

Turns on when the CPU module is executing the user program.

(6) Error LED (ERR)

Turns on when an error occurs in the CPU module.

(7) Status LED (STAT)

The status LED can be turned on or off using the user program to indicate a specified status.

(8) Input LED (IN)

Turns on when a corresponding input is on.

(9) Output LED (Tr.OUT or Ry.OUT)

Turns on when a corresponding output is on.

(10) Analog Potentiometer

Sets a value of 0 through 255 to a special data register. All slim type CPU modules have one potentiometer, which can be used to set a preset value for an analog timer.

(11) Analog Voltage Input Connector

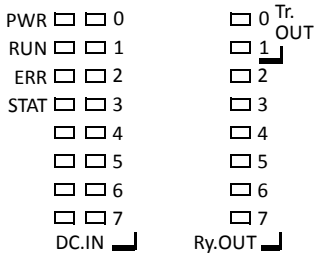
For connecting an analog voltage source of 0 through 10V DC. The analog voltage is converted to a value of 0 through 255 and stored to a special data register.

(12) Port 1 (RS232C)

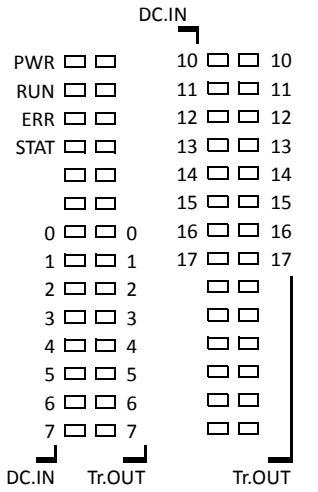
For connecting a computer to download a user program and monitor the PLC operation on a computer using WindLDR.

LED Indicators

16-I/O Type (Relay Output)



32-I/O Type (Transistor Output)



(13) Cartridge Connector 1

For connecting an optional memory cartridge or clock cartridge.

(14) Cartridge Connector 2

For connecting an optional memory cartridge or clock cartridge.

(15) Communication Connector

For connecting an optional communication module or HMI base module. Remove the connector cover before connecting a module.

(16) Hinged Lid

Open the lid to gain access to the port 1, cartridge connectors 1 and 2, analog potentiometer, and analog voltage input connector.

(17) Dummy Cartridges

Remove the dummy cartridge when using an optional memory cartridge or clock cartridge.

(18) Expansion Connector Seal

Remove the expansion connector seal when connecting an expansion module.

General Specifications (Slim Type CPU Module)

Normal Operating Conditions

CPU Module	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3
Operating Temperature	0 to 55°C (operating ambient temperature)	
Storage Temperature	–25 to +70°C	
Relative Humidity	10 to 95% (non-condensing, operating and storage humidity)	
Pollution Degree	2 (IEC 60664-1)	
Degree of Protection	IP20 (IEC 60529)	
Corrosion Immunity	Atmosphere free from corrosive gases	
Altitude	Operation: 0 to 2,000m (0 to 6,565 feet) Transport: 0 to 3,000m (0 to 9,840 feet)	
Vibration Resistance	When mounted on a DIN rail or panel surface: 5 to 8.4 Hz amplitude 3.5 mm, 8.4 to 150 Hz acceleration 9.8 m/s^2 (1G) 2 hours per axis on each of three mutually perpendicular axes (IEC 61131-2)	
Shock Resistance	147 m/s^2 (15G), 11 ms duration, 3 shocks per axis on three mutually perpendicular axes (IEC 61131-2)	
ESD Immunity	Contact discharge: ±4 kV, Air discharge: ±8 kV (IEC 61000-4-2)	
Weight	230g	190g

Power Supply

Rated Power Voltage	24V DC	
Allowable Voltage Range	20.4 to 26.4V DC (including ripple)	
Maximum Input Current	700 mA (26.4V DC)	700 mA (26.4V DC)
Maximum Power Consumption (Note 1, 2)	CPU module + 7 I/O modules + expansion module + 8 I/O modules	
	19W (26.4V DC)	19W (26.4V DC)
Allowable Momentary Power Interruption	10 ms (at 24V DC)	
Dielectric Strength	Between power and ⏚ terminals: 500V AC, 1 minute Between I/O and ⏚ terminals: 500V AC, 1 minute	
Insulation Resistance	Between power and ⏚ terminals: 10 MΩ minimum (500V DC megger) Between I/O and ⏚ terminals: 10 MΩ minimum (500V DC megger)	
Noise Resistance	DC power terminals: 1.0 kV, 50 ns to 1 µs I/O terminals (coupling clamp): 1.5 kV, 50 ns to 1 µs	
Inrush Current	50A maximum (24V DC)	
Grounding Wire	UL1015 AWG22, UL1007 AWG18	
Power Supply Wire	UL1015 AWG22, UL1007 AWG18	
Effect of Improper Power Supply Connection	Reverse polarity: No operation, no damage Improper voltage or frequency: Permanent damage may be caused Improper lead connection: Permanent damage may be caused	

Note 1: Among relay outputs on the CPU module and relay output modules connected to the CPU module, a maximum of 54 points can be turned on simultaneously. Among relay outputs connected beyond the expansion module, a maximum of 54 points can be turned on simultaneously. Relay outputs exceeding these limits may not turn on correctly.

Note 2: Maximum power consumption for individual CPU module is 3.0W (125 mA at 24V DC) for FC5A-D16RK1/RS1 and 3.4W (140 mA at 24V DC) for FC5A-D32K3/S3.

Function Specifications (Slim Type CPU Module)

CPU Module Specifications

CPU Module		FC5A-D16RK1 FC5A-D16RS1		FC5A-D32K3 FC5A-D32S3	
Program Capacity		62,400 bytes (10,400 steps)			
Expandable I/O Modules		7 modules + additional 8 modules using the expansion interface module			
I/O Points	Input	8	Expansion: 224 (Note 1) Additional: 256 (Note 2)	16	Expansion: 224 (Note 1) Additional: 256 (Note 2)
	Output	8		16	
User Program Storage		EEPROM (10,000 rewriting life)			
RAM Backup	Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged			
	Backup Data	Internal relay, shift register, counter, data register, expansion data register			
	Battery	Lithium secondary battery			
	Charging Time	Approx. 15 hours for charging from 0% to 90% of full charge			
	Battery Life	5 years in cycles of 9-hour charging and 15-hour discharging			
	Replaceability	Not possible to replace battery			
Control System		Stored program system			
Instruction Words		42 basic 126 advanced		42 basic 130 advanced	
Processing Time	Basic instruction	83 µs (1000 steps) See page A-1.			
	END processing	0.35 ms (not including expansion I/O service, clock function processing, data link processing, and interrupt processing) See page A-5.			
Internal Relay		2,048			
Shift Register		256			
Timer		256 (1-sec, 100-ms, 10-ms, 1-ms)			
Counter		256 (adding, dual pulse reversible, up/down selection reversible)			
Data Register		2,000			
Expansion Data Register		6,000			
Extra Data Register		40,000 (Note 3)			
Input Filter		Without filter, 3 to 15 ms (selectable in increments of 1 ms)			
Catch Input Interrupt Input		Four inputs (I2 through I5) can be designated as catch inputs or interrupt inputs I2 and I5: Minimum turn on pulse width: 40 µs maximum Minimum turn off pulse width: 150 µs maximum I3 and I4: Minimum turn on pulse width: 5 µs maximum Minimum turn off pulse width: 5 µs maximum			
Self-diagnostic Function		Power failure, watchdog timer, data link connection, user program EEPROM sum check, timer/counter preset value sum check, user program RAM sum check, keep data, user program syntax, user program writing, CPU module, clock IC, I/O bus initialize, user program execution			
Start/Stop Method		Turning power on and off Start/stop command in WindLDR Turning start control special internal relay M8000 on and off Turning designated stop or reset input off and on			
High-speed Counter		Total 4 points Single/two-phase selectable: 100 kHz (2 points) Single-phase: 100 kHz (2 points) Counting range: 0 to 4,294,967,295 (32 bits) Operation mode: Rotary encoder mode and adding counter mode			
Analog Potentiometer		1 point		1 point	
		Data range: 0 to 255			

Analog Voltage Input	Quantity: Input voltage range: Input impedance: Data range:	1 point 0 to 10V DC Approx. 100 kΩ 0 to 255 (8 bits)	
Pulse Output	2 points		3 points
	Maximum frequency:	100 kHz	
Communication Port	Port 1 (RS232C) Communication connector for port 2		
Cartridge Connector	2 points for connecting a memory cartridge (32KB or 64KB) and a clock cartridge		

Note 1: The maximum number of outputs that can be turned on simultaneously is 54 including those on the CPU module.

Note 2: Among the additional I/O modules, the maximum number of outputs that can be turned on simultaneously is 54.

Note 3: Extra data registers D10000 through D49999 are enabled using WindLDR Function Area Settings, then run-time program download cannot be used.

System Statuses at Stop, Reset, and Restart

Mode	Output	Internal Relay, Shift Register, Counter, Data Register, Expansion DR, Extra DR		Timer Current Value
		Keep Type	Clear Type	
Run	Operating	Operating	Operating	Operating
Stop (Stop input ON)	OFF	Unchanged	Unchanged	Unchanged
Reset (Reset input ON)	OFF	OFF/Reset to zero	OFF/Reset to zero	Reset to zero
Restart	Unchanged	Unchanged	OFF/Reset to zero	Reset to preset

Note: All expansion data registers are keep types.

Communication Function

Communication Port	Port 1	Port 2		
Communication Adapter	—	**FC4A-PC1**	**FC4A-PC2**	**FC4A-PC3**
Communication Module	—	**FC4A-HPC1**	**FC4A-HPC2**	**FC4A-HPC3**
Standards	EIA RS232C	EIA RS232C	EIA RS485	EIA RS485
Maximum Baud Rate	57,600 bps	57,600 bps	57,600 bps	57,600 bps
Maintenance Communication (Computer Link)	Possible	Possible	Possible	Possible
User Communication	Possible	Possible	—	Possible
Modem Communication	—	Possible	—	—
Data Link Communication	—	—	—	Possible (31 slaves max.)
Modbus Communication	—	Possible (Note 1)	—	Possible
Maximum Cable Length	Special cable (Note 2)	Special cable (Note 2)	Special cable (Note 2)	200m (Note 3)
Isolation between Internal Circuit and Communication Port	Not isolated	Not isolated	Not isolated	Not isolated

Note 1: 1:1 Modbus communication only

Note 2: For special cables, see page A-12.

Note 3: Recommended cable for RS485: Twisted-pair shielded cable with a minimum core wire of 0.3 mm^2.
Conductor resistance 85 Ω/km maximum, shield resistance 20 Ω/km maximum.

Memory Cartridge (Option)

Memory Type	EEPROM
Accessible Memory Capacity	32 KB, 64 KB, 128 KB The maximum program capacity depends on the CPU module. When using the 32 KB memory cartridge on the slim type CPU module, the maximum program capacity is limited to 30,000 bytes.
Hardware for Storing Data	CPU module
Software for Storing Data	WindLDR
Quantity of Stored Programs	One user program can be stored on one memory cartridge.
Program Execution Priority	When a memory cartridge is installed, the user program on the memory cartridge is executed. User programs can be downloaded from the memory cartridge to the CPU module. User programs can also be uploaded to the memory cartridge from upgraded CPU modules with system program version 200 or higher.

Clock Cartridge (Option)

Accuracy	±30 sec/month (typical) at 25°C
Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged
Battery	Lithium secondary battery
Charging Time	Approx. 10 hours for charging from 0% to 90% of full charge
Battery Life	Approx. 100 recharge cycles after discharging down to 10% of full charge
Replaceability	Not possible to replace battery

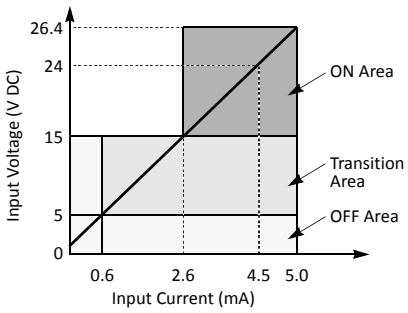
DC Input Specifications (Slim Type CPU Module)

CPU Module	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3
Input Points and Common Lines	8 points in 1 common line	16 points in 2 common lines
Terminal Arrangement	See CPU Module Terminal Arrangement on pages 2-23 through 2-25.	
Rated Input Voltage	24V DC sink/source input signal	
Input Voltage Range	20.4 to 26.4V DC	
Rated Input Current	I0, I1, I3, I4, I6, I7: 4.5 mA/point (24V DC) I2, I5, I10 to I17: 7 mA/point (24V DC)	
Input Impedance	I0, I1, I3, I4, I6, I7: 4.9 kΩ I2, I5, I10 to I17: 3.4 kΩ	
Turn ON Time	I0, I1, I3, I4, I6, I7: 5 µs + filter value I2, I5: 35 µs + filter value I10 to I17: 40 µs + filter value	
Turn OFF Time	I0, I1, I3, I4, I6, I7: 5 µs + filter value I2, I5: 150 µs + filter value I10 to I17: 150 µs + filter value	
Isolation	Between input terminals: Not isolated Internal circuit: Photocoupler isolated	
Input Type	Type 1 (IEC 61131)	
External Load for I/O Interconnection	Not needed	
Signal Determination Method	Static	
Effect of Improper Input Connection	Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.	
Cable Length	3m (9.84 ft.) in compliance with electromagnetic immunity	
Connector on Mother Board	MC1.5/13-G-3.81BK (Phoenix Contact)	FL26A2MA (Oki Electric Cable)
Connector Insertion/Removal Durability	100 times minimum	

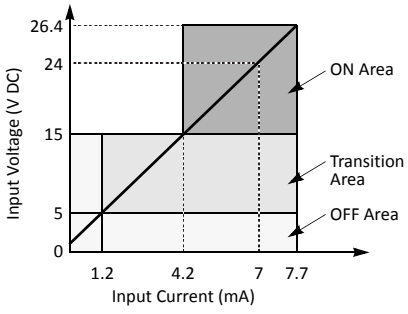
Input Operating Range

The input operating range of the Type 1 (IEC 61131-2) input module is shown below:

Inputs I0, I1, I3, I4, I6, and I7

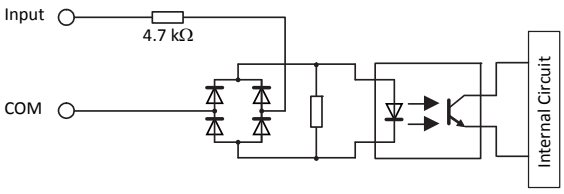


Inputs I2, I5, and I10 to I17

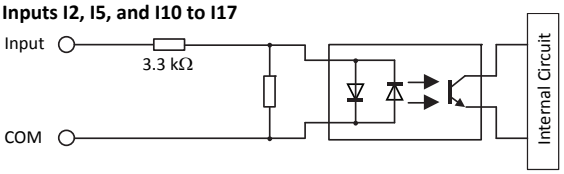


Input Internal Circuit

Inputs I0, I1, I3, I4, I6, and I7



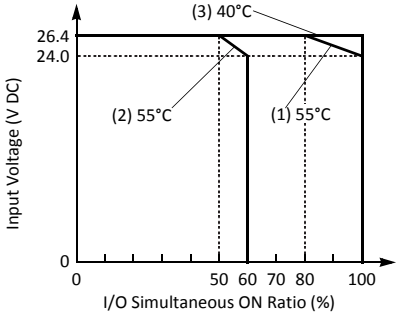
Inputs I2, I5, and I10 to I17



I/O Usage Limits

When using the FC5A-D16RK1/RS1 at an ambient temperature of 55°C in the normal mounting direction, limit the inputs and outputs, respectively, which turn on simultaneously on each connector along line (1).

When using the FC5A-D32K3/S3, limit the inputs and outputs, respectively, which turn on simultaneously on each connector along line (2).

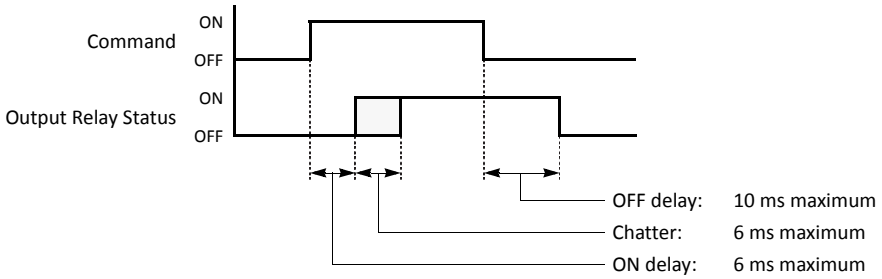


When using at 40°C, all I/Os on every slim type CPU module can be turned on simultaneously at 26.4V DC as indicated with line (3)

Relay Output Specifications (Slim Type CPU Module)

CPU Module		FC5A-D16RK1	FC5A-D16RS1
No. of Outputs		8 points including 2 transistor output points	
Output Points per Common Line	**COM0**	(2 points transistor sink output)	(2 points transistor source output)
	COM1	3 NO contacts	
	COM2	2 NO contacts	
	COM3	1 NO contact	
Terminal Arrangement		See CPU Module Terminal Arrangement on page 2-23.	
Maximum Load Current		2A per point 8A per common line	
Minimum Switching Load		1 mA/5V DC (reference value)	
Initial Contact Resistance		30 mΩ maximum	
Electrical Life		100,000 operations minimum (rated load 1,800 operations/hour)	
Mechanical Life		20,000,000 operations minimum (no load 18,000 operations/hour)	
Rated Load		240V AC/2A (resistive load, inductive load cos ø = 0.4) 30V DC/2A (resistive load, inductive load L/R = 7 ms)	
Dielectric Strength		Between output and ⏚ terminals: 1,500V AC, 1 minute Between output terminal and internal circuit: 1,500V AC, 1 minute Between output terminals (COMs): 1,500V AC, 1 minute	
Connector on Mother Board		MC1.5/16-G-3.81BK (Phoenix Contact)	
Connector Insertion/Removal Durability		100 times minimum	
Contact Protection Circuit for Relay Output		See page 3-17.	

Output Delay

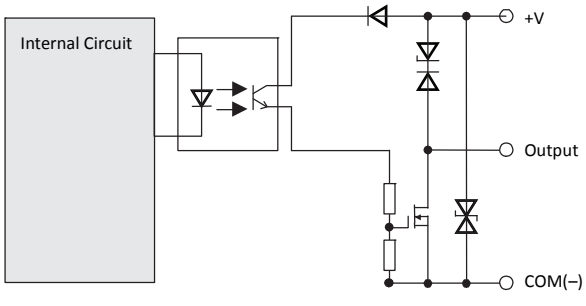


Transistor Sink and Source Output Specifications (Slim Type CPU Module)

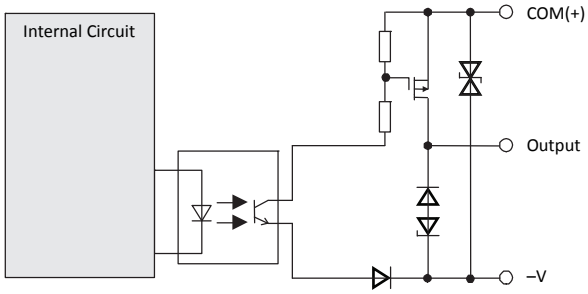
CPU Module		FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3
Output Type		FC5A-D16RK1: Sink output FC5A-D16RS1: Source output	FC5A-D32K3: Sink output FC5A-D32S3: Source output
Output Points and Common Lines		2 points in 1 common line	16 points in 2 common lines
Terminal Arrangement		See CPU Module Terminal Arrangement on pages 2-23 through 2-25.	
Rated Load Voltage		24V DC	
Operating Load Voltage Range		20.4 to 28.8V DC	
Rated Load Current		0.3A per output point	
Maximum Load Current		1A per common line	
Voltage Drop (ON Voltage)		1V maximum (voltage between COM and output terminals when output is on)	
Inrush Current		1A maximum	
Leakage Current		0.1 mA maximum	
Clamping Voltage		39V±1V	
Maximum Lamp Load		8W	
Inductive Load		L/R = 10 ms (28.8V DC, 1 Hz)	
External Current Draw		Sink output: 100 mA maximum, 24V DC (power voltage at the +V terminal) Source output: 100 mA maximum, 24V DC (power voltage at the –V terminal)	
Isolation		Between output terminal and internal circuit: Photocoupler isolated Between output terminals: Not isolated	
Connector on Mother Board		MC1.5/16-G-3.81BK (Phoenix Contact)	FL26A2MA (Oki Electric Cable)
Connector Insertion/Removal Durability		100 times minimum	
Output Delay	**Turn ON Time**	Q0 to Q1: 5 µs maximum	Q0 to Q2: 5 µs maximum Q3 to Q17 300 µs maximum
	Turn OFF Time	Q0 to Q1: 5 µs maximum	Q0 to Q2: 5 µs maximum Q3 to Q17 300 µs maximum

Output Internal Circuit

FC5A-D16RK1 and FC5A-D32K3 (Sink Output)



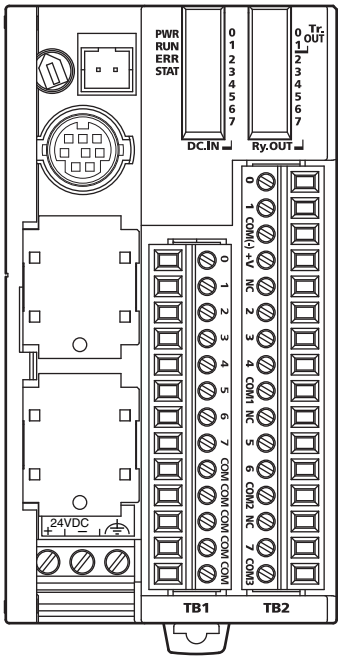
FC5A-D16RS1 and FC5A-D32S3 (Source Output)



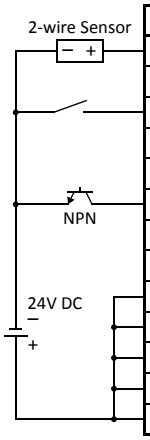
CPU Module Terminal Arrangement and I/O Wiring Diagrams (Slim Type)

FC5A-D16RK1 (16-I/O Relay and Transistor Sink High-speed Output Type CPU Module)

Applicable Terminal Blocks: **TB1 (Left Side)** **FC5A-PMT13P (supplied with the CPU module)**
TB2 (Right Side) **FC4A-PMTK16P (supplied with the CPU module)**



Source Input Wiring



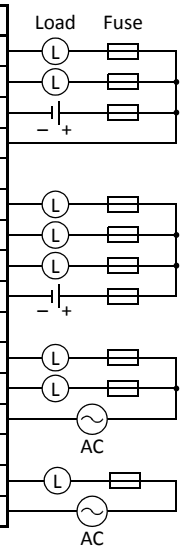
TB1

Terminal No.	Input
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	COM
10	COM
11	COM
12	COM
13	COM

Sink Output Wiring

TB2

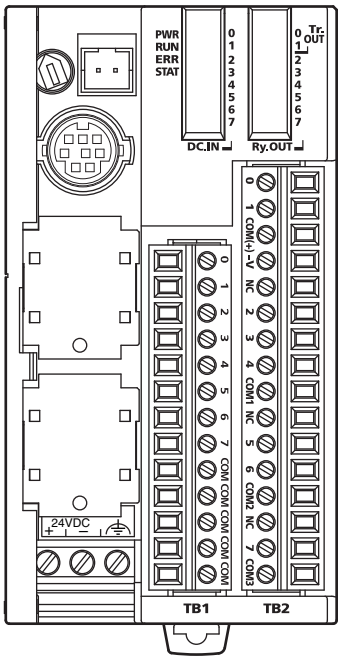
Terminal No.	Output
1	Q0
2	Q1
3	COM(–)
4	+V
5	NC
6	Q2
7	Q3
8	Q4
9	COM1
10	NC
11	Q5
12	Q6
13	COM2
14	NC
15	Q7
16	COM3



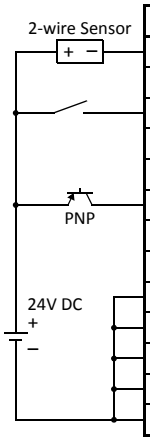
- Outputs Q0 and Q1 are transistor sink outputs; others are relay outputs.
- COM, COM(–), COM1, COM2, and COM3 terminals are *not* interconnected.
- COM terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19.

FC5A-D16RS1 (16-I/O Relay and Transistor Source High-speed Output Type CPU Module)

Applicable Terminal Blocks: **TB1 (Left Side)** **FC5A-PMT13P (supplied with the CPU module)**
TB2 (Right Side) **FC4A-PMTS16P (supplied with the CPU module)**



Sink Input Wiring



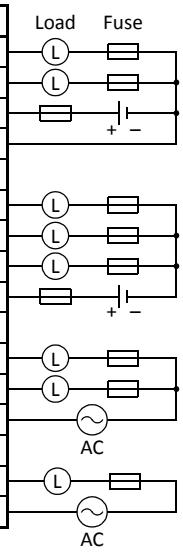
TB1

Terminal No.	Input
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	COM
10	COM
11	COM
12	COM
13	COM

Source Output Wiring

TB2

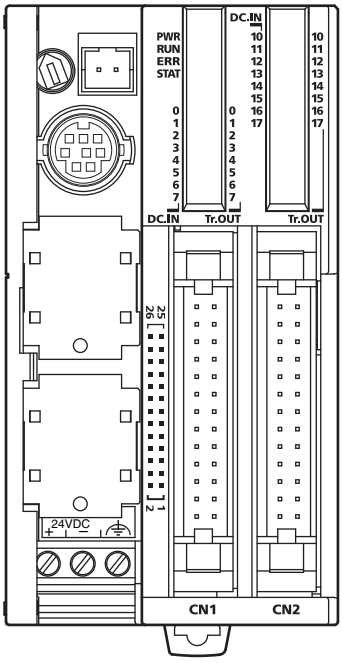
Terminal No.	Output
1	Q0
2	Q1
3	COM(+)
4	–V
5	NC
6	Q2
7	Q3
8	Q4
9	COM1
10	NC
11	Q5
12	Q6
13	COM2
14	NC
15	Q7
16	COM3



- Outputs Q0 and Q1 are transistor source outputs; others are relay outputs.
- COM, COM(+), COM1, COM2, and COM3 terminals are *not* interconnected.
- COM terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19.

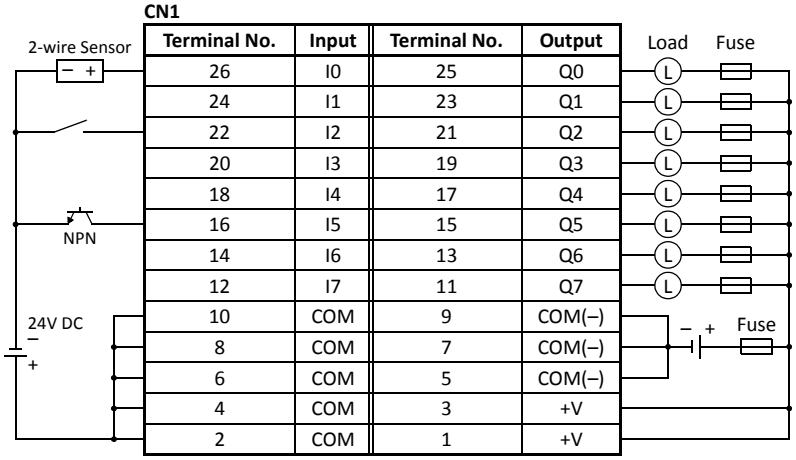
FC5A-D32K3 (32-I/O Transistor Sink Output Type CPU Module)

Applicable Connector: FC4A-PMC26P (*not* supplied with the CPU module)



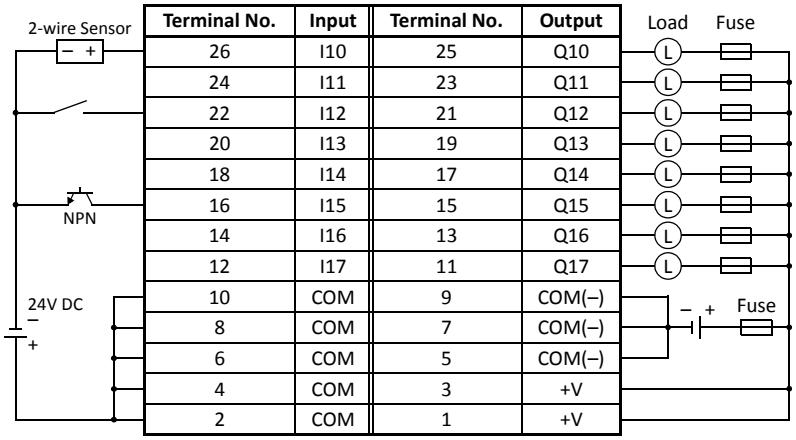
Source Input Wiring **Sink Output Wiring**

CN1



Terminal No.	Input	Terminal No.	Output
26	I0	25	Q0
24	I1	23	Q1
22	I2	21	Q2
20	I3	19	Q3
18	I4	17	Q4
16	I5	15	Q5
14	I6	13	Q6
12	I7	11	Q7
10	COM	9	COM(–)
8	COM	7	COM(–)
6	COM	5	COM(–)
4	COM	3	+V
2	COM	1	+V

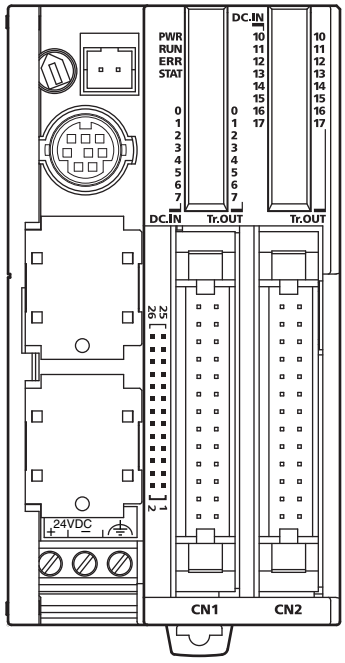
CN2



Terminal No.	Input	Terminal No.	Output
26	I10	25	Q10
24	I11	23	Q11
22	I12	21	Q12
20	I13	19	Q13
18	I14	17	Q14
16	I15	15	Q15
14	I16	13	Q16
12	I17	11	Q17
10	COM	9	COM(–)
8	COM	7	COM(–)
6	COM	5	COM(–)
4	COM	3	+V
2	COM	1	+V

- Terminals on CN1 and CN2 are *not* interconnected.
- COM and COM(–) terminals are *not* interconnected.
- COM terminals are interconnected.
- COM(–) terminals are interconnected.
- +V terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19.

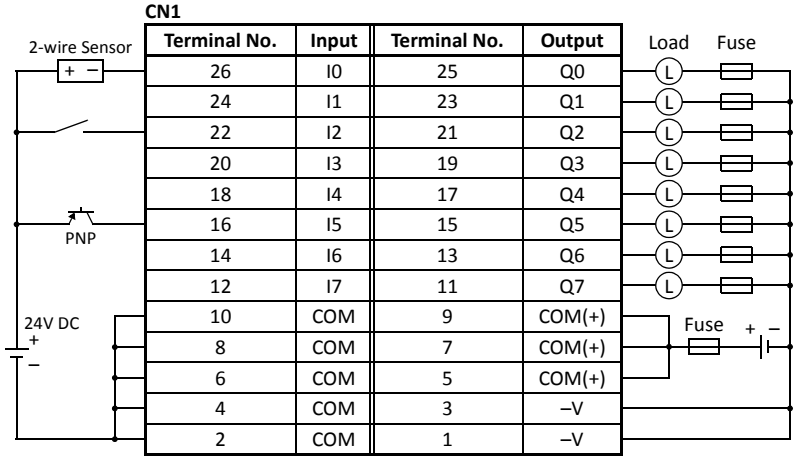
FC5A-D32S3 (32-I/O Transistor Source Output Type CPU Module)
Applicable Connector: FC4A-PMC26P (*not* supplied with the CPU module)



Sink Input Wiring **Source Output Wiring**

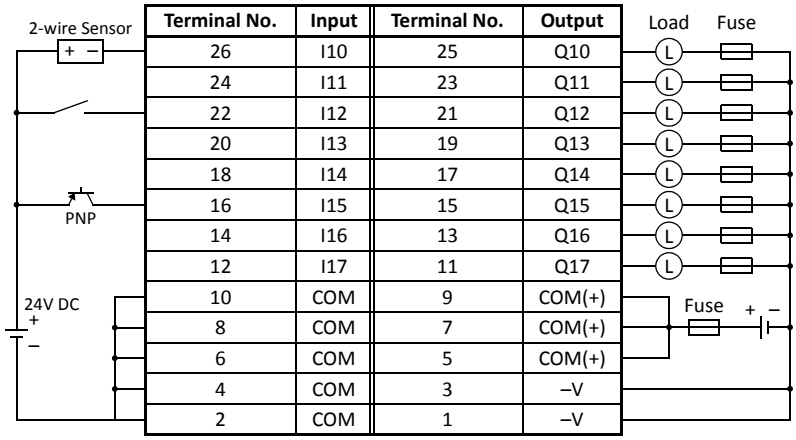
CN1

Terminal No.	Input	Terminal No.	Output
26	I0	25	Q0
24	I1	23	Q1
22	I2	21	Q2
20	I3	19	Q3
18	I4	17	Q4
16	I5	15	Q5
14	I6	13	Q6
12	I7	11	Q7
10	COM	9	COM(+)
8	COM	7	COM(+)
6	COM	5	COM(+)
4	COM	3	–V
2	COM	1	–V



CN2

Terminal No.	Input	Terminal No.	Output
26	I10	25	Q10
24	I11	23	Q11
22	I12	21	Q12
20	I13	19	Q13
18	I14	17	Q14
16	I15	15	Q15
14	I16	13	Q16
12	I17	11	Q17
10	COM	9	COM(+)
8	COM	7	COM(+)
6	COM	5	COM(+)
4	COM	3	–V
2	COM	1	–V



- Terminals on CN1 and CN2 are *not* interconnected.
- COM and COM(+) terminals are *not* interconnected.
- COM terminals are interconnected.
- COM(+) terminals are interconnected.
- –V terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19.

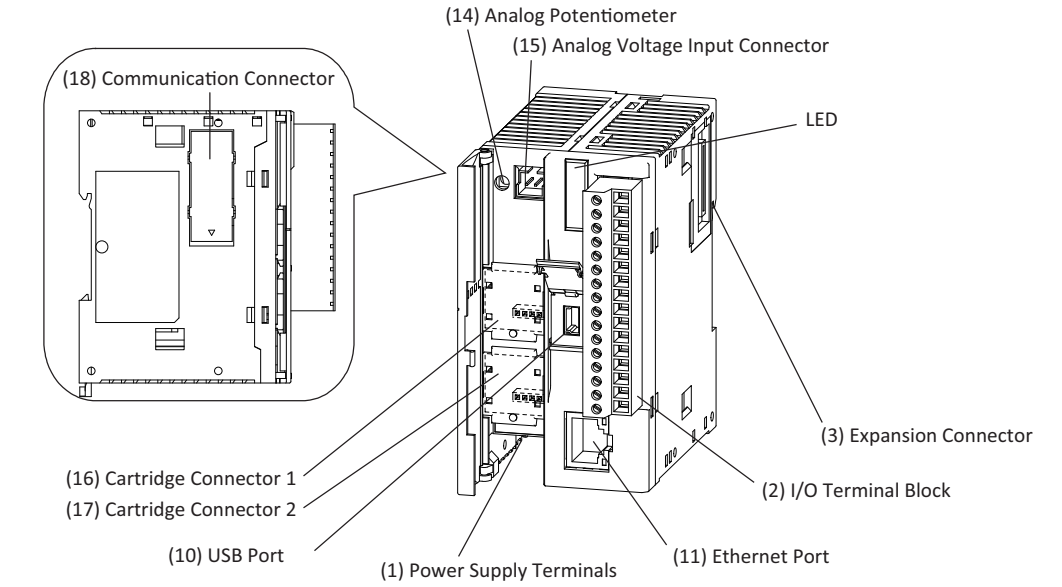
CPU Modules (Slim Type Web Server)

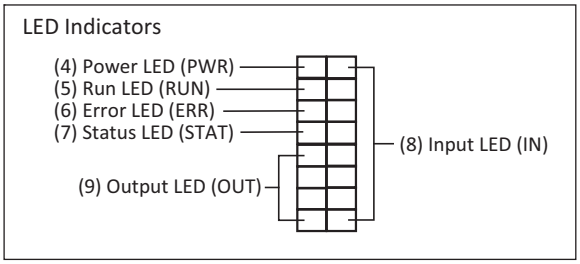
Slim type Web server CPU modules are available in 12-I/O type and have 8 input and 4 output terminals. Slim type Web server CPU module has built-in Ethernet port for maintenance communication, user communication, Modbus TCP communication, sending e-mail, and Web server. Slim type Web server CPU module also has built-in USB communication port for maintenance communication, and can mount an optional RS232C or RS485 communication module for 1:N computer link, user communication, data link communication, and Modbus ASCII/RTU communication. The HMI base module can also be mounted to install an optional HMI module and a communication adapter. Every slim type CPU module has two cartridge connectors to install an optional memory cartridge and a clock cartridge.

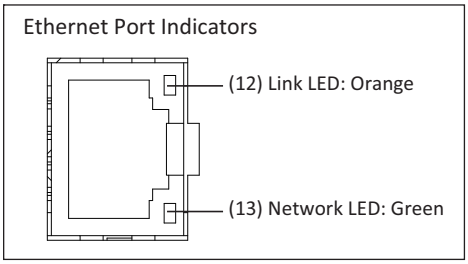
CPU Module Type Numbers (Slim Type Web Server)

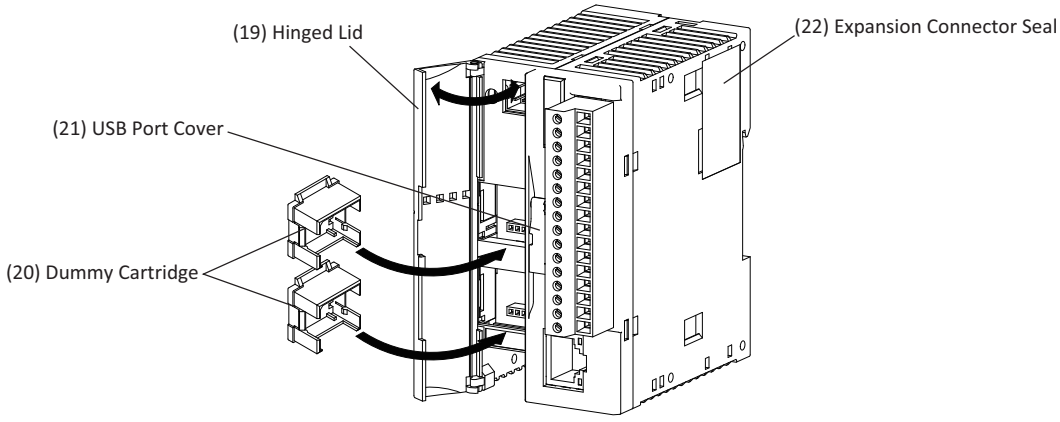
I/O Points	Output Type	Type No.
12 (8 in / 4 out)	Transistor Sink Output 0.3A	FC5A-D12K1E
	Transistor Source Output 0.3A	FC5A-D12S1E

Parts Description









(1) Power Supply Terminals
Connect power supply to these terminals. Power voltage 24V DC.

(2) I/O Terminal Block
For connecting input and output signals.

(3) Expansion Connector
For connecting digital and analog I/O modules.

(4) Power LED (PWR)
Turns on when power is supplied to the CPU module.

(5) Run LED (RUN)
Turns on when the CPU module is executing the user program.

(6) Error LED (ERR)
Turns on when an error occurs in the CPU module.

(7) Status LED (STAT)
The status LED can be turned on or off using the user program to indicate a specified status.

(8) Input LED (IN)
Turns on when a corresponding input is on.

(9) Output LED (OUT)
Turns on when a corresponding output is on.

(10) USB Port
For connecting a computer to download a user program and monitor the PLC operation on a computer using WindLDR. Programs written in WindLDR can be downloaded to the PLC.

(11) Ethernet Port
For connecting a LAN cable to communicate with PCs, PLCs, or any other network devices.

(12) Link LED: Orange
Turns on when the CPU module is connected to another network device using a LAN cable.

(13) Network LED: Green
Flashes when CPU module sends or receives data from the Ethernet port.

(14) Analog Potentiometer
Sets a value of 0 through 255 to a special data register. All slim type CPU modules have one potentiometer, which can be used to set a preset value for an analog timer.

(15) Analog Voltage Input Connector
For connecting an analog voltage source of 0 through 10V DC. The analog voltage is converted to a value of 0 through 255 and stored to a special data register.

(16) Cartridge Connector 1
For connecting an optional memory cartridge or clock cartridge.

(17) Cartridge Connector 2
For connecting an optional memory cartridge or clock cartridge.

(18) Communication Connector
For connecting an optional communication module or HMI base module. Remove the connector cover before connecting a module.

(19) Hinged Lid
Open the lid to gain access to the cartridge connectors 1 and 2, analog potentiometer, and analog voltage input connector.

(20) Dummy Cartridge
Remove the dummy cartridge when using an optional memory cartridge or clock cartridge.

(21) USB Port Cover
Open this cover to use the USB port.

(22) Expansion Connector Seal
Remove the expansion connector seal when connecting an expansion module.

General Specifications

Normal Operating Conditions

CPU Module	FC5A-D12K1E FC5A-D12S1E
Operating Temperature	0 to 55°C (operating ambient temperature)
Storage Temperature	–25 to +70°C
Relative Humidity	10 to 95% (non-condensing, operating and storage humidity)
Pollution Degree	2 (IEC 60664-1)
Degree of Protection	IP20 (IEC 60529)
Corrosion Immunity	Atmosphere free from corrosive gases
Altitude	Operation: 0 to 2,000m (0 to 6,565 feet) Transport: 0 to 3,000m (0 to 9,840 feet)
Vibration Resistance	When mounted on a DIN rail or panel surface: 5 to 8.4 Hz amplitude 3.5 mm, 8.4 to 150 Hz acceleration 9.8 m/s^2 (1G) 2 hours per axis on each of three mutually perpendicular axes (IEC 61131-2)
Shock Resistance	147 m/s^2 (15G), 11 ms duration, 3 shocks per axis on three mutually perpendicular axes (IEC 61131-2)
ESD Immunity	Contact discharge: ±4 kV, Air discharge: ±8 kV (IEC 61000-4-2)
Weight	200g

Power Supply

Rated Power Voltage	24V DC	
Allowable Voltage Range	20.4 to 26.4V DC (including ripple)	
Maximum Input Current	700 mA (26.4V DC)	
Maximum Power Consumption (Note 1, 2)	CPU module + 7 I/O modules + expansion module + 8 I/O modules	
	19W (26.4V DC)	
Allowable Momentary Power Interruption	10 ms (at 24V DC)	
Dielectric Strength	Between power and ⏚ terminals: Between I/O and ⏚ terminals:	500V AC, 1 minute 500V AC, 1 minute
Insulation Resistance	Between power and ⏚ terminals: Between I/O and ⏚ terminals:	10 MΩ minimum (500V DC megger) 10 MΩ minimum (500V DC megger)
Noise Resistance	DC power terminals: I/O terminals (coupling clamp):	1.0 kV, 50 ns to 1 µs 1.5 kV, 50 ns to 1 µs
Inrush Current	50A maximum (24V DC)	
Grounding Wire	UL1015 AWG22, UL1007 AWG18	
Power Supply Wire	UL1015 AWG22, UL1007 AWG18	
Effect of Improper Power Supply Connection	Reverse polarity: Improper voltage or frequency: Improper lead connection:	No operation, no damage Permanent damage may be caused Permanent damage may be caused

Note 1: Among relay output modules connected to the CPU module, a maximum of 54 points can be turned on simultaneously. Among relay outputs connected beyond the expansion module, a maximum of 54 points can be turned on simultaneously. Relay outputs exceeding these limits may not turn on correctly.

Note 2: Maximum power consumption for individual CPU module is 3.0W (125 mA at 24V DC).

Function Specifications

CPU Module Specifications

CPU Module		FC5A-D12K1E FC5A-D12S1E	
Program Capacity		62,400/127,800 bytes (10,400/21,300 steps) (Note 1)	
Expandable I/O Modules		7 modules + additional 8 modules using the expansion interface module	
I/O Points	Input	8	Expansion: 224 (Note 2) Additional: 256 (Note 3)
	Output	4	
User Program Storage		FROM (10,000 rewriting life)	
RAM Backup	Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged	
	Backup Data	Internal relay, shift register, counter, data register, expansion data register	
	Battery	Lithium secondary battery	
	Charging Time	Approx. 15 hours for charging from 0% to 90% of full charge	
	Battery Life	5 years in cycles of 9-hour charging and 15-hour discharging	
	Replaceability	Not possible to replace battery	
Control System		Stored program system	
Instruction Words		42 basic 152 advanced	
Processing Time	Basic instruction	83 µs (1000 steps) See page A-1.	
	END processing	0.35 ms (not including expansion I/O service, clock function processing, data link processing, interrupt processing, USB communication processing, and Ethernet communication processing) See page A-5.	
Internal Relay		2,048	
Shift Register		256	
Timer		256 (1-sec, 100-ms, 10-ms, 1-ms)	
Counter		256 (adding, dual pulse reversible, up/down selection reversible)	
Data Register		2,000	
Expansion Data Register		6,000	
Extra Data Register		40,000	
Input Filter		Without filter, 3 to 15 ms (selectable in increments of 1 ms)	
Catch Input Interrupt Input		Four inputs (I2 through I5) can be designated as catch inputs or interrupt inputs I2 and I5: Minimum turn on pulse width: 40 µs maximum Minimum turn off pulse width: 150 µs maximum I3 and I4: Minimum turn on pulse width: 5 µs maximum Minimum turn off pulse width: 5 µs maximum	
Self-diagnostic Function		Power failure, watchdog timer, data link connection, user program sum check (FROM, external EEPROM), timer/counter preset value sum check, user program RAM sum check, keep data, user program syntax, user program writing, CPU module, clock IC, I/O bus initialize, user program execution, memory cartridge program transfer	
Start/Stop Method		Turning power on and off Start/stop command in WindLDR Turning start control special internal relay M8000 on and off Turning designated stop or reset input off and on	
High-speed Counter		Total 4 points Single/two-phase selectable: 100 kHz (2 points) Single-phase: 100 kHz (2 points) Counting range: 0 to 4,294,967,295 (32 bits) Operation mode: Rotary encoder mode and adding counter mode	
Analog Potentiometer		1 point	
		Data range: 0 to 255	

Analog Voltage Input	Quantity: Input voltage range: Input impedance: Data range:	1 point 0 to 10V DC Approx. 100 kΩ 0 to 255 (8 bits)
Pulse Output	3 points	
	Maximum frequency:	100 kHz
Communication Port	Communication connector for port 2	
Cartridge Connector	2 points for connecting a memory cartridge (32KB, 64KB, or 128KB) and a clock cartridge	

Note 1: Select program capacity of 62,400 bytes or 127,800 bytes. When 127,800 bytes is selected, the run-time program download cannot be used.

Note 2: The maximum number of outputs that can be turned on simultaneously is 54.

Note 3: Among the additional I/O modules, the maximum number of outputs that can be turned on simultaneously is 54.

System Statuses at Stop, Reset, and Restart

Mode	Output	Internal Relay, Shift Register, Counter, Data Register, Expansion DR, Extra DR		Timer Current Value
		Keep Type	Clear Type	
Run	Operating	Operating	Operating	Operating
Stop (Stop input ON)	OFF	Unchanged	Unchanged	Unchanged
Reset (Reset input ON)	OFF	OFF/Reset to zero	OFF/Reset to zero	Reset to zero
Restart	Unchanged	Unchanged	OFF/Reset to zero	Reset to preset

Note: All expansion data registers are keep types.

Communication Function

CPU Module		FC5A-D12K1E FC5A-D12S1E
USB	**Function**	Maintenance Communication (Note 1)
	Cable	USB cable from the third party (A connector to Mini-B connector) (Note 2)
	Isolation between Internal Circuit and Communication Port	Not isolated
	USB Type	USB Mini-B
	USB Standard	USB 2.0
Ethernet	**Electrical Characteristics**	IEEE 802.3 compliant
	Transmission Speed	10BASE-T, 100BASE-TX
	Function	Maintenance communication, user communication, Modbus TCP communication, e-mail, Web server
	Recommended Cable	CAT. 5 STP
	Isolation between Internal Circuit and Communication Port	Pulse transformer isolated
	User Web Data Storage	FROM
	User Web Data Capacity	1MB
Port 2 (Optional) (Note 3)		Possible

Note 1: To use the USB port, USB driver must be installed on the PC. For the procedure to install the driver, see Appendix of the FC5A user's manual Web server CPU module volume.

Note 2: A USB maintenance cable (HG9Z-XCM42) and a USB Mini-B extension cable (HG9Z-XCE21) are available as optional accessories. For instructions on using the USB extension cable, refer to Chapter b_3.fm "Securing USB Extension Cable Using Cable Tie" on page 3-5.

Note 3: Communication modules that can be connected to port 2 are listed in the following table.

Memory Cartridge (Option)

Memory Type	EEPROM
Accessible Memory Capacity	32 KB, 64 KB, 128 KB The maximum program capacity depends on the CPU module. When using the 32 KB memory cartridge on the slim type CPU module, the maximum program capacity is limited to 30,000 bytes.
Hardware for Storing Data	CPU module
Software for Storing Data	WindLDR
Quantity of Stored Programs	One user program can be stored on one memory cartridge. (Note 1)
Program Execution Priority	When a memory cartridge is installed, the user program on the memory cartridge is executed. User programs can be downloaded from the memory cartridge to the CPU module. User programs can also be uploaded to the memory cartridge from the CPU module.

Note 1: User Web data is not stored.

Clock Cartridge (Option)

Accuracy	±30 sec/month (typical) at 25°C
Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged
Battery	Lithium secondary battery
Charging Time	Approx. 10 hours for charging from 0% to 90% of full charge
Battery Life	Approx. 100 recharge cycles after discharging down to 10% of full charge
Replaceability	Not possible to replace battery

Communication Function

Communication Port	**Port 2**		
Communication Adapter	**FC4A-PC1**	**FC4A-PC2**	**FC4A-PC3**
Communication Module	**FC4A-HPC1**	**FC4A-HPC2**	**FC4A-HPC3**
Standards	EIA RS232C	EIA RS485	EIA RS485
Maximum Baud Rate	115,200 bps	115,200 bps	115,200 bps
Maintenance Communication (Computer Link)	Possible	Possible	Possible
User Communication	Possible	Possible	Possible
Modem Communication	—	—	—
Data Link Communication	—	Possible (31 slaves max.) (Note 1)	Possible (31 slaves max.) (Note 1)
Modbus Communication	Possible (Note 2)	Possible	Possible
Maximum Cable Length	Special cable (Note 3)	Special cable (Note 3)	200m (Note 4)
Isolation between Internal Circuit and Communication Port	Not isolated	Not isolated	Not isolated

Note 1: Maximum baud rate when using data link communication is 57,600 bps.

Note 2: 1:1 Modbus communication only

Note 3: For special cables, see page A-12.

Note 4: Recommended cable for RS485: Twisted-pair shielded cable with a minimum core wire of 0.3 mm^2.
Conductor resistance 85 Ω/km maximum, shield resistance 20 Ω/km maximum.

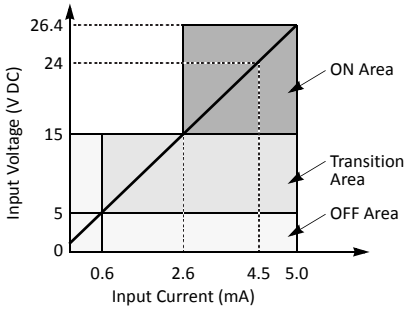
DC Input Specifications (Slim Type Web Server)

CPU Module	FC5A-D12K1E FC5A-D12S1E
Input Points and Common Lines	8 points in 1 common line
Terminal Arrangement	See CPU Module Terminal Arrangement on page 2-34.
Rated Input Voltage	24V DC sink/source input signal
Input Voltage Range	20.4 to 28.8V DC
Rated Input Current	I0, I1, I3, I4, I6, I7: 4.5 mA/point (24V DC) I2, I5: 7 mA/point (24V DC)
Input Impedance	I0, I1, I3, I4, I6, I7: 4.9 kΩ I2, I5: 3.4 kΩ
Turn ON Time	I0, I1, I3, I4, I6, I7: 5 µs + filter value I2, I5: 35 µs + filter value
Turn OFF Time	I0, I1, I3, I4, I6, I7: 5 µs + filter value I2, I5: 150 µs + filter value
Isolation	Between input terminals: Not isolated Internal circuit: Photocoupler isolated
Input Type	Type 1 (IEC 61131-2)
External Load for I/O Interconnection	Not needed
Signal Determination Method	Static
Effect of Improper Input Connection	Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.
Cable Length	3m (9.84 ft.) in compliance with electromagnetic immunity
Connector on Mother Board	MC1.5/13-G-3.81BK (Phoenix Contact)
Connector Insertion/Removal Durability	100 times minimum

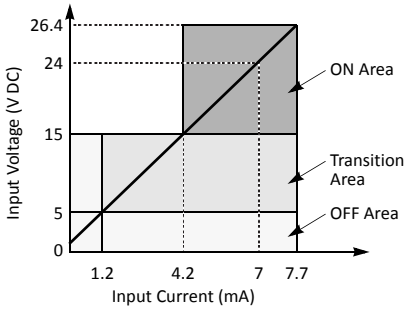
Input Operating Range

The input operating range of the Type 1 (IEC 61131-2) input module is shown below:

Inputs I0, I1, I3, I4, I6, and I7

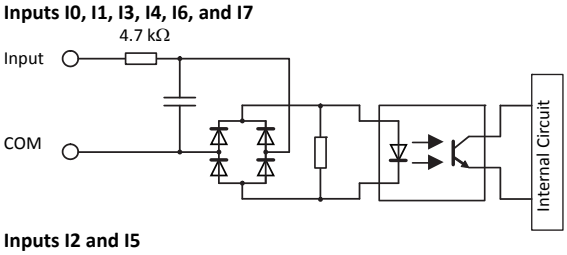


Inputs I2 and I5

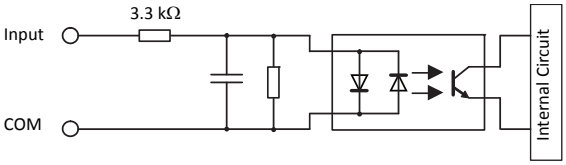


Input Internal Circuit

Inputs I0, I1, I3, I4, I6, and I7

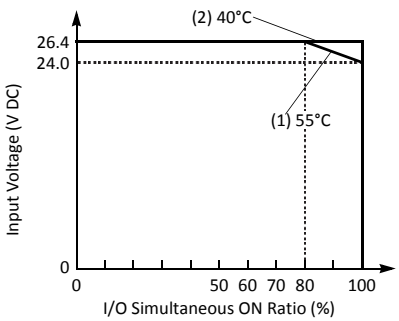


Inputs I2 and I5



I/O Usage Limits

When using the FC5A-D12K1E/S1E at an ambient temperature of 55°C in the normal mounting direction, limit the inputs and outputs, respectively, which turn on simultaneously on each connector along line (1).



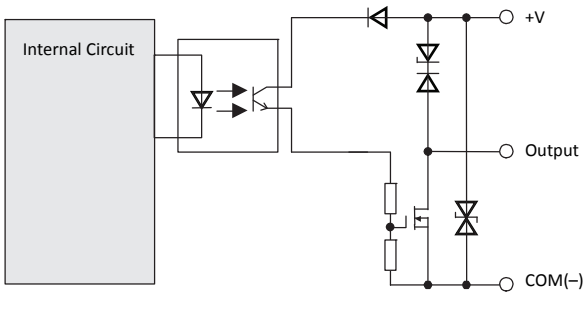
When using at 40°C, all I/Os on every slim type CPU module can be turned on simultaneously at 26.4V DC as indicated with line (2)

Transistor Sink and Source Output Specifications (Slim Type Web Server)

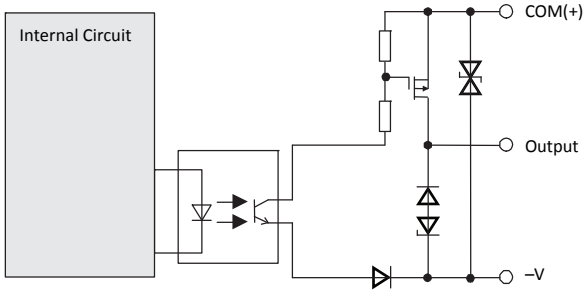
CPU Module		FC5A-D12K1E FC5A-D12S1E
Output Type		FC5A-D12K1E: Sink output FC5A-D12S1E: Source output
Output Points and Common Lines		4 points in 1 common line
Terminal Arrangement		See CPU Module Terminal Arrangement on page 2-34.
Rated Load Voltage		24V DC
Operating Load Voltage Range		20.4 to 28.8V DC
Rated Load Current		0.3A per output point
Maximum Load Current		1A per common line
Voltage Drop (ON Voltage)		1V maximum (voltage between COM and output terminals when output is on)
Inrush Current		1A maximum
Leakage Current		0.1 mA maximum
Clamping Voltage		39V±1V
Maximum Lamp Load		8W
Inductive Load		L/R = 10 ms (28.8V DC, 1 Hz)
External Current Draw		Sink output: 100 mA maximum, 24V DC (power voltage at the +V terminal) Source output: 100 mA maximum, 24V DC (power voltage at the –V terminal)
Isolation		Between output terminal and internal circuit: Photocoupler isolated Between output terminals: Not isolated
Connector on Mother Board		MC1.5/16-G-3.81BK (Phoenix Contact)
Connector Insertion/Removal Durability		100 times minimum
Output Delay	**Turn ON Time**	Q0 to Q2: 5 µs maximum Q3: 300 µs maximum
	Turn OFF Time	Q0 to Q2: 5 µs maximum Q3: 300 µs maximum

Output Internal Circuit

FC5A-D12K1E (Sink Output)



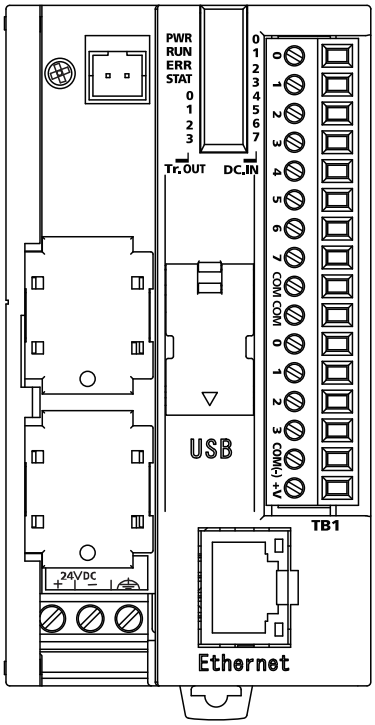
FC5A-D12S1E (Source Output)



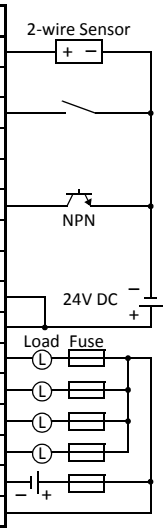
CPU Module Terminal Arrangement and I/O Wiring Diagrams (Slim Type Web Server)

FC5A-D12K1E (12-I/O Transistor Sink High-speed Output Type CPU Module)

Applicable Terminal Blocks: FC5A-PMTK16EP (supplied with the CPU module)



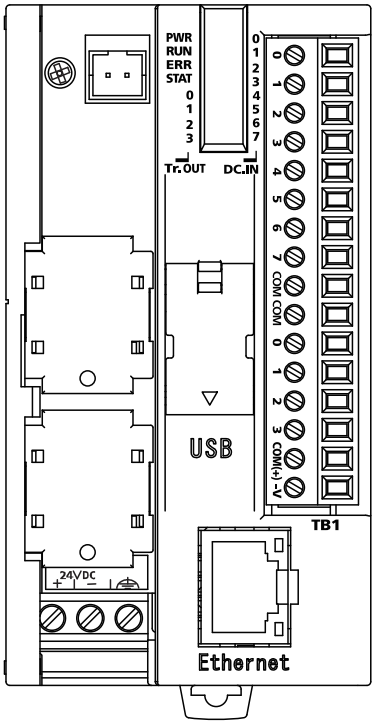
Terminal No.	Input/Output
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	COM
10	COM
11	Q0
12	Q1
13	Q2
14	Q3
15	COM(-)
16	+V



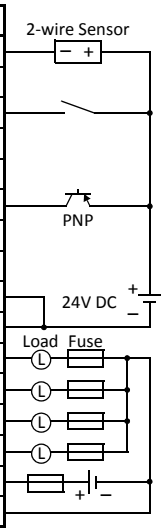
- Outputs Q0 to Q3 are transistor sink outputs.
- COM and COM(–) terminals are *not* interconnected.
- COM terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19 (Basic Vol.).

FC5A-D12S1E (12-I/O Transistor Source High-speed Output Type CPU Module)

Applicable Terminal Blocks: FC5A-PMTS16EP (supplied with the CPU module)



Terminal No.	Input/Output
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	COM
10	COM
11	Q0
12	Q1
13	Q2
14	Q3
15	COM(+)
16	-V



- Outputs Q0 to Q3 are transistor source outputs.
- COM and COM(+) terminals are *not* interconnected.
- COM terminals are interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 through 3-19 (Basic Vol.).

Input Modules

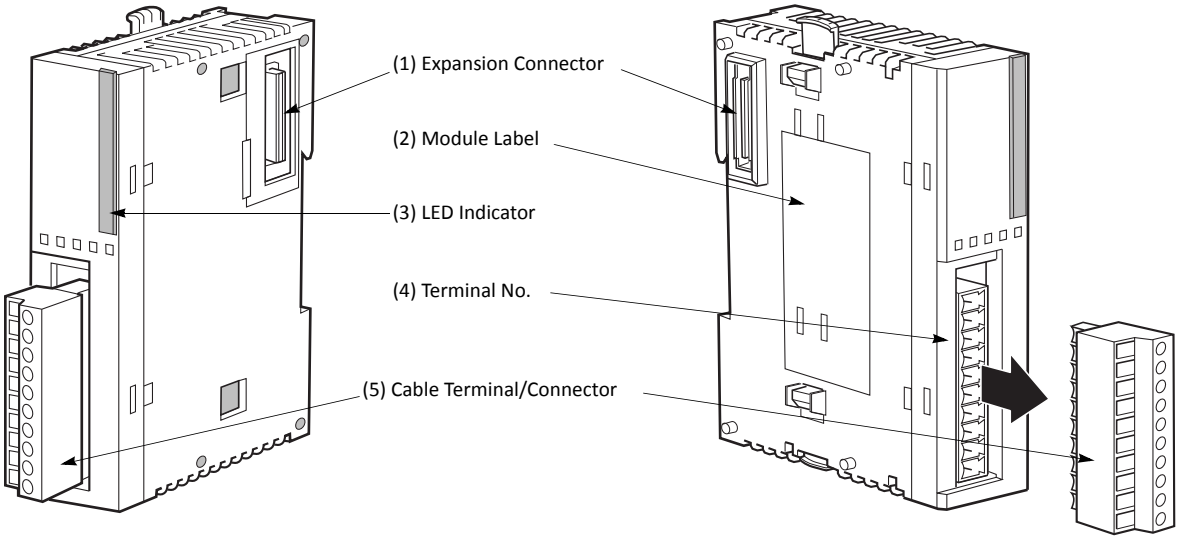
Digital input modules are available in 8-, 16-, and 32-point DC input modules and an 8-point AC input module with a screw terminal block or plug-in connector for input wiring. All DC input modules accept both sink and source DC input signals.

The input modules can be connected to the all-in-one 24-I/O type CPU module and all slim type CPU modules to expand input terminals. The all-in-one 10- and 16-I/O type CPU modules cannot connect input modules.

Input Module Type Numbers

Module Name	8-point DC Input	16-point DC Input	32-point DC Input	8-point AC Input
Screw Terminal	FC4A-N08B1	FC4A-N16B1	—	FC4A-N08A11
Connector	—	FC4A-N16B3	FC4A-N32B3	—

Parts Description



The above figures illustrate the 8-point DC input module.

(1) Expansion Connector	Connects to the CPU and other I/O modules. (The all-in-one 10- and 16-I/O type CPU modules cannot be connected.)
(2) Module Label	Indicates the input module Type No. and specifications.
(3) LED Indicator	Turns on when a corresponding input is on.
(4) Terminal No.	Indicates terminal numbers.
(5) Cable Terminal/Connector	Five different terminal/connector styles are available for wiring.

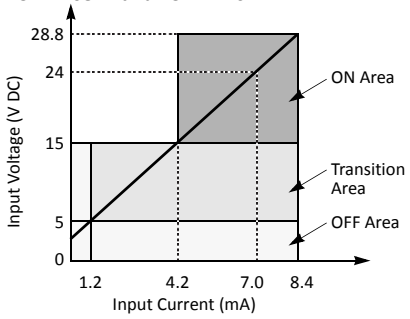
DC Input Module Specifications

Type No.		FC4A-N08B1	FC4A-N16B1	FC4A-N16B3	FC4A-N32B3
Input Points and Common Lines		8 points in 1 common line	16 points in 1 common line	16 points in 1 common line	32 points in 2 common lines
Terminal Arrangement		See Input Module Terminal Arrangement on pages 2-38 through 2-40.			
Rated Input Voltage		24V DC sink/source input signal			
Input Voltage Range		20.4 to 28.8V DC			
Rated Input Current		7 mA/point (24V DC)		5 mA/point (24V DC)	
Input Impedance		3.4 kΩ		4.4 kΩ	
Turn ON Time (24V DC)		4 ms			
Turn OFF Time (24V DC)		4 ms			
Isolation		Between input terminals: Not isolated Internal circuit: Photocoupler isolated			
External Load for I/O Interconnection		Not needed			
Signal Determination Method		Static			
Effect of Improper Input Connection		Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.			
Cable Length		3m (9.84 ft.) in compliance with electromagnetic immunity			
Connector on Mother Board		MC1.5/10-G-3.81BK (Phoenix Contact)		FL20A2MA (Oki Electric Cable)	
Connector Insertion/Removal Durability		100 times minimum			
Internal Current Draw	All Inputs ON	25 mA (5V DC) 0 mA (24V DC)	40 mA (5V DC) 0 mA (24V DC)	35 mA (5V DC) 0 mA (24V DC)	65 mA (5V DC) 0 mA (24V DC)
	All Inputs OFF	5 mA (5V DC) 0 mA (24V DC)	5 mA (5V DC) 0 mA (24V DC)	5 mA (5V DC) 0 mA (24V DC)	10 mA (5V DC) 0 mA (24V DC)
Weight		85g	100g	65g	100g

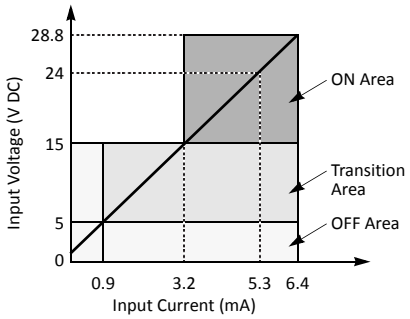
Input Operating Range

The input operating range of the Type 1 (IEC 61131-2) input module is shown below:

FC4A-N08B1 and FC4A-N16B1

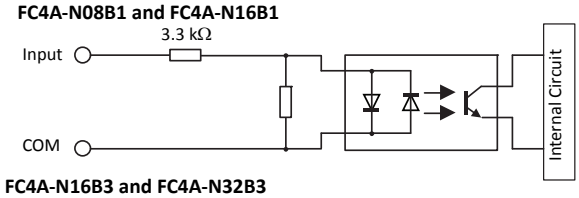


FC4A-N16B3 and FC4A-N32B3

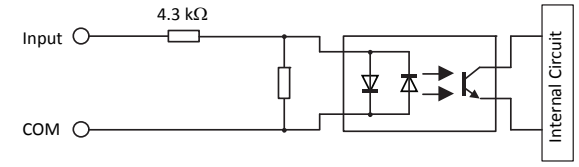


Input Internal Circuit

FC4A-N08B1 and FC4A-N16B1



FC4A-N16B3 and FC4A-N32B3

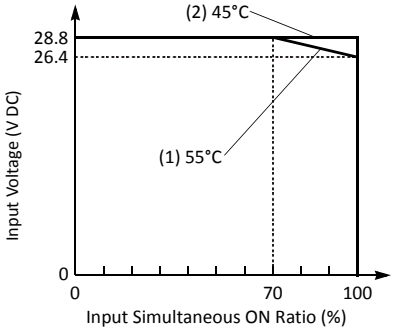


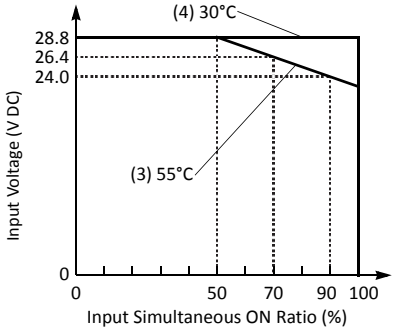
Input Usage Limits

When using the FC4A-N16B1 at 55°C in the normal mounting direction, limit the inputs which turn on simultaneously along line (1). At 45°C, all inputs can be turned on simultaneously at 28.8V DC as indicated with line (2).

When using the FC4A-N16B3 or -N32B3 at 55°C, limit the inputs which turn on simultaneously on each connector along line (3). At 30°C, all inputs can be turned on simultaneously at 28.8V DC as indicated with line (4).

When using the FC4A-N08B1, all inputs can be turned on simultaneously at 55°C, input voltage 28.8V DC.





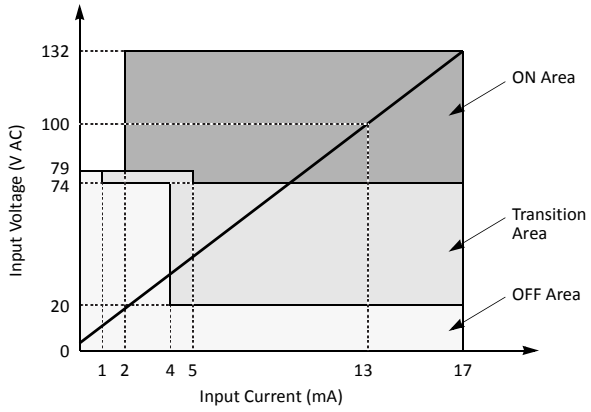
AC Input Module Specifications

Type No.		FC4A-N08A11
Input Points and Common Lines		8 points in 2 common lines
Terminal Arrangement		See Input Module Terminal Arrangement on page 2-41.
Rated Input Voltage		100 to 120V AC (50/60 Hz)
Input Voltage Range		85 to 132V AC
Rated Input Current		17 mA/point (120V AC, 60 Hz)
Input Type		AC input; Type 1, 2 (IEC 61131)
Input Impedance		0.8 kΩ (60 Hz)
Turn ON Time		25 ms
Turn OFF Time		30 ms
Isolation		Between input terminals in the same common: Not isolated Between input terminals in different commons: Isolated Between input terminals and internal circuits: Photocoupler isolated
External Load for I/O Interconnection		Not needed
Signal Determination Method		Static
Effect of Improper Input Connection		If any input exceeding the rated value is applied, permanent damage may be caused.
Connector on Mother Board		MC1.5/11-G-3.81BK (Phoenix Contact)
Connector Insertion/Removal Durability		100 times minimum
Internal Current Draw	All Inputs ON	60 mA (5V DC) 0 mA (24V DC)
	All Inputs OFF	30 mA (5V DC) 0 mA (24V DC)
Weight		80g

Input Operating Range

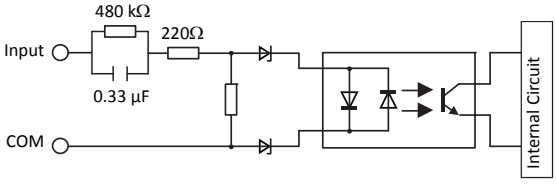
The input operating range of the Type 1 and 2 (IEC 61131-2) input module is shown below:

FC4A-N08A11



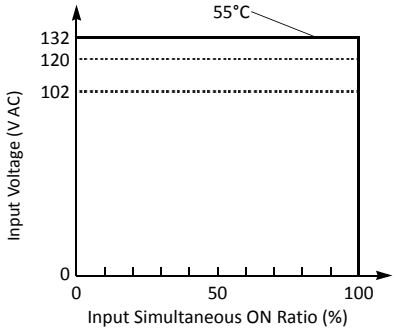
Input Internal Circuit

FC4A-N08A11



Input Usage Limits

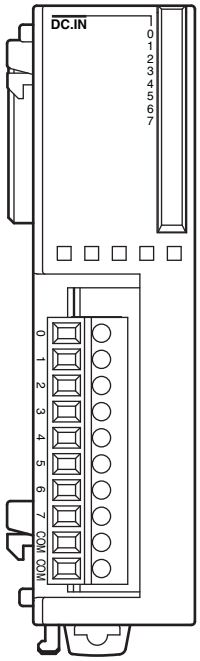
When using the FC4A-N08A11, all inputs can be turned on simultaneously at 55°C, input voltage 132V AC.



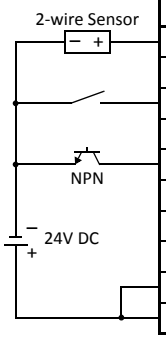
DC Input Module Terminal Arrangement and Wiring Diagrams

FC4A-N08B1 (8-point DC Input Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT10P (supplied with the input module)

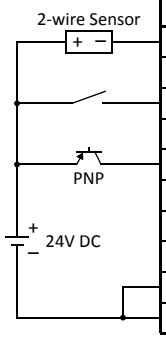


Source Input Wiring



Terminal No.	Input
0	I0
1	I1
2	I2
3	I3
4	I4
5	I5
6	I6
7	I7
COM	COM
COM	COM

Sink Input Wiring

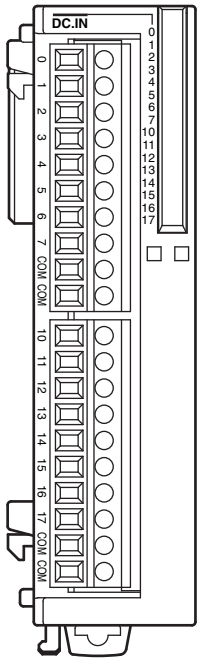


Terminal No.	Input
0	I0
1	I1
2	I2
3	I3
4	I4
5	I5
6	I6
7	I7
COM	COM
COM	COM

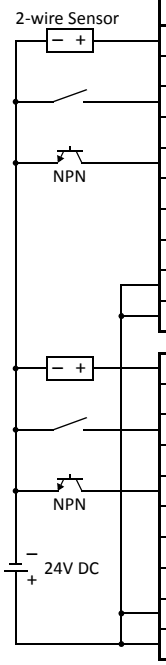
- Two COM terminals are interconnected.
- For input wiring precautions, see page 3-15.

FC4A-N16B1 (16-point DC Input Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT10P (supplied with the input module)

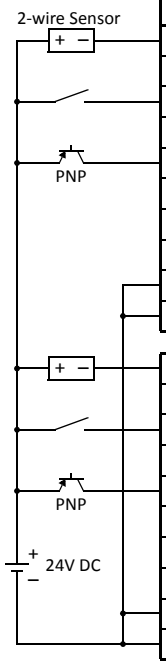


Source Input Wiring



Terminal No.	Input
0	I0
1	I1
2	I2
3	I3
4	I4
5	I5
6	I6
7	I7
COM	COM
COM	COM
10	I10
11	I11
12	I12
13	I13
14	I14
15	I15
16	I16
17	I17
COM	COM
COM	COM

Sink Input Wiring

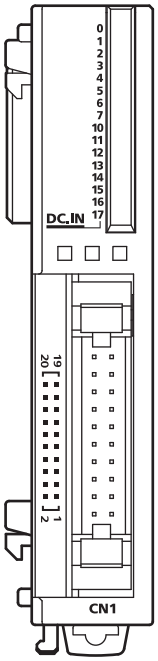


Terminal No.	Input
0	I0
1	I1
2	I2
3	I3
4	I4
5	I5
6	I6
7	I7
COM	COM
COM	COM
10	I10
11	I11
12	I12
13	I13
14	I14
15	I15
16	I16
17	I17
COM	COM
COM	COM

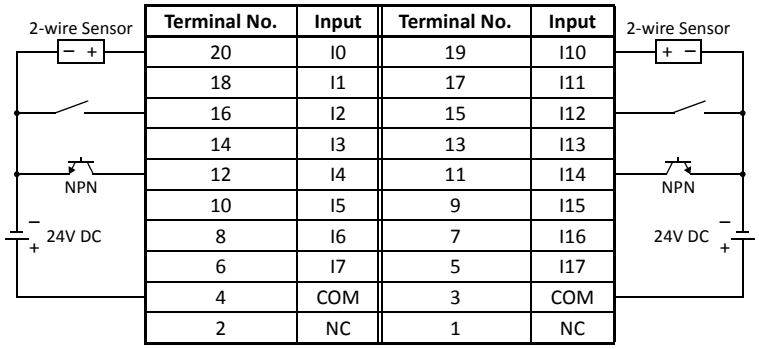
- Four COM terminals are interconnected.
- For input wiring precautions, see page 3-15.

FC4A-N16B3 (16-point DC Input Module) — Connector Type

Applicable Connector: FC4A-PMC20P (*not* supplied with the input module)

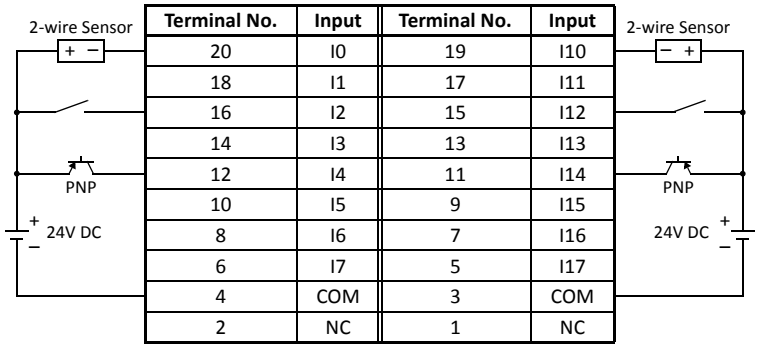


Source Input Wiring



Terminal No.	Input	Terminal No.	Input
20	I0	19	I10
18	I1	17	I11
16	I2	15	I12
14	I3	13	I13
12	I4	11	I14
10	I5	9	I15
8	I6	7	I16
6	I7	5	I17
4	COM	3	COM
2	NC	1	NC

Sink Input Wiring

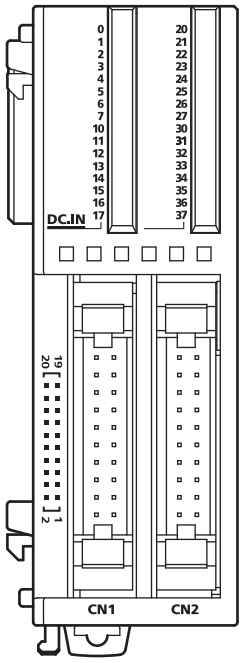


Terminal No.	Input	Terminal No.	Input
20	I0	19	I10
18	I1	17	I11
16	I2	15	I12
14	I3	13	I13
12	I4	11	I14
10	I5	9	I15
8	I6	7	I16
6	I7	5	I17
4	COM	3	COM
2	NC	1	NC

- Two COM terminals are interconnected.
- For input wiring precautions, see page 3-15.

FC4A-N32B3 (32-point DC Input Module) — Connector Type

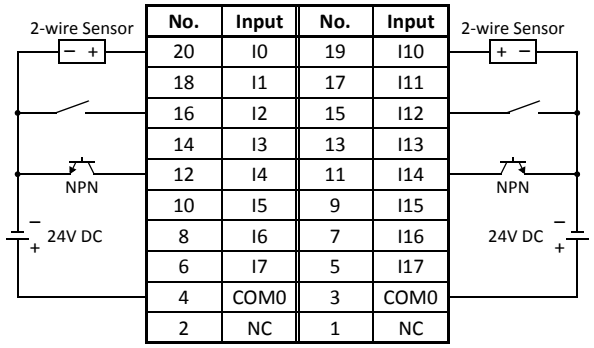
Applicable Connector: FC4A-PMC20P (*not* supplied with the input module)



- COM0 terminals are interconnected.
- COM1 terminals are interconnected.
- COM0 and COM1 terminals are *not* interconnected.
- For input wiring precautions, see page 3-15.

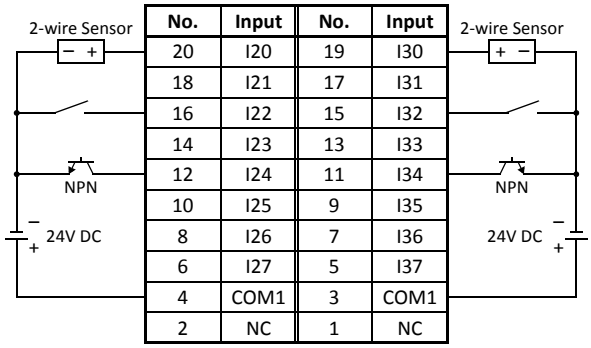
Source Input Wiring

CN1



No.	Input	No.	Input
20	I0	19	I10
18	I1	17	I11
16	I2	15	I12
14	I3	13	I13
12	I4	11	I14
10	I5	9	I15
8	I6	7	I16
6	I7	5	I17
4	COM0	3	COM0
2	NC	1	NC

CN2



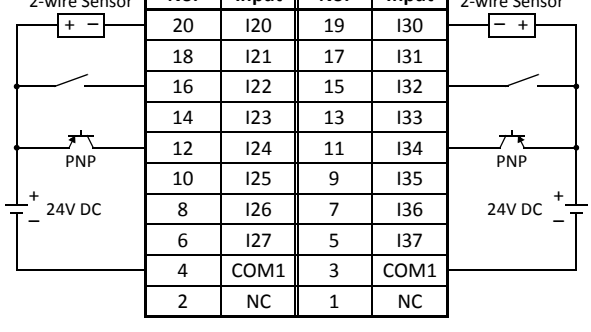
No.	Input	No.	Input
20	I20	19	I30
18	I21	17	I31
16	I22	15	I32
14	I23	13	I33
12	I24	11	I34
10	I25	9	I35
8	I26	7	I36
6	I27	5	I37
4	COM1	3	COM1
2	NC	1	NC

Sink Input Wiring

CN1

No.	Input	No.	Input
20	I0	19	I10
18	I1	17	I11
16	I2	15	I12
14	I3	13	I13
12	I4	11	I14
10	I5	9	I15
8	I6	7	I16
6	I7	5	I17
4	COM0	3	COM0
2	NC	1	NC

CN2

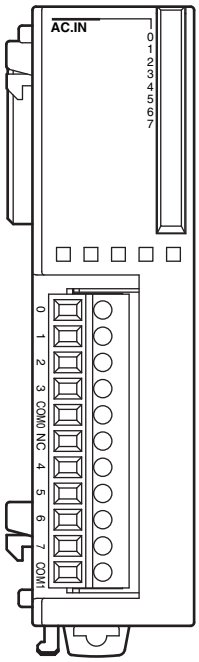


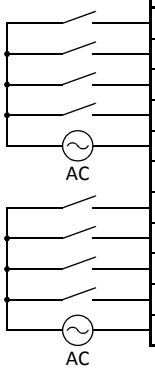
No.	Input	No.	Input
20	I20	19	I30
18	I21	17	I31
16	I22	15	I32
14	I23	13	I33
12	I24	11	I34
10	I25	9	I35
8	I26	7	I36
6	I27	5	I37
4	COM1	3	COM1
2	NC	1	NC

AC Input Module Terminal Arrangement and Wiring Diagrams

FC4A-N08A11 (8-point AC Input Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the input module)





Terminal No.	Output
0	I0
1	I1
2	I2
3	I3
COM0	COM0
NC	NC
4	I4
5	I5
6	I6
7	I7
COM1	COM1

- Two COM terminals are *not* interconnected.
- For input wiring precautions, see page 3-15.
- Do not connect an external load to the input terminals.

Output Modules

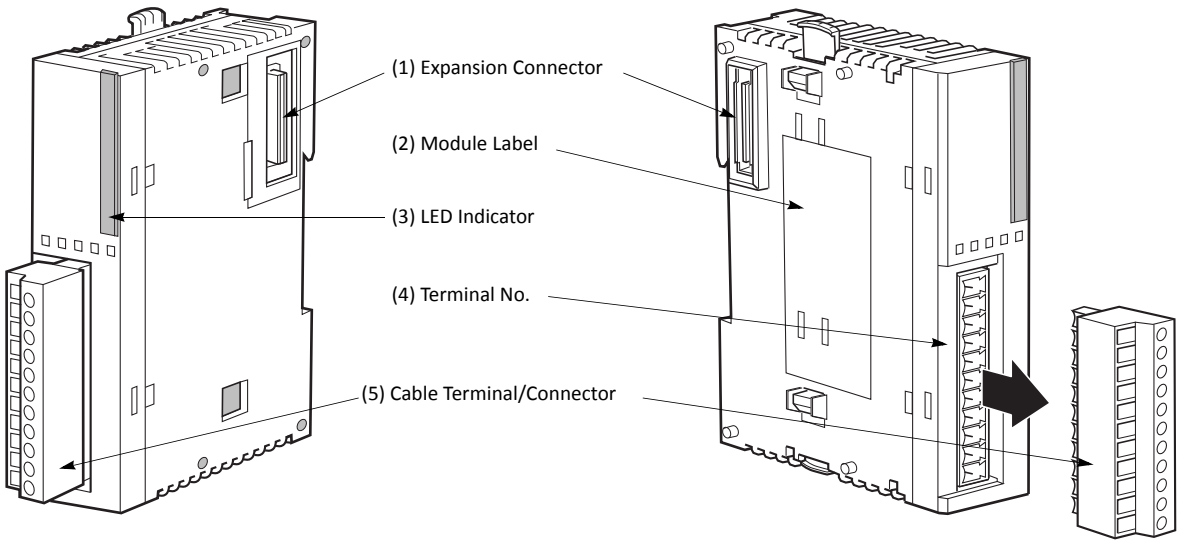
Digital output modules are available in 8- and 16-point relay output modules, 8-, 16- and 32-point transistor sink output modules, and 8-, 16- and 32-point transistor source output modules with a screw terminal block or plug-in connector for output wiring.

The output modules can be connected to the all-in-one 24-I/O type CPU module and all slim type CPU modules to expand output terminals. The all-in-one 10- and 16-I/O type CPU modules cannot connect output modules.

Output Module Type Numbers

Module Name	Terminal	Type No.
8-point Relay Output	Removable Terminal Block	FC4A-R081
16-point Relay Output		FC4A-R161
8-point Transistor Sink Output		FC4A-T08K1
8-point Transistor Source Output		FC4A-T08S1
16-point Transistor Sink Output	MIL Connector	FC4A-T16K3
16-point Transistor Source Output		FC4A-T16S3
32-point Transistor Sink Output		FC4A-T32K3
32-point Transistor Source Output		FC4A-T32S3

Parts Description



The above figures illustrate the 8-point relay output module.

(1) Expansion Connector	Connects to the CPU and other I/O modules. (The all-in-one 10- and 16-I/O type CPU modules cannot be connected.)
(2) Module Label	Indicates the output module Type No. and specifications.
(3) LED Indicator	Turns on when a corresponding output is on.
(4) Terminal No.	Indicates terminal numbers.
(5) Cable Terminal/Connector	Five different terminal/connector styles are available for wiring.

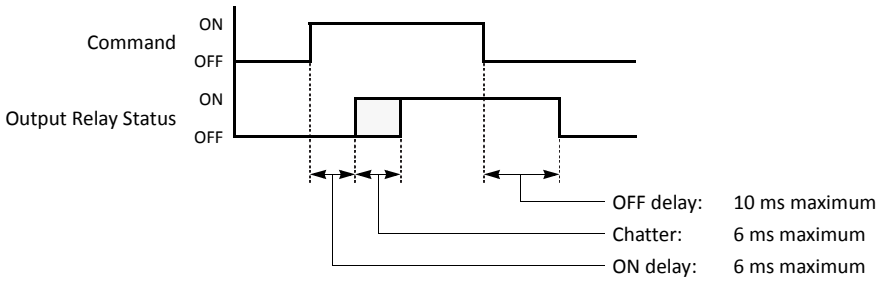
Relay Output Module Specifications

Type No.		FC4A-R081	FC4A-R161
Output Points and Common Lines		8 NO contacts in 2 common lines	16 NO contacts in 2 common lines
Terminal Arrangement		See Relay Output Module Terminal Arrangement on page 2-44.	
Maximum Load Current		2A per point	
		7A per common line	8A per common line
Minimum Switching Load		1 mA/5V DC (reference value)	
Initial Contact Resistance		30 mΩ maximum	
Electrical Life		100,000 operations minimum (rated load 1,800 operations/hour)	
Mechanical Life		20,000,000 operations minimum (no load 18,000 operations/hour)	
Rated Load		240V AC/2A (resistive load, inductive load cos ø = 0.4) 30V DC/2A (resistive load, inductive load L/R = 7 ms)	
Dielectric Strength		Between output and ⏚ or ⏚ terminals: 1,500V AC, 1 minute Between output terminal and internal circuit: 1,500V AC, 1 minute Between output terminals (COMs): 1,500V AC, 1 minute	
Connector on Mother Board		MC1.5/11-G-3.81BK (Phoenix Contact)	MC1.5/10-G-3.81BK (Phoenix Contact)
Connector Insertion/Removal Durability		100 times minimum	100 times minimum
Internal Current Draw	**All Outputs ON**	30 mA (5V DC) 40 mA (24V DC)	45 mA (5V DC) 75 mA (24V DC)
	All Outputs OFF	5 mA (5V DC) 0 mA (24V DC)	5 mA (5V DC) 0 mA (24V DC)
Internal Power Consumption (at 24V DC while all outputs ON)		1.16W	2.10W
Weight		110g	145g
Contact Protection Circuit for Relay Output		See page 3-17.	

Note: When relay output modules are connected to the all-in-one 24-I/O type CPU module or any slim type CPU module, the maximum number of relay outputs that can be turned on simultaneously, including the outputs on the CPU module, are shown below.

CPU Module Type	All-in-One 24-I/O CPU Module		Slim Type CPU Module
	AC Power Type	DC Power Type	
Maximum Relay Outputs Turning On Simultaneously	33	44	108 total 54 (on the left of expansion interface module) 54 (on the right of expansion interface module)

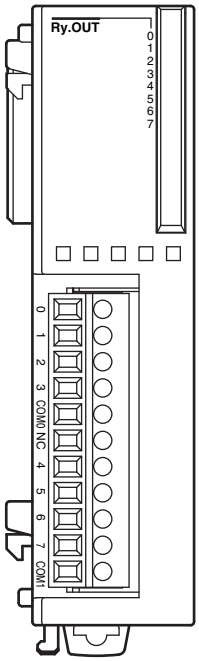
Output Delay

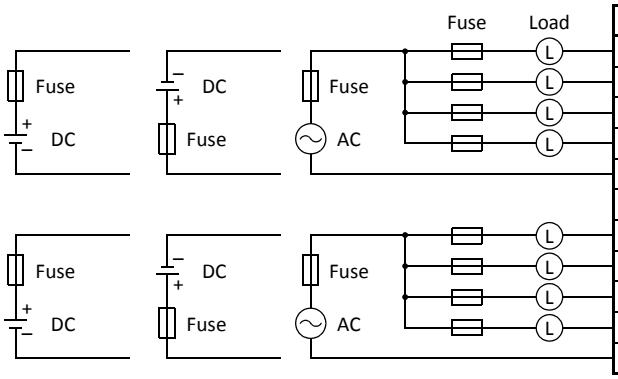


Relay Output Module Terminal Arrangement and Wiring Diagrams

FC4A-R081 (8-point Relay Output Module) — Screw Terminal Type

Applicable Terminal Block: **FC4A-PMT11P (supplied with the output module)**



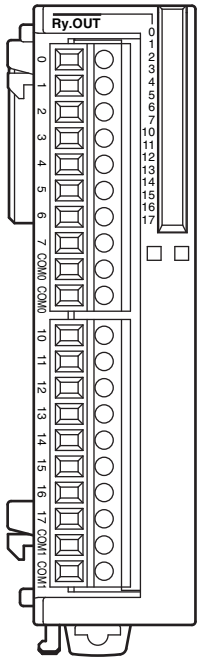


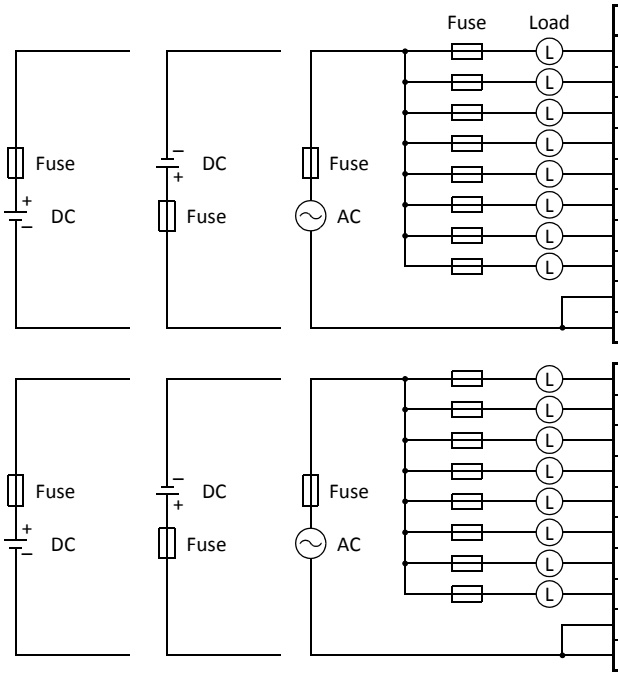
Terminal No.	Output
0	Q0
1	Q1
2	Q2
3	Q3
COM0	COM0
NC	NC
4	Q4
5	Q5
6	Q6
7	Q7
COM1	COM1

- COM0 and COM1 terminals are *not* interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

FC4A-R161 (16-point Relay Output Module) — Screw Terminal Type

Applicable Terminal Block: **FC4A-PMT10P (supplied with the output module)**





Terminal No.	Output
0	Q0
1	Q1
2	Q2
3	Q3
4	Q4
5	Q5
6	Q6
7	Q7
COM0	COM0
COM0	COM0
10	Q10
11	Q11
12	Q12
13	Q13
14	Q14
15	Q15
16	Q16
17	Q17
COM1	COM1
COM1	COM1

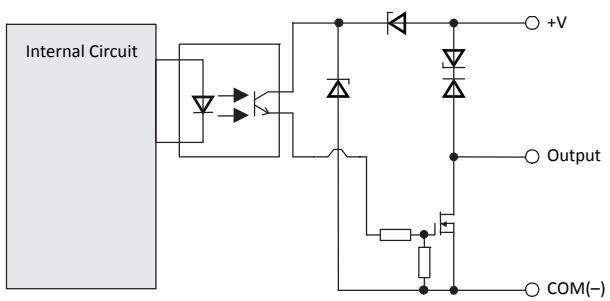
- COM0 terminals are interconnected.
- COM1 terminals are interconnected.
- COM0 and COM1 terminals are *not* interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

Transistor Sink Output Module Specifications

Type No.		FC4A-T08K1	FC4A-T16K3	FC4A-T32K3
Output Type		Transistor sink output		
Output Points and Common Lines		8 points in 1 common line	16 points in 1 common line	32 points in 2 common lines
Terminal Arrangement		See Transistor Sink Output Module Terminal Arrangement on pages 2-46 and 2-47.		
Rated Load Voltage		24V DC		
Operating Load Voltage Range		20.4 to 28.8V DC		
Rated Load Current		0.3A per output point	0.1A per output point	
Maximum Load Current (at 28.8V DC)		0.3A per output point 3A per common line	0.1A per output point 1A per common line	
Voltage Drop (ON Voltage)		1V maximum (voltage between COM and output terminals when output is on)		
Inrush Current		1A maximum		
Leakage Current		0.1 mA maximum		
Clamping Voltage		39V±1V		
Maximum Lamp Load		8W		
Inductive Load		L/R = 10 ms (28.8V DC, 1 Hz)		
External Current Draw		100 mA maximum, 24V DC (power voltage at the +V terminal)		
Isolation		Between output terminal and internal circuit: Photocoupler isolated Between output terminals: Not isolated		
Connector on Mother Board		MC1.5/10-G-3.81BK (Phoenix Contact)	FL20A2MA (Oki Electric Cable)	
Connector Insertion/Removal Durability		100 times minimum		
Internal Current Draw	**All Outputs ON**	10 mA (5V DC) 20 mA (24V DC)	10 mA (5V DC) 40 mA (24V DC)	20 mA (5V DC) 70 mA (24V DC)
	All Outputs OFF	5 mA (5V DC) 0 mA (24V DC)	5 mA (5V DC) 0 mA (24V DC)	10 mA (5V DC) 0 mA (24V DC)
Internal Power Consumption (at 24V DC while all outputs ON)		0.55W	1.03W	1.82W
Output Delay		Turn ON time: 300 µs maximum Turn OFF time: 300 µs maximum		
Weight (approx.)		85g	70g	105g

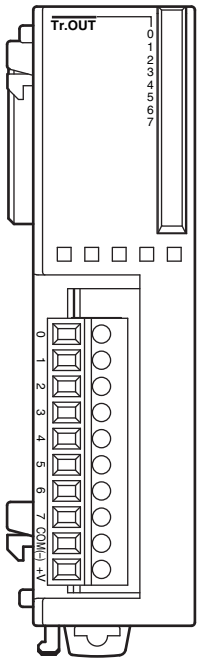
Output Internal Circuit

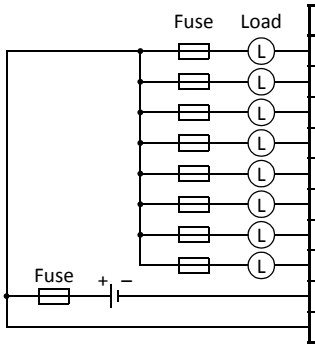
Sink Output



Transistor Sink Output Module Terminal Arrangement and Wiring Diagrams

FC4A-T08K1 (8-point Transistor Sink Output Module) — Screw Terminal Type
Applicable Terminal Block: FC4A-PMT10P (supplied with the output module)

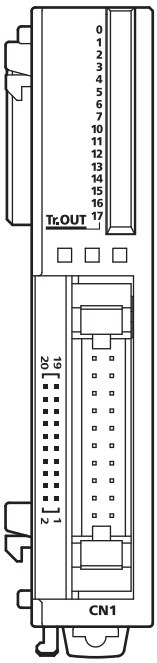


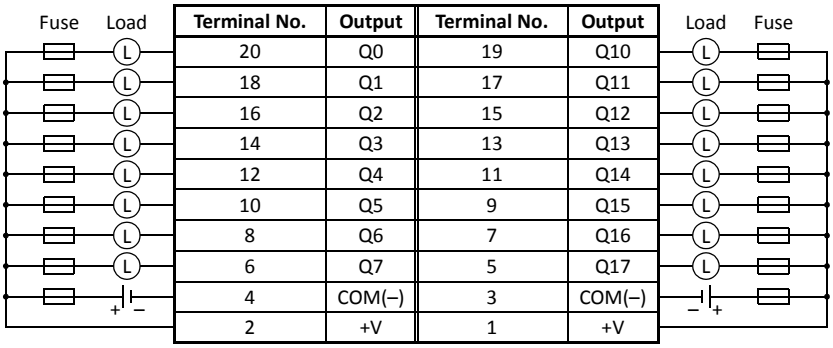


Terminal No.	Output
0	Q0
1	Q1
2	Q2
3	Q3
4	Q4
5	Q5
6	Q6
7	Q7
COM(–)	COM(–)
+V	+V

- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

FC4A-T16K3 (16-point Transistor Sink Output Module) — Connector Type
Applicable Connector: FC4A-PMC20P (*not* supplied with the output module)

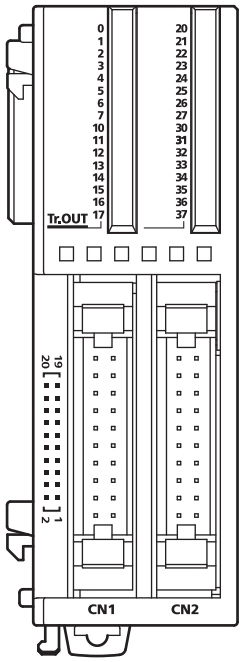




Terminal No.	Output	Terminal No.	Output
20	Q0	19	Q10
18	Q1	17	Q11
16	Q2	15	Q12
14	Q3	13	Q13
12	Q4	11	Q14
10	Q5	9	Q15
8	Q6	7	Q16
6	Q7	5	Q17
4	COM(–)	3	COM(–)
2	+V	1	+V

- COM(–) terminals are interconnected.
- +V terminals are interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

FC4A-T32K3 (32-point Transistor Sink Output Module) — Connector Type
Applicable Connector: FC4A-PMC20P (*not* supplied with the output module)



CN1

Fuse	Load	Terminal No.	Output	Terminal No.	Output	Load	Fuse
	L	20	Q0	19	Q10	L	
	L	18	Q1	17	Q11	L	
	L	16	Q2	15	Q12	L	
	L	14	Q3	13	Q13	L	
	L	12	Q4	11	Q14	L	
	L	10	Q5	9	Q15	L	
	L	8	Q6	7	Q16	L	
	L	6	Q7	5	Q17	L	
+	–	4	COM0(–)	3	COM0(–)	–	+
		2	+V0	1	+V0		

CN2

Fuse	Load	Terminal No.	Output	Terminal No.	Output	Load	Fuse
	L	20	Q20	19	Q30	L	
	L	18	Q21	17	Q31	L	
	L	16	Q22	15	Q32	L	
	L	14	Q23	13	Q33	L	
	L	12	Q24	11	Q34	L	
	L	10	Q25	9	Q35	L	
	L	8	Q26	7	Q36	L	
	L	6	Q27	5	Q37	L	
+	–	4	COM1(–)	3	COM1(–)	–	+
		2	+V1	1	+V1		

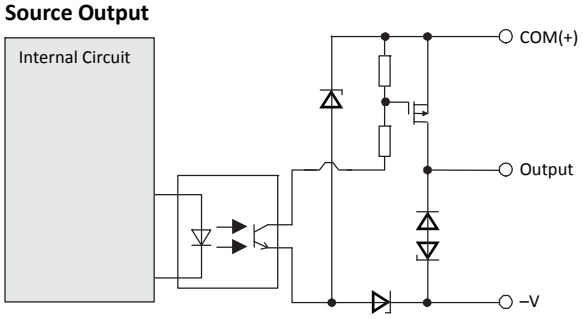
- Terminals on CN1 and CN2 are *not* interconnected.
- COM0(–) terminals are interconnected.
- COM1(–) terminals are interconnected.
- +V0 terminals are interconnected.
- +V1 terminals are interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

Transistor Source Output Module Specifications

Type No.		FC4A-T08S1	FC4A-T16S3	FC4A-T32S3
Output Type		Transistor source output		
Output Points and Common Lines		8 points in 1 common line	16 points in 1 common line	32 points in 2 common lines
Terminal Arrangement		See Transistor Source Output Module Terminal Arrangement on pages 2-49 and 2-50.		
Rated Load Voltage		24V DC		
Operating Load Voltage Range		20.4 to 28.8V DC		
Rated Load Current		0.3A per output point	0.1A per output point	
Maximum Load Current (at 28.8V DC)		0.3A per output point 3A per common line	0.1A per output point 1A per common line	
Voltage Drop (ON Voltage)		1V maximum (voltage between COM and output terminals when output is on)		
Inrush Current		1A maximum		
Leakage Current		0.1 mA maximum		
Clamping Voltage		39V±1V		
Maximum Lamp Load		8W		
Inductive Load		L/R = 10 ms (28.8V DC, 1 Hz)		
External Current Draw		100 mA maximum, 24V DC (power voltage at the –V terminal)		
Isolation		Between output terminal and internal circuit: Photocoupler isolated Between output terminals: Not isolated		
Connector on Mother Board		MC1.5/10-G-3.81BK (Phoenix Contact)	FL20A2MA (Oki Electric Cable)	
Connector Insertion/Removal Durability		100 times minimum		
Internal Current Draw	**All Outputs ON**	10 mA (5V DC) 20 mA (24V DC)	10 mA (5V DC) 40 mA (24V DC)	20 mA (5V DC) 70 mA (24V DC)
	All Outputs OFF	5 mA (5V DC) 0 mA (24V DC)	5 mA (5V DC) 0 mA (24V DC)	10 mA (5V DC) 0 mA (24V DC)
Internal Power Consumption (at 24V DC while all outputs ON)		0.55W	1.03W	1.82W
Output Delay		Turn ON time: 300 µs maximum Turn OFF time: 300 µs maximum		
Weight (approx.)		85g	70g	105g

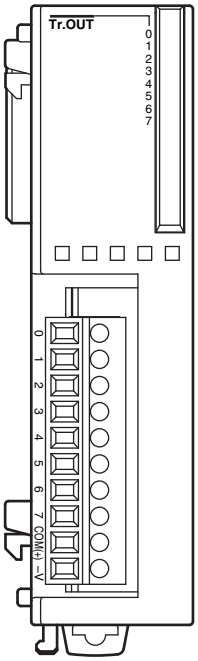
Output Internal Circuit

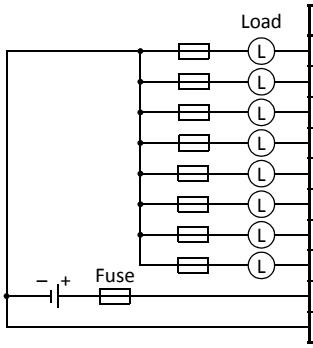
Source Output



Transistor Source Output Module Terminal Arrangement and Wiring Diagrams

FC4A-T08S1 (8-point Transistor Source Output Module) — Screw Terminal Type
Applicable Terminal Block: FC4A-PMT10P (supplied with the output module)

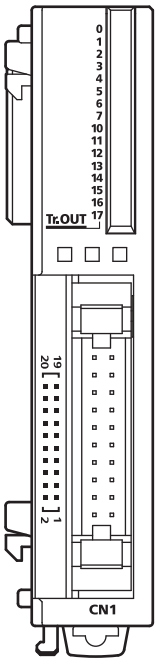


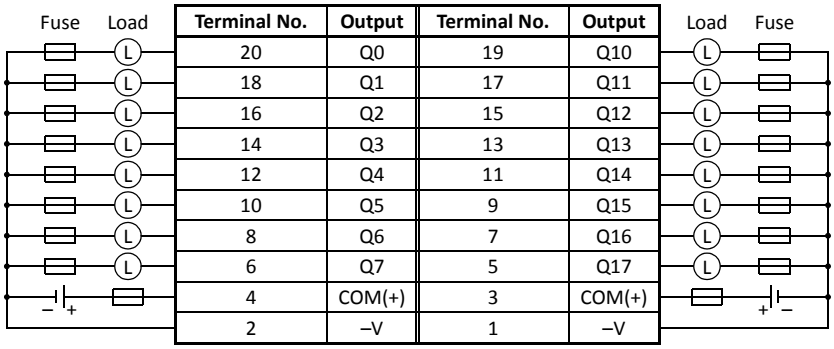


Terminal No.	Output
0	Q0
1	Q1
2	Q2
3	Q3
4	Q4
5	Q5
6	Q6
7	Q7
COM(+)	COM(+)
–V	–V

- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

FC4A-T16S3 (16-point Transistor Source Output Module) — Connector Type
Applicable Connector: FC4A-PMC20P (*not* supplied with the output module)

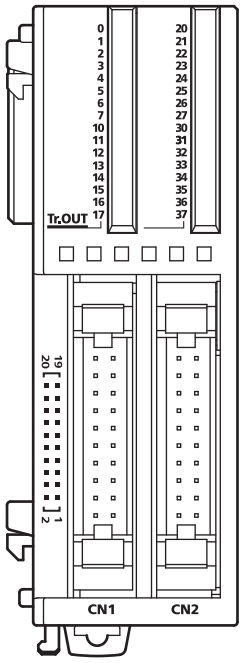




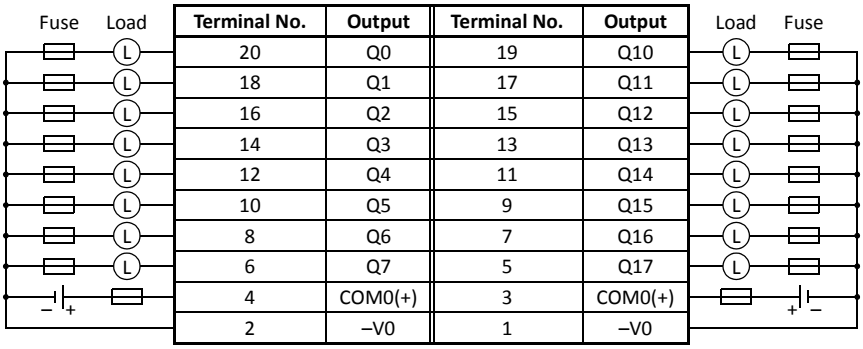
Terminal No.	Output	Terminal No.	Output
20	Q0	19	Q10
18	Q1	17	Q11
16	Q2	15	Q12
14	Q3	13	Q13
12	Q4	11	Q14
10	Q5	9	Q15
8	Q6	7	Q16
6	Q7	5	Q17
4	COM(+)	3	COM(+)
2	–V	1	–V

- COM(+) terminals are interconnected.
- –V terminals are interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

FC4A-T32S3 (32-point Transistor Source Output Module) — Connector Type
Applicable Connector: FC4A-PMC20P (*not* supplied with the output module)

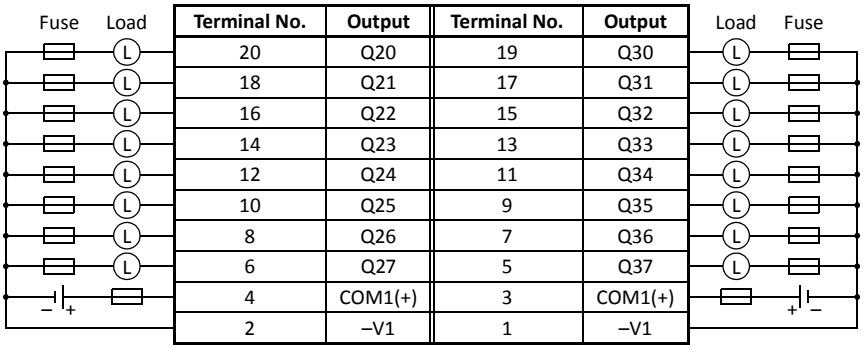


CN1



Terminal No.	Output	Terminal No.	Output
20	Q0	19	Q10
18	Q1	17	Q11
16	Q2	15	Q12
14	Q3	13	Q13
12	Q4	11	Q14
10	Q5	9	Q15
8	Q6	7	Q16
6	Q7	5	Q17
4	COM0(+)	3	COM0(+)
2	–V0	1	–V0

CN2



Terminal No.	Output	Terminal No.	Output
20	Q20	19	Q30
18	Q21	17	Q31
16	Q22	15	Q32
14	Q23	13	Q33
12	Q24	11	Q34
10	Q25	9	Q35
8	Q26	7	Q36
6	Q27	5	Q37
4	COM1(+)	3	COM1(+)
2	–V1	1	–V1

- Terminals on CN1 and CN2 are *not* interconnected.
- COM0(+) terminals are interconnected.
- COM1(+) terminals are interconnected.
- –V0 terminals are interconnected.
- –V1 terminals are interconnected.
- Connect a fuse appropriate for the load.
- For output wiring precautions, see page 3-16.

Mixed I/O Modules

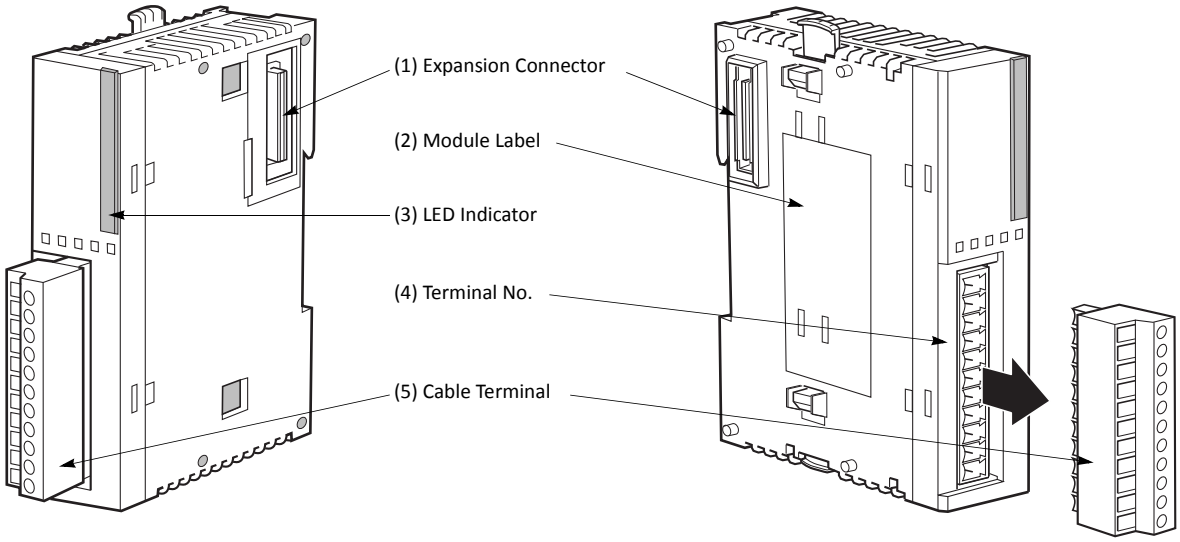
The 4-in/4-out mixed I/O module has 4-point DC sink/source inputs and 4-point relay outputs, with a screw terminal block for I/O wiring. The 16-in/8-out mixed I/O module has 16-point DC sink/source inputs and 8-point relay outputs, with a wire-clamp terminal block for I/O wiring.

The mixed I/O modules can be connected to the all-in-one 24-I/O type CPU module and all slim type CPU modules to expand input and output terminals. The all-in-one 10- and 16-I/O type CPU modules cannot connect mixed I/O modules.

Mixed I/O Module Type Numbers

Module Name	Terminal	Type No.
4-in/4-out Mixed I/O Module	Removable Terminal Block	FC4A-M08BR1
16-in/8-out Mixed I/O Module	Non-removable Wire-clamp Terminal Block	FC4A-M24BR2

Parts Description



The above figures illustrate the 4-in/4-out mixed I/O module.

(1) Expansion Connector	Connects to the CPU and other I/O modules. (The all-in-one 10- and 16-I/O type CPU modules cannot be connected.)
(2) Module Label	Indicates the mixed I/O module Type No. and specifications.
(3) LED Indicator	Turns on when a corresponding input or output is on.
(4) Terminal No.	Indicates terminal numbers.
(5) Cable Terminal	Two different terminal styles are available for wiring.

Mixed I/O Module Specifications

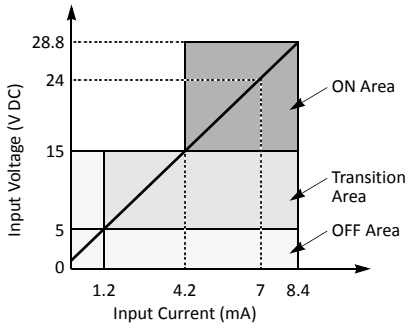
Type No.		FC4A-M08BR1	FC4A-M24BR2
I/O Points		4 inputs in 1 common line 4 outputs in 1 common line	16 inputs in 1 common line 8 outputs in 2 common lines
Terminal Arrangement		See Mixed I/O Module Terminal Arrangement on pages 2-53 and 2-54.	
Connector on Mother Board		MC1.5/11-G-3.81BK (Phoenix Contact)	Input: F6018-17P (Fujicon) Output: F6018-11P (Fujicon)
Connector Insertion/Removal Durability		100 times minimum	Not removable
Internal Current Draw	All I/Os ON	25 mA (5V DC) 20 mA (24V DC)	65 mA (5V DC) 45 mA (24V DC)
	All I/Os OFF	5 mA (5V DC) 0 mA (24V DC)	10 mA (5V DC) 0 mA (24V DC)
Internal Power Consumption (at 24V DC while all outputs ON)		0.65W	1.52W
Weight		95g	140g

DC Input Specifications (Mixed I/O Module)

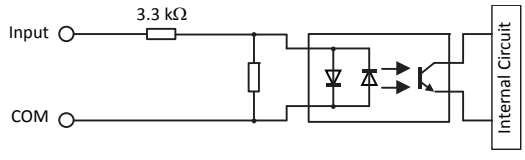
Input Points and Common Line	4 points in 1 common line	16 points in 1 common line
Rated Input Voltage	24V DC sink/source input signal	
Input Voltage Range	20.4 to 28.8V DC	
Rated Input Current	7 mA/point (24V DC)	
Input Impedance	3.4 kΩ	
Turn ON Time	4 ms (24V DC)	
Turn OFF Time	4 ms (24V DC)	
Isolation	Between input terminals: Not isolated Internal circuit: Photocoupler isolated	
External Load for I/O Interconnection	Not needed	
Signal Determination Method	Static	
Effect of Improper Input Connection	Both sinking and sourcing input signals can be connected. If any input exceeding the rated value is applied, permanent damage may be caused.	
Cable Length	3m (9.84 ft.) in compliance with electromagnetic immunity	

Input Operating Range

The input operating range of Type 1 (IEC 61131-2) input modules is shown below:

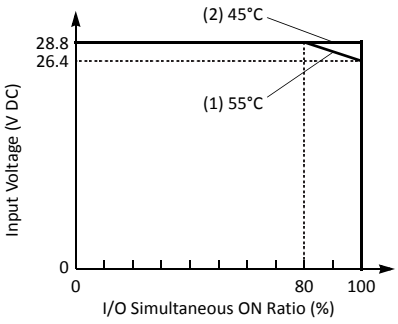


Input Internal Circuit



I/O Usage Limits

When using the FC4A-M24BR2 at an ambient temperature of 55°C in the normal mounting direction, limit the inputs and outputs, respectively, which turn on simultaneously along line (1).



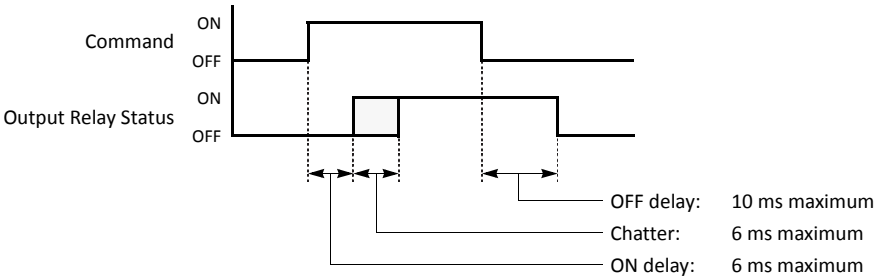
When using at 45°C, all I/Os can be turned on simultaneously at input voltage 28.8V DC as indicated with line (2).

When using the FC4A-M08BR1, all I/Os can be turned on simultaneously at 55°C, input voltage 28.8V DC.

Relay Output Specifications (Mixed I/O Module)

Type No.	FC4A-M08BR1	FC4A-M24BR2
Output Points and Common Lines	4 NO contacts in 1 common line	8 NO contacts in 2 common lines
Maximum Load Current	2A per point 7A per common line	
Minimum Switching Load	1 mA/5V DC (reference value)	
Initial Contact Resistance	30 mΩ maximum	
Electrical Life	100,000 operations minimum (rated load 1,800 operations/hour)	
Mechanical Life	20,000,000 operations minimum (no load 18,000 operations/hour)	
Rated Load	240V AC/2A (resistive load, inductive load cos ø = 0.4) 30V DC/2A (resistive load, inductive load L/R = 7 ms)	
Dielectric Strength	Between output and ⏚ or ⏚ terminals: 1,500V AC, 1 minute Between output terminal and internal circuit: 1,500V AC, 1 minute Between output terminals (COMs): 1,500V AC, 1 minute	
Contact Protection Circuit for Relay Output	See page 3-17.	

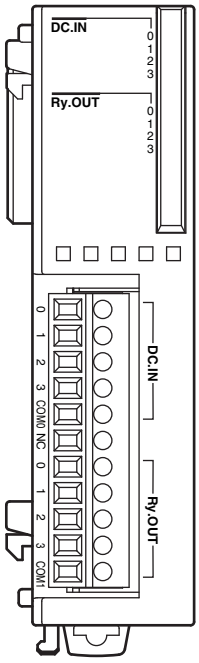
Output Delay

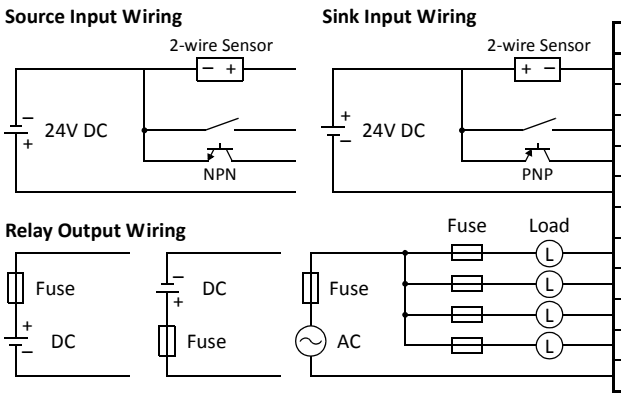


Mixed I/O Module Terminal Arrangement and Wiring Diagrams

FC4A-M08BR1 (Mixed I/O Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the mixed I/O module)

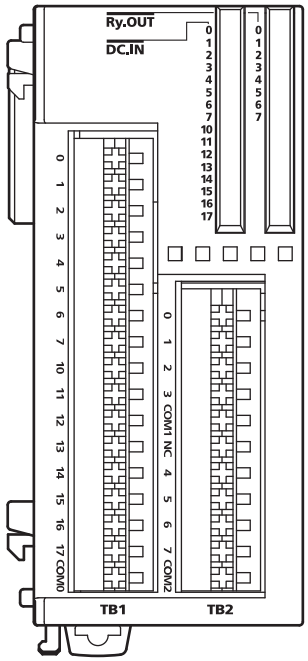




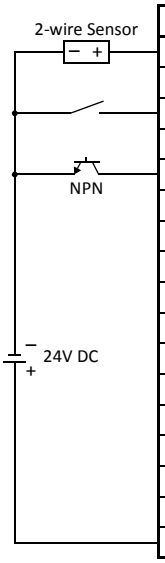
Terminal No.	I/O
0	I0
1	I1
2	I2
3	I3
COM0	COM0
NC	NC
0	Q0
1	Q1
2	Q2
3	Q3
COM1	COM1

- COM0 and COM1 terminals are *not* interconnected.
- For wiring precautions, see pages 3-15 and 3-16.

FC4A-M24BR2 (Mixed I/O Module) — Wire-clamp Terminal Type

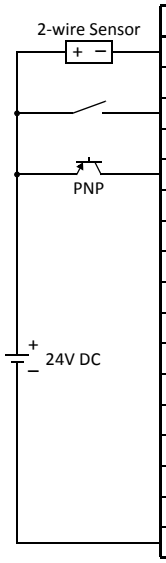


Source Input Wiring



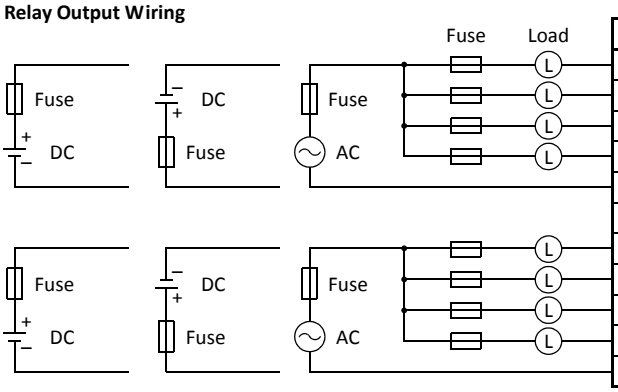
Terminal No.	Input
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	I10
10	I11
11	I12
12	I13
13	I14
14	I15
15	I16
16	I17
17	COM0

Sink Input Wiring



Terminal No.	Input
1	I0
2	I1
3	I2
4	I3
5	I4
6	I5
7	I6
8	I7
9	I10
10	I11
11	I12
12	I13
13	I14
14	I15
15	I16
16	I17
17	COM0

Relay Output Wiring



Terminal No.	Output
1	Q0
2	Q1
3	Q2
4	Q3
5	COM1
6	NC
7	Q4
8	Q5
9	Q6
10	Q7
11	COM2

- COM0, COM1, and COM2 terminals are *not* interconnected.
- Connect a fuse appropriate for the load.
- For wiring precautions, see pages 3-15 and 3-16.

Analog I/O Modules

Analog I/O modules are available in 3-I/O types, 2-, 4-, and 8-input types, and 1-, 2- and 4-output types. The input channel can accept voltage and current signals, thermocouple and resistance thermometer signals, or thermistor signals. The output channel generates voltage and current signals.

Analog I/O Module Type Numbers

Name	I/O Signal	I/O Points	Category	Type No.
Analog I/O Module	Voltage (0 to 10V DC) Current (4 to 20mA)	2 inputs	END Refresh Type	FC4A-L03A1
	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output		
	Thermocouple (K, J, T) Resistance thermometer (Pt100)	2 inputs		FC4A-L03AP1
	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output		
Analog Input Module	Voltage (0 to 10V DC) Current (4 to 20mA)	2 inputs		FC4A-J2A1
	Voltage (0 to 10V DC) Current (4 to 20mA) Thermocouple (K, J, T) Resistance thermometer (Pt100, Pt1000, Ni100, Ni1000)	4 inputs	Ladder Refresh Type	FC4A-J4CN1
	Voltage (0 to 10V DC) Current (4 to 20mA)	8 inputs		FC4A-J8C1
	Thermistor (NTC, PTC)	8 inputs		FC4A-J8AT1
Analog Output Module	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output	END Refresh Type	FC4A-K1A1
	Voltage (–10 to +10V DC) Current (4 to 20mA)	2 outputs	Ladder Refresh Type	FC4A-K2C1
	Voltage (0 to 10V DC) Current (4 to 20mA)	4 outputs		FC4A-K4A1

END Refresh Type and Ladder Refresh Type

Depending on the internal circuit design for data refreshing, analog I/O modules are categorized into two types.

Analog I/O Module Category		END Refresh Type	Ladder Refresh Type
While CPU is running	Parameter Refreshing	At the end processing in the first scan	When executing ANST macro
	Analog I/O Data Refreshing	At the end processing	In the step after ANST macro (always refreshed whether input to ANST is on or off)
While CPU is stopped	Analog Output Data Refreshing	When M8025 (maintain outputs while CPU stopped) is on, output data is refreshed. When off, output is turned off.	Maintains output status when the CPU is stopped. Output data can be changed using STPA instruction while the CPU is stopped. See page 9-22.
Data Register Allocation		By default	Optionally designated in ANST macro

END Refresh Type

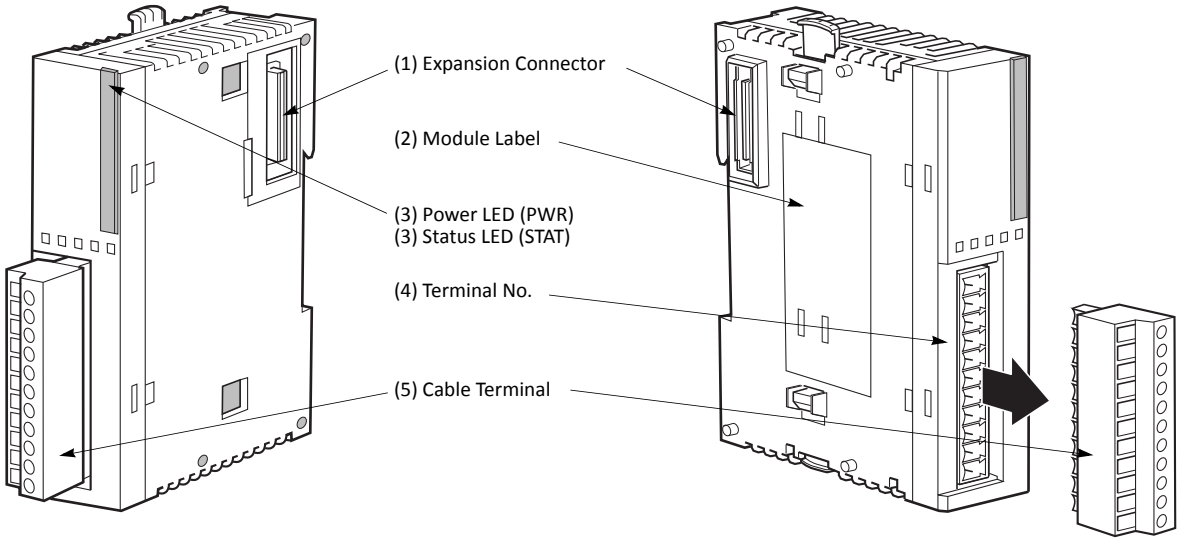
Each END refresh type analog I/O module is allocated 20 data registers to store analog I/O data and parameters for controlling analog I/O operation. These data registers are updated at every end processing while the CPU module is running. WindLDR has ANST macro to program the analog I/O modules.

The CPU module checks the analog I/O configuration only once at the end processing in the first scan. If you have changed the parameter while the CPU is running, stop and restart the CPU to enable the new parameter.

Ladder Refresh Type

Each ladder refresh type analog I/O module can be allocated any data registers to store analog I/O data and parameters for controlling analog I/O operation. The data registers are programmed in the ANST macro. Analog I/O data are updated at the ladder step following the ANST macro. Analog I/O parameters are updated when the ANST macro is executed, so analog I/O parameters can be changed while the CPU is running.

Parts Description

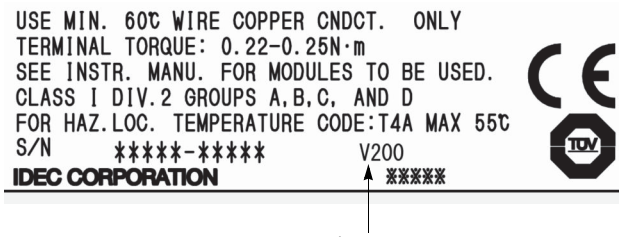


The terminal style depends on the model of analog I/O modules.

(1) Expansion Connector Connects to the CPU and other I/O modules.
(The all-in-one 10- and 16-I/O type CPU modules cannot be connected.)

(2) Module Label Indicates the analog I/O module Type No. and specifications.

Four analog I/O modules FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, and FC4A-K1A1 of version 200 or higher have the version number indicated on the module label attached to the side of the module. Confirm the version number because some specifications differ depending on the version number. Analog I/O modules earlier than version 200 do not have a version number indicated on the module label.



(3) Power LED (PWR) END refresh type FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-K1A1, FC4A-K4A1 (Note):
Turns on when power is supplied to the analog I/O module.
Note: Power LED of FC4A-K4A1 flashes when external power supply error is occurring. For details about operating status, see pages 9-14 and 9-17.

(3) Status LED (STAT) Ladder refresh type FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, FC4A-K2C1:
Indicates the operating status of the analog I/O module.

Status LED	Analog Input Operating Status
OFF	Analog I/O module is stopped
ON	Normal operation
Flash	Initializing Changing configuration Hardware initialization error External power supply error

(4) Terminal No. Indicates terminal numbers.

(5) Cable Terminal All analog I/O modules have a removable terminal block.

Analog I/O Module Specifications

General Specifications (END Refresh Type)

Type No.	FC4A-L03A1	FC4A-L03AP1	FC4A-J2A1	FC4A-K1A1
Rated Power Voltage	24V DC			
Allowable Voltage Range	20.4 to 28.8V DC			
Terminal Arrangement	See Analog I/O Module Terminal Arrangement on pages 2-64 to 2-67.			
Connector on Mother Board	MC1.5/11-G-3.81BK (Phoenix Contact)			
Connector Insertion/Removal Durability	100 times minimum			
Internal Current Draw	50 mA (5V DC) 0 mA (24V DC)	50 mA (5V DC) 0 mA (24V DC)	50 mA (5V DC) 0 mA (24V DC)	50 mA (5V DC) 0 mA (24V DC)
External Current Draw (Note 1)	50 (45) mA (Note 2) (24V DC)	50 (40) mA (Note 2) (24V DC)	40 (35) mA (Note 2) (24V DC)	40 mA (24V DC)
Weight (Approx.)	100g (85g) (Note 2)			

Note 1: The external current draw is the value when all analog inputs are used and the analog output value is at 100%.

Note 2: Values in ( ) represent analog I/O modules earlier than version 200. For analog I/O module version, see page 2-56.

General Specifications (Ladder Refresh Type)

Type No.	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1
Rated Power Voltage	24V DC		
Allowable Voltage Range	20.4 to 28.8V DC		
Terminal Arrangement	See Analog I/O Module Terminal Arrangement on pages 2-64 to 2-67.		
Connector on Mother Board	MC1.5/10-G-3.81BK (Phoenix Contact)		
Connector Insertion/Removal Durability	100 times minimum		
Internal Current Draw	50 mA (5V DC) 0 mA (24V DC)	40 mA (5V DC) 0 mA (24V DC)	45 mA (5V DC) 0 mA (24V DC)
External Current Draw (Note)	55 mA (24V DC)	50 mA (24V DC)	55 mA (24V DC)
Weight	140g	140g	125g

Type No.	FC4A-K2C1	FC4A-K4A1
Rated Power Voltage	24V DC	
Allowable Voltage Range	20.4 to 28.8V DC	
Terminal Arrangement	See Analog I/O Module Terminal Arrangement on pages 2-64 to 2-67.	
Connector on Mother Board	MC1.5/10-G-3.81BK (Phoenix Contact)	MC1.5/11-G-3.81BK (Phoenix Contact)
Connector Insertion/Removal Durability	100 times minimum	
Internal Current Draw	60 mA (5V DC) 0 mA (24V DC)	65 mA (5V DC) 0 mA (24V DC)
External Current Draw (Note)	85 mA (24V DC)	130 mA (24V DC)
Weight (Approx.)	110g	100g

Note: The external current draw is the value when all analog inputs are used and the analog output value is at 100%.

Analog Input Specifications (END Refresh Type)

Type No.		FC4A-L03A1 / FC4A-J2A1		FC4A-L03AP1	
Analog Input Signal Type		Voltage Input	Current Input	Thermocouple	Resistance Thermometer
Input Range		0 to 10V DC	4 to 20 mA DC	Type K (0 to 1300°C) Type J (0 to 1200°C) Type T (0 to 400°C)	Pt 100 3-wire type (–100 to 500°C)
Input Impedance		1 MΩ minimum	250Ω	1 MΩ minimum	1 MΩ minimum
Allowable Conductor Resistance (per wire)		—	—	—	200Ω maximum
Input Detection Current		—	—	—	1.0 mA maximum
AD Conversion	Sample Duration Time	10 (20) ms (Note 1)		10 (20) ms (Note 1)	20 ms
	Sample Repetition Time	20 ms		20 ms	40 (20) ms (Note 1)
	Total Input System Transfer Time (Note 2)	60 (105) ms + 1 scan time (Note 1)		60 (200) ms + 1 scan time (Note 1)	80 (200) ms + 1 scan time (Note 1)
	Type of Input	Single-ended input	Differential input		
	Operating Mode	Self-scan			
	Conversion Method	∑Δ type ADC			
Input Error	Maximum Error at 25°C	±0.2% of full scale		±0.2% of full scale + cold junction compensation error (±4°C maximum)	±0.2% of full scale
	Temperature Coefficient	±0.006% of full scale/°C			
	Repeatability after Stabilization Time	±0.5% of full scale			
	Non-lineality	±0.2% of full scale			
	Maximum Error	±1% of full scale			
Data	Digital Resolution	4096 increments (12 bits) 13,000 increments maximum (14 bits) (Note 3)			
	Input Value of LSB	2.5 mV	4 µA	K: 0.100°C/0.180°F (0.325°C) J: 0.100°C/0.180°F (0.300°C) T: 0.100°C/0.180°F (0.100°C) (Note 3)	0.100°C/0.180°F (0.150°C) (Note 3)
	Data Type in Application Program	Default: 0 to 4095 Optional: –32768 to 32767 (selectable for each channel) (Note 4)			
	Monotonicity	Yes			
	Input Data Out of Range	Detectable (Note 5)			

Type No.		FC4A-L03A1 / FC4A-J2A1		FC4A-L03AP1	
Analog Input Signal Type		**Voltage Input**	**Current Input**	**Thermocouple**	**Resistance Thermometer**
Noise Resistance	**Maximum Temporary Deviation during Electrical Noise Tests**	±1% maximum (when 1 kV is directly applied to the power supply line and a 1 kV clamp voltage is applied to I/O lines)			
		(±3% maximum) (Note 1) (when a 500V clamp voltage is applied to the power supply and I/O lines)			(Not assured) (Note 1)
	Input Filter	No			
	Recommended Cable for Noise Immunity	Twisted pair shielded cable		—	
	Crosstalk	2 LSB maximum			
Isolation		Between input and power circuit: Transformer isolated Between input and internal circuit: Photocoupler-isolated			
Effect of Improper Input Connection		No damage			
Maximum Permanent Allowed Overload (No Damage)		13V DC	40 mA DC	—	
Selection of Analog Input Signal Type		Using programming software			
Calibration or Verification to Maintain Rated Accuracy		Not possible			

Note 1: Values in ( ) represent analog I/O modules earlier than version 200. For analog I/O module version, see page 2-56.

Note 2: Total input system transfer time = Sample repetition time + Internal processing time

Note 3: Minimum values represent analog input data in Celsius and Fahrenheit. Values in ( ) represent analog I/O modules earlier than version 200.

Note 4: The data processed in the analog I/O module can be linear-converted to a value between –32768 and 32767. The optional range designation, and analog I/O data minimum and maximum values can be selected using data registers allocated to analog I/O modules. See page 9-13.

Note 5: When an error is detected, a corresponding error code is stored to a data register allocated to analog I/O operating status. See page 9-7.

Analog Input Specifications (Ladder Refresh Type)

Type No.		FC4A-J4CN1 / FC4A-J8C1		FC4A-J4CN1	
Analog Input Signal Type		Voltage Input	Current Input	Thermocouple	Resistance Thermometer
Input Range		0 to 10V DC	4 to 20 mA DC	Type K: 0 to 1300°C Type J: 0 to 1200°C Type T: 0 to 400°C	Pt100, Pt1000: 3-wire type (–100 to 500°C) Ni100, Ni1000: 3-wire type (–60 to 180°C)
Input Impedance		1 MΩ	FC4A-J4CN1: 7Ω FC4A-J8C1: 100Ω	1 MΩ	—
Input Detection Current		—	—	—	0.1 mA
AD Conversion	Sample Duration Time	2 ms maximum			
	Sample Repetition Time	FC4A-J4CN1: 10 ms maximum FC4A-J8C1: 2 ms maximum		30 ms maximum	10 ms maximum
	Total Input System Transfer Time (Note 1)	FC4A-J4CN1: 50 ms × channels + 1 scan time FC4A-J8C1: 8 ms × channels + 1 scan time		85 ms × channels + 1 scan time	50 ms × channels + 1 scan time
	Type of Input	Single-ended input			
	Operating Mode	Self-scan			
	Conversion Method	FC4A-J4CN1: ∑Δ type ADC FC4A-J8C1: Successive approximation register method			
Input Error	Maximum Error at 25°C	±0.2% of full scale		±0.2% of full scale + cold junction compensation error (±3°C maximum)	Pt100, Ni100: ±0.4% of full scale Pt1000, Ni1000: ±0.2% of full scale
	Cold Junction Compensation Error	—	—	±3.0°C maximum	—
	Temperature Coefficient	±0.005% of full scale/°C			
	Repeatability after Stabilization Time	±0.5% of full scale			
	Non-lineality	±0.04% of full scale			
	Maximum Error	±1% of full scale			

Type No.		FC4A-J4CN1 / FC4A-J8C1		FC4A-J4CN1	
Analog Input Signal Type		**Voltage Input**	**Current Input**	**Thermocouple**	**Resistance Thermometer**
Data	**Digital Resolution**	50000 increments (16 bits)		K: Approx. 24000 increments (15 bits) J: Approx. 33000 increments (15 bits) T: Approx. 10000 increments (14 bits)	Pt100: Approx. 6400 increments (13 bits) Pt1000: Approx. 64000 increments (16 bits) Ni100: Approx. 4700 increments (13 bits) Ni1000: Approx. 47000 increments (16 bits)
	Input Value of LSB	0.2 mV	0.32 µA	K: 0.058°C J: 0.038°C T: 0.042°C	Pt100: 0.086°C Pt1000: 0.0086°C Ni100: 0.037°C Ni1000: 0.0037°C
	Data Type in Application Program	Default: 0 to 50000		Default: 0 to 50000	Pt100, Ni100: 0 to 6000 Pt1000, Ni1000: 0 to 60000
		Optional: –32768 to 32767 (selectable for each channel) (Note 2)			
		—		Temperature: Celsius, Fahrenheit	
	Monotonicity	Yes			
	Input Data Out of Range	Detectable (Note 3)			
Noise Resistance	**Maximum Temporary Deviation during Electrical Noise Tests**	±3% maximum (when a 500V clamp voltage is applied to the power supply and I/O lines)			Not assured
	Input Filter	Software			
	Recommended Cable for Noise Immunity	Twisted pair cable		—	
	Crosstalk	2 LSB maximum			
Isolation		Between input and power circuit: Transformer isolated Between input and internal circuit: Photocoupler-isolated			
Effect of Improper Input Connection		No damage			
Maximum Permanent Allowed Overload (No Damage)		11V DC	22 mA DC	—	
Selection of Analog Input Signal Type		Using programming software			
Calibration or Verification to Maintain Rated Accuracy		Not possible			

Note 1: Total input system transfer time = Sample repetition time + Internal processing time
The total input system transfer time increases in proportion to the number of channels used.

Note 2: The data processed in the analog I/O module can be linear-converted to a value between –32768 and 32767. The optional range designation, and analog I/O data minimum and maximum values can be selected using data registers allocated to analog I/O modules. See page 9-13.

Note 3: When an error is detected, a corresponding error code is stored to a data register allocated to analog I/O operating status. See page 9-7.

Analog Input Specifications (Ladder Refresh Type)

Type No.		FC4A-J8AT1	
Analog Input Signal Type		NTC Thermistor	PTC Thermistor
Input Range		–50 to 150°C	
Applicable Thermistor		100 kΩ maximum	
Input Detection Current		0.1 mA	
AD Conversion	Sample Duration Time	2 ms maximum	
	Sample Repetition Time	2 ms maximum	
	Total Input System Transfer Time (Note 1)	10 ms × channels + 1 scan time (Note 1)	
	Type of Input	Single-ended input	
	Operating Mode	Self-scan	
	Conversion Method	Successive approximation register method	
Input Error	Maximum Error at 25°C	±0.2% of full scale	
	Temperature Coefficient	±0.005% of full scale/°C	
	Repeatability after Stabilization Time	±0.5% of full scale	
	Non-lineality	No	
	Maximum Error	±1% of full scale	
Data	Digital Resolution	Approx. 4000 increments (12 bits)	
	Input Value of LSB	25Ω	
	Data Type in Application Program	Default: 0 to 4000 Optional: –32768 to 32767 (selectable for each channel) (Note 2) Temperature: Celsius, Fahrenheit (NTC only) Resistance: 0 to 10000	
	Monotonicity	Yes	
	Input Data Out of Range	Detectable (Note 3)	
Noise Resistance	Maximum Temporary Deviation during Electrical Noise Tests	±3% maximum (when a 500V clamp voltage is applied to the power supply and I/O lines)	
	Input Filter	Software	
	Recommended Cable for Noise Immunity	—	
	Crosstalk	2 LSB maximum	
Isolation		Between input and power circuit: Transformer isolated Between input and internal circuit: Photocoupler-isolated	
Effect of Improper Input Connection		No damage	
Selection of Analog Input Signal Type		Using programming software	
Calibration or Verification to Maintain Rated Accuracy		Not possible	

Note 1: Total input system transfer time = Sample repetition time + Internal processing time
The total input system transfer time increases in proportion to the number of channels used.

Note 2: The data processed in the analog I/O module can be linear-converted to a value between –32768 and 32767. The optional range designation, and analog I/O data minimum and maximum values can be selected using data registers allocated to analog I/O modules. See page 9-13.

Note 3: When an error is detected, a corresponding error code is stored to a data register allocated to analog I/O operating status. See page 9-7.

Analog Output Specifications

Category			END Refresh Type			Ladder Refresh	
Type No.			FC4A-L03A1	FC4A-L03AP1	FC4A-K1A1	FC4A-K4A1	FC4A-K2C1
Output Range		Voltage	0 to 10V DC				–10 to +10V DC
		Current	4 to 20 mA DC				
Load	Load Impedance		1 (2) kΩ minimum (voltage), 300Ω maximum (current) (Note 1)				
	Applicable Load Type		Resistive load				
DA Conversion	Settling Time		10 (50) ms (Note 1)	10 (130) ms (Note 1)	10 (50) ms (Note 1)	2 ms/ch (Note 2)	1 ms/ch
	Total Output System Transfer Time		Settling time + 1 scan time			2 ms × channels + 1 scan time	1 ms × channels + 1 scan time
Output Error	Maximum Error at 25°C		±0.2% of full scale				
	Temperature Coefficient		±0.015% of full scale/°C				±0.005% of full scale/°C
	Repeatability after Stabilization Time		±0.5% of full scale				
	Output Voltage Drop		±1% of full scale				
	Non-lineality		±0.2% of full scale				
	Output Ripple		1 LSB maximum			20 mV maximum	±0.1% of full scale
	Overshoot		0%				
	Total Error		±1% of full scale				
Data	Digital Resolution		4096 increments (12 bits)				50000 increments (16 bits)
	Output Value of LSB	Voltage	2.5 mV				0.4 mV
		Current	4 µA				0.32 µA
	Data Type in Application Program		Default: 0 to 4095 (voltage, current)				–25000 to 25000 (voltage)
							0 to 50000 (current)
			Optional: –32768 to 32767 (selectable for each channel) (Note 3)				
	Monotonicity		Yes				
	Current Loop Open		Not detectable				
Noise Resistance	Maximum Temporary Deviation during Electrical Noise Tests (Note 4)		±1% (±3%) maximum (Note 1)			±4% maximum	±3% maximum
	Recommended Cable for Noise Immunity		Twisted pair shielded cable				Twisted pair cable
	Crosstalk		No crosstalk because of 1 channel output			2 LSB maximum	
Isolation			Between input and power circuit: Transformer isolated Between input and internal circuit: Photocoupler-isolated				
Effect of Improper Output Connection			No damage				
Selection of Analog Output Signal Type			Using programming software				
Calibration or Verification to Maintain Rated Accuracy			Not possible				

Note 1: Values in ( ) represent analog I/O modules earlier than version 200. For analog I/O module version, see page 2-56.

Note 2: Rise time is not included.

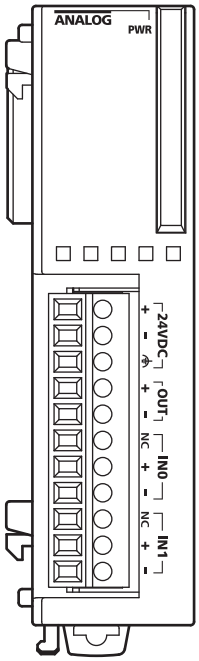
Note 3: The data processed in the analog I/O module can be linear-converted to a value between –32768 and 32767. The optional range designation, and analog I/O data minimum and maximum values can be selected using data registers allocated to analog I/O modules. See page 9-13.

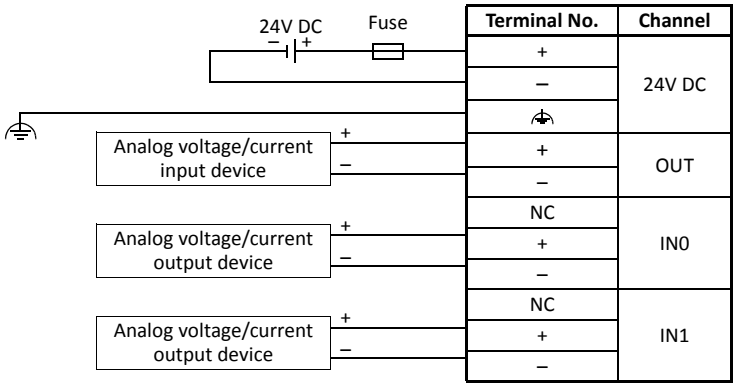
Note 4: For analog I/O modules of version 200 or higher, the value represents when 1 kV is directly applied to the power supply line and a 1 kV clamp voltage is applied to I/O lines. For analog I/O modules earlier than version 200, the value represents when a 500V clamp voltage is applied to the power supply and I/O lines.

Analog I/O Module Terminal Arrangement and Wiring Diagrams

FC4A-L03A1 (Analog I/O Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the analog I/O module)



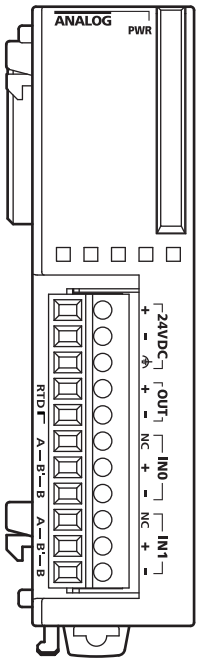


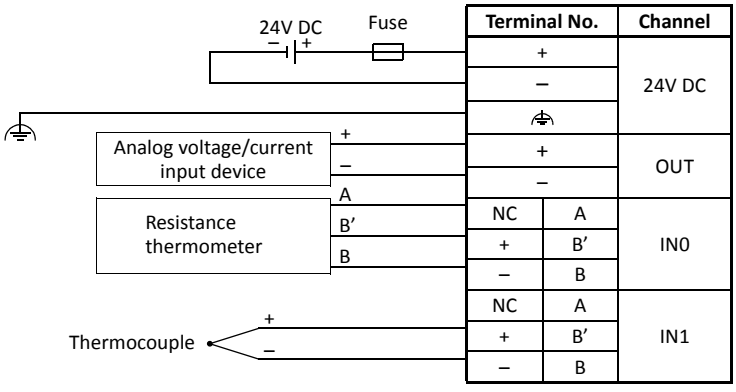
Terminal No.		Channel
+		24V DC
–		
⏚		
+		OUT
–		
NC		IN0
+		
–		
NC		IN1
+		
–		

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- Before turn on the power, make sure that wiring to the analog I/O module is correct. If wiring is incorrect, the analog I/O module may be damaged.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-L03AP1 (Analog I/O Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the analog I/O module)



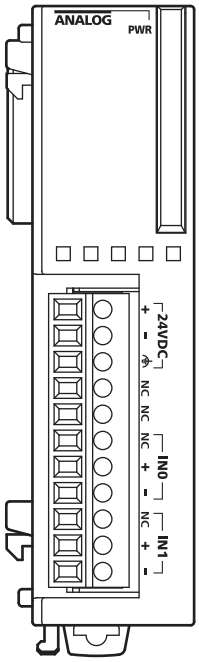


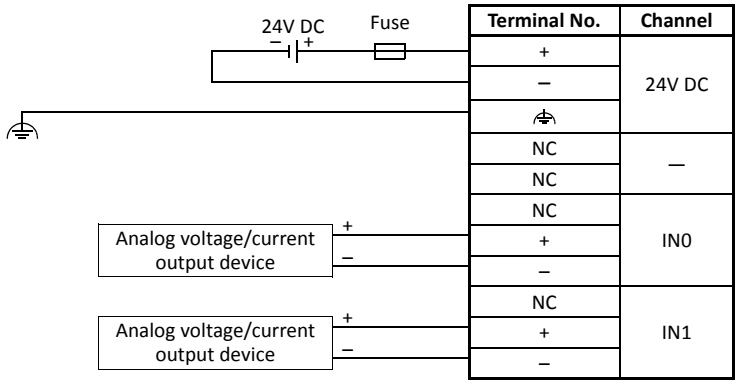
Terminal No.		Channel
+		24V DC
–		
⏚		
+		OUT
–		
NC	A	IN0
+	B'	
–	B	
NC	A	IN1
+	B'	
–	B	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- When connecting a resistance thermometer, connect the three wires to RTD (resistance temperature detector) terminals A, B', and B of input channel IN0 or IN1.
- When connecting a thermocouple, connect the two wires to terminals + and – of input channels IN0 or IN1.
- Do not connect any wiring to unused terminals.
- Do not connect the thermocouple to a hazardous voltage (60V DC or 42.4V peak or higher).
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-J2A1 (Analog Input Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the analog input module)



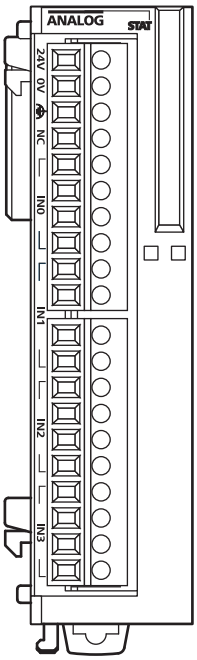


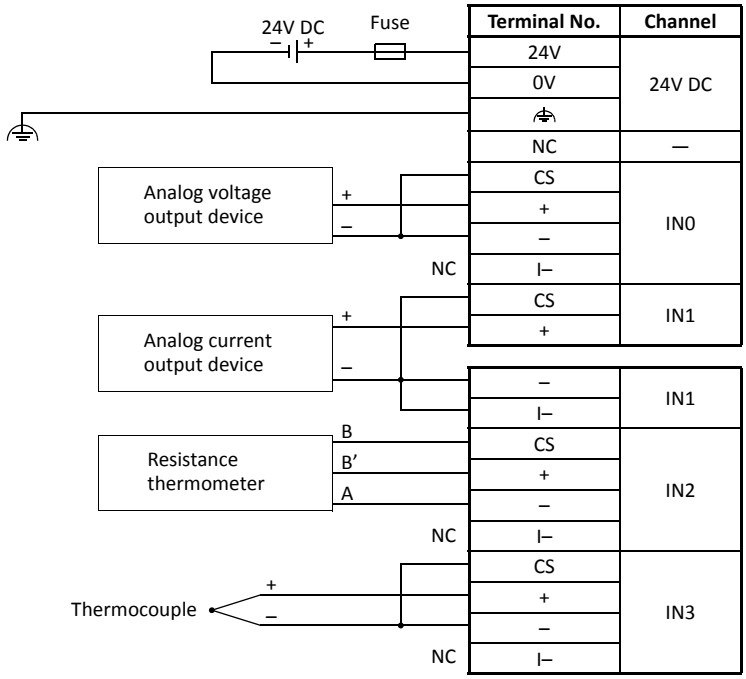
Terminal No.	Channel
+	24V DC
–	
⏚	
NC	—
NC	
NC	IN0
+	
–	
NC	IN1
+	
–	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-J4CN1 (Analog Input Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT10P (supplied with the analog input module)



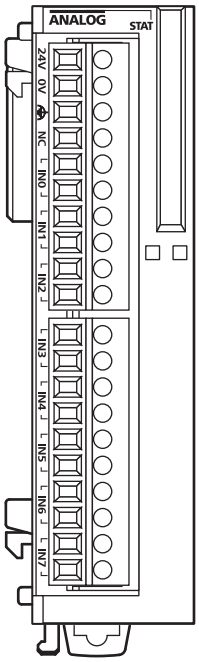


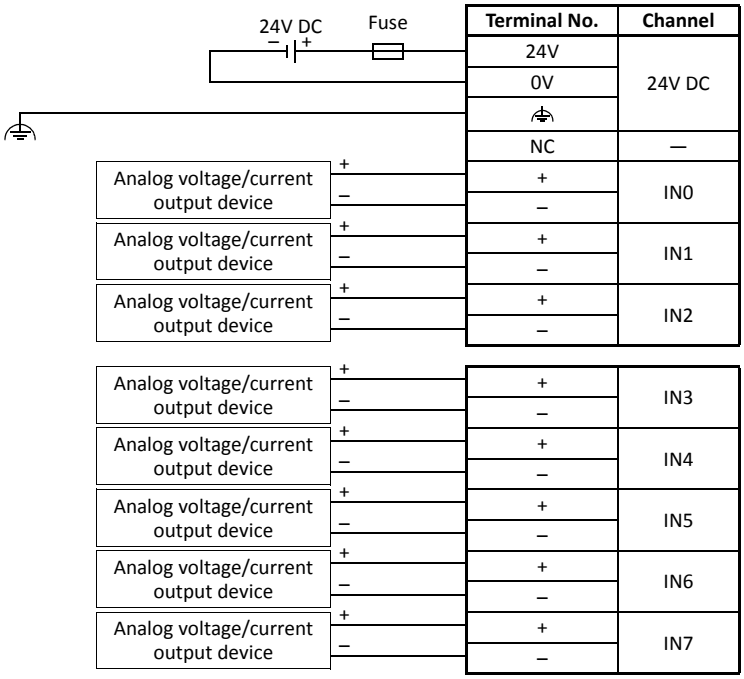
Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
CS	IN0
+	
–	
I–	
CS	IN1
+	
–	IN1
I–	
B	IN2
B’	
A	
NC	
CS	IN3
+	
–	
I–	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- When connecting a resistance thermometer, connect three wires B, B’, and A to the CS (current sense), +, and – terminals of input channels IN0 through IN3, respectively.
- When connecting a thermocouple, connect the + wire to the + terminal and the – wire to the CS and – terminals.
- Do not connect the thermocouple to a hazardous voltage (60V DC or 42.4V peak or higher).
- Do not connect any wiring to unused terminals.
- – terminals of input channels IN0 through IN3 are interconnected.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-J8C1 (Analog Input Module) — Screw Terminal Type

Applicable Terminal Block: **FC4A-PMT10P (supplied with the analog input module)**



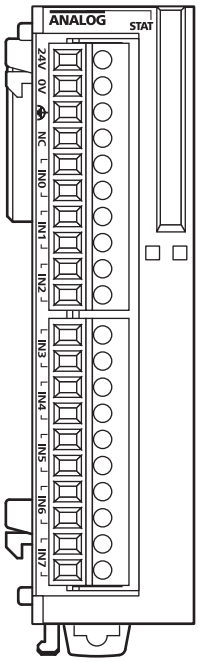


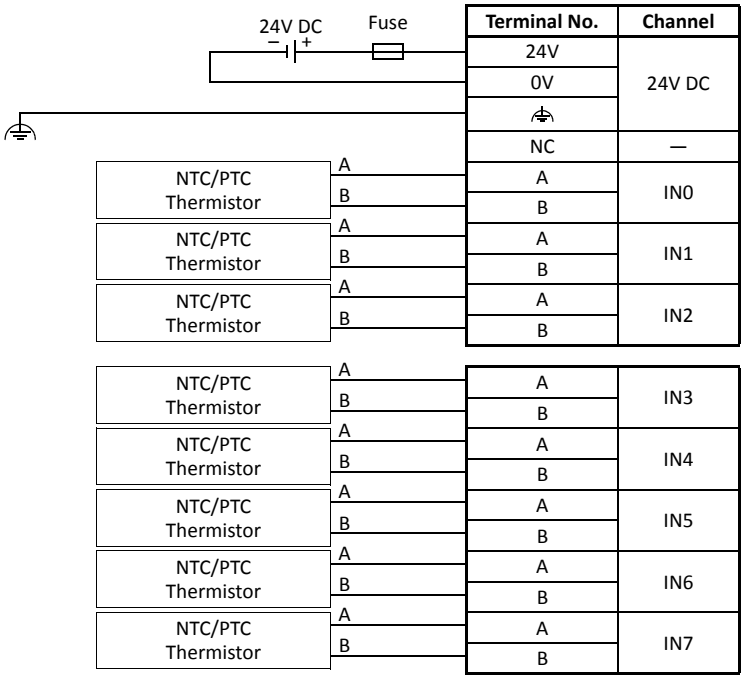
Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
+	IN0
–	
+	IN1
–	
+	IN2
–	
+	IN3
–	
+	IN4
–	
+	IN5
–	
+	IN6
–	
+	IN7
–	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- – terminals of input channels IN0 through IN7 are interconnected.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-J8AT1 (Analog Input Module) — Screw Terminal Type

Applicable Terminal Block: **FC4A-PMT10P (supplied with the analog input module)**



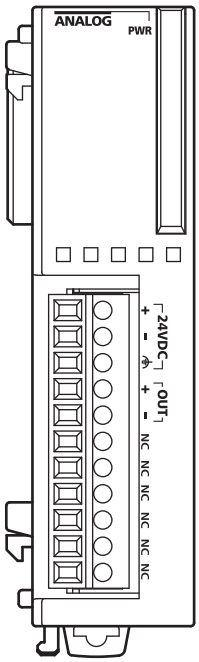


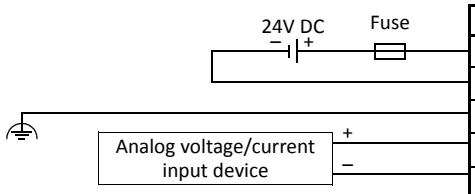
Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
A	IN0
B	
A	IN1
B	
A	IN2
B	
A	IN3
B	
A	IN4
B	
A	IN5
B	
A	IN6
B	
A	IN7
B	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-K1A1 (Analog Output Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the analog output module)



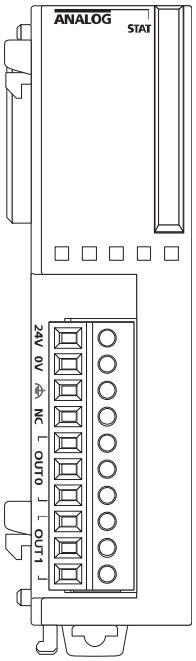


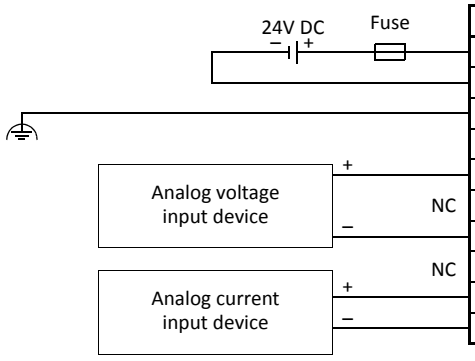
Terminal No.	Channel
+	24V DC
–	
⏚	
+	OUT
–	
NC	—
NC	
NC	
NC	—
NC	
NC	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-K2C1 (Analog Output Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT10P (supplied with the analog output module)



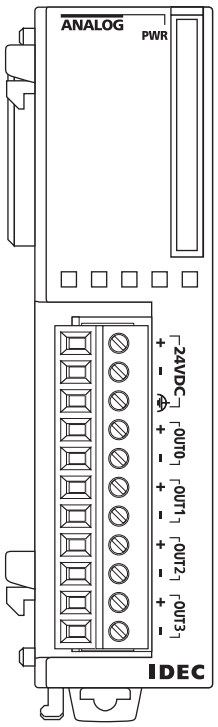


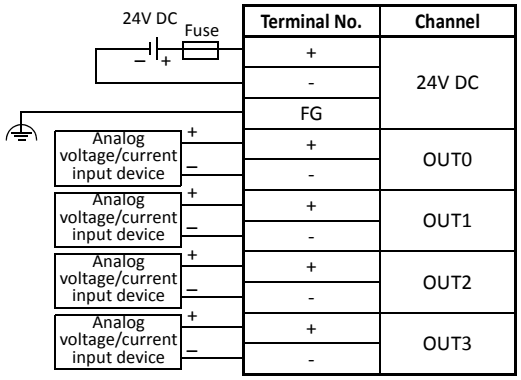
Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
V+	OUT0
I+	
–	
V+	OUT1
I+	
–	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- – terminals of output channels OUT0 and OUT1 are interconnected.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

FC4A-K4A1 (Analog Output Module) — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT11P (supplied with the analog output module)





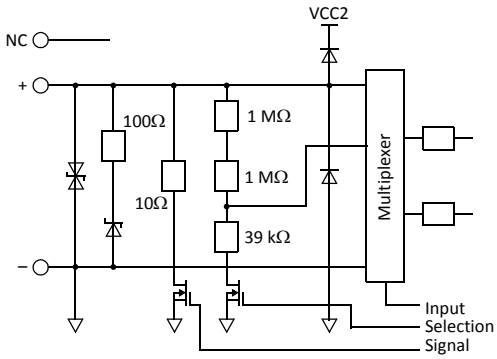
Terminal No.	Channel
+	24V DC
-	
FG	
+	OUT0
-	
+	OUT1
-	
+	OUT2
-	
+	OUT3
-	

- Connect a fuse appropriate for the applied voltage and current draw, at the position shown in the diagram. This is required when equipment containing the MicroSmart is destined for Europe.
- Do not connect any wiring to unused terminals.
- When the analog I/O module may malfunction due to noise, use the shielded cable for the analog input and output and connect both ends of the shield to a ground.

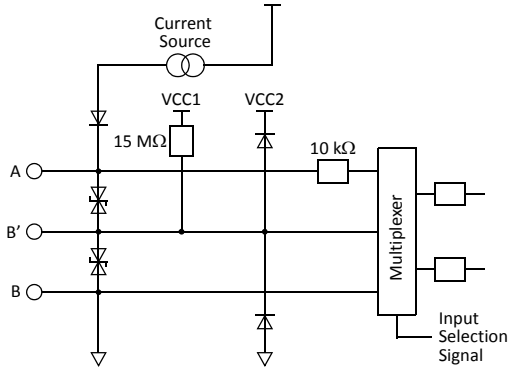
Type of Protection

Input Circuits

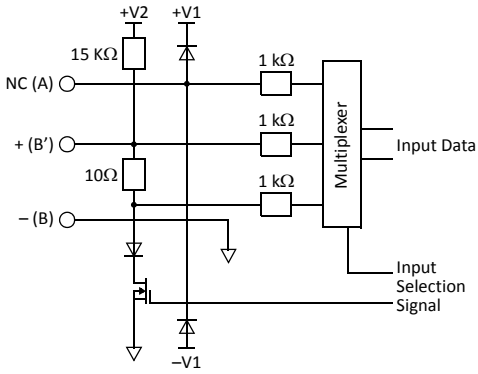
FC4A-L03A1, FC4A-J2A1 (Ver. 200 or higher)



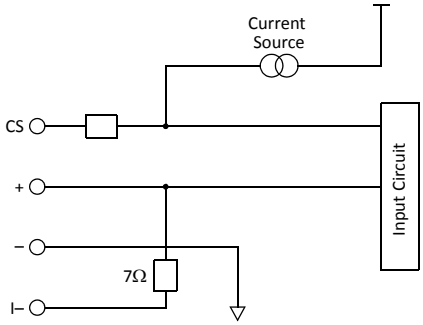
FC4A-L03AP1 (Ver. 200 or higher)



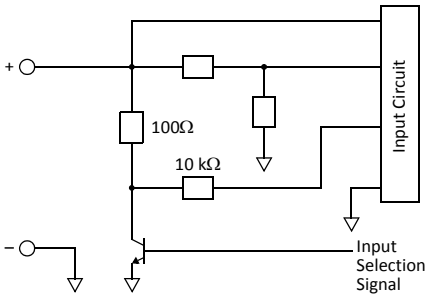
FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1



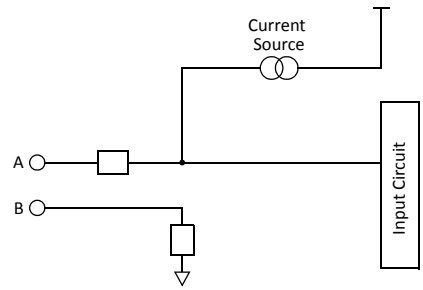
FC4A-J4CN1



FC4A-J8C1

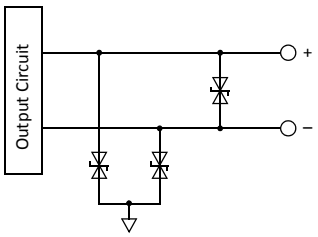


FC4A-J8AT1

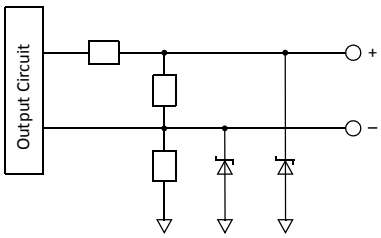


Output Circuits

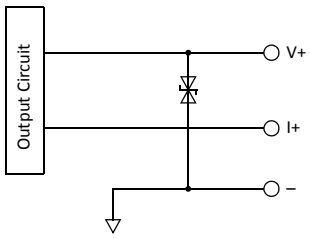
FC4A-L03A1, FC4A-L03AP1, FC4A-K1A1 (Ver. 200 or higher)



FC4A-L03A1, FC4A-L03AP1, FC4A-K1A1

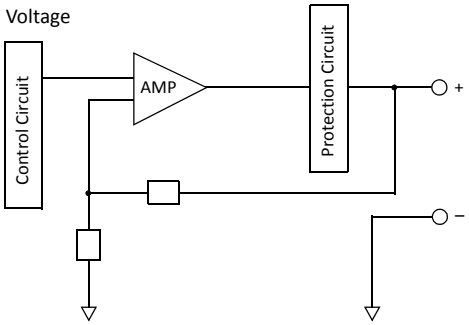


FC4A-K2C1

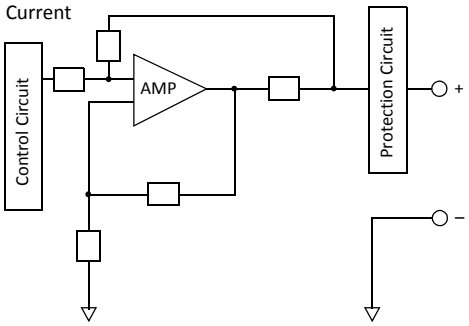


FC4A-K4A1

Voltage



Current



Power Supply for Analog I/O Modules

When supplying power to the analog I/O modules, take the following considerations.

- **Power Supply for FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-K1A1, and FC4A-K4A1**

Use separate power supplies for the MicroSmart CPU module and FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-K1A1, and FC4A-K4A1. Power up the analog I/O modules at least 1 second earlier than the CPU module. This is recommended to ensure correct operation of the analog I/O control.

Note: When re-powering up the analog I/O modules FC4A-L03A1, -L03AP1, and -J2A1, a time interval is needed before turning on these modules. If a single power supply is used for the MicroSmart CPU module and the analog I/O modules, turn on the analog I/O modules at least 5 seconds (at 25°C) after turning off these modules. If separate power supplies are used for the MicroSmart CPU module and the analog I/O modules, turn on the analog I/O modules at least 30 seconds (at 25°C) after turning off the analog I/O modules whether the CPU module is powered up or not.

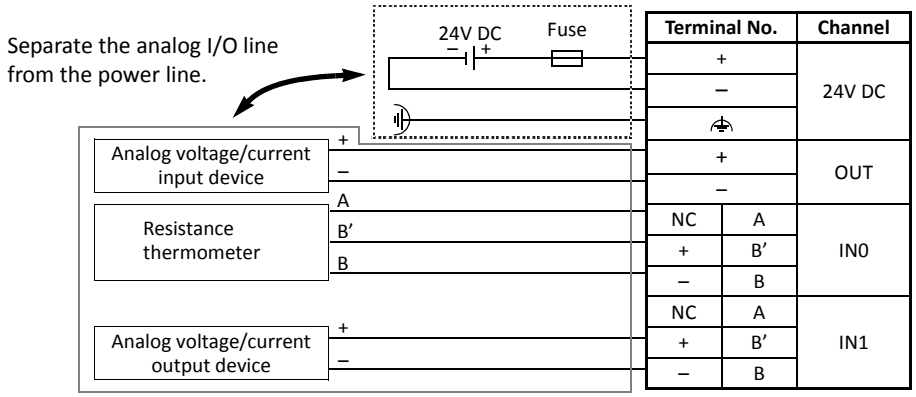
- **Power Supply for FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, and FC4A-K2C1**

Use the same power supply for the MicroSmart CPU module and FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, and FC4A-K2C1 to suppress the influence of noises.

After the CPU module has started to run, ladder refresh type analog input modules perform initialization for a maximum of 5 seconds. During this period, the analog input data have an indefinite value. Design the user program to make sure that the analog input data are read to the CPU module after the analog input operating status has changed to 0 (normal operation). For the analog input operating status, see page 9-14.

Wiring Analog I/O Lines

Separate the analog I/O lines, particularly resistance thermometer inputs, from motor lines as much as possible to suppress the influence of noises.

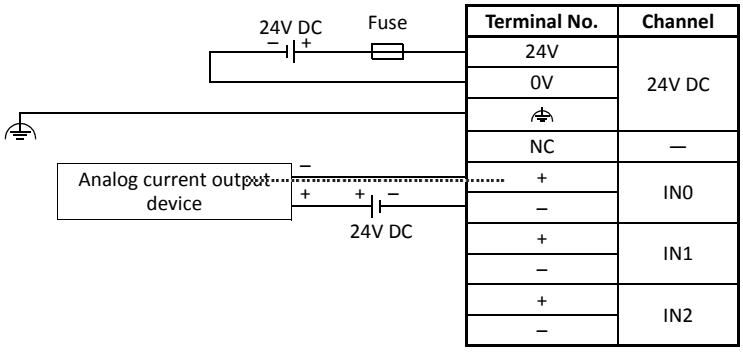


Terminal No.		Channel
+		24V DC
–		
⏚		
+		OUT
–		
NC	A	IN0
+	B'	
–	B	
NC	A	IN1
+	B'	
–	B	

Note: FC5A all-in-one 24-I/O type CPU modules cannot use analog I/O modules in combination with the AS-Interface master module (FC4A-AS62M) and/or expansion RS232C/RS485 communication module (FC5A-SIF2 or FC5A-SIF4). When using these modules in combination with analog I/O modules, use the slim type CPU module.

Wiring 2-Wire Analog Current Output Devices

To use an analog input module with a 2-wire analog device, wire the analog device in series with a separate 24V DC power supply.



Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
+	IN0
–	
+	IN1
–	
+	IN2
–	

Expansion Interface Module

Slim type CPU modules can normally connect a maximum of seven I/O modules. Using the expansion interface module makes it possible to connect additional eight I/O modules to expand another 256 I/O points. The maximum number of I/O points is 512, including the I/Os in the CPU module.

Expansion interface modules are available in two mounting styles: for integrated mounting and separate mounting.

For the integrated mounting, expansion interface module FC5A-EXM2 is mounted next to the seventh I/O module and more I/O modules are mounted next to the expansion interface module.

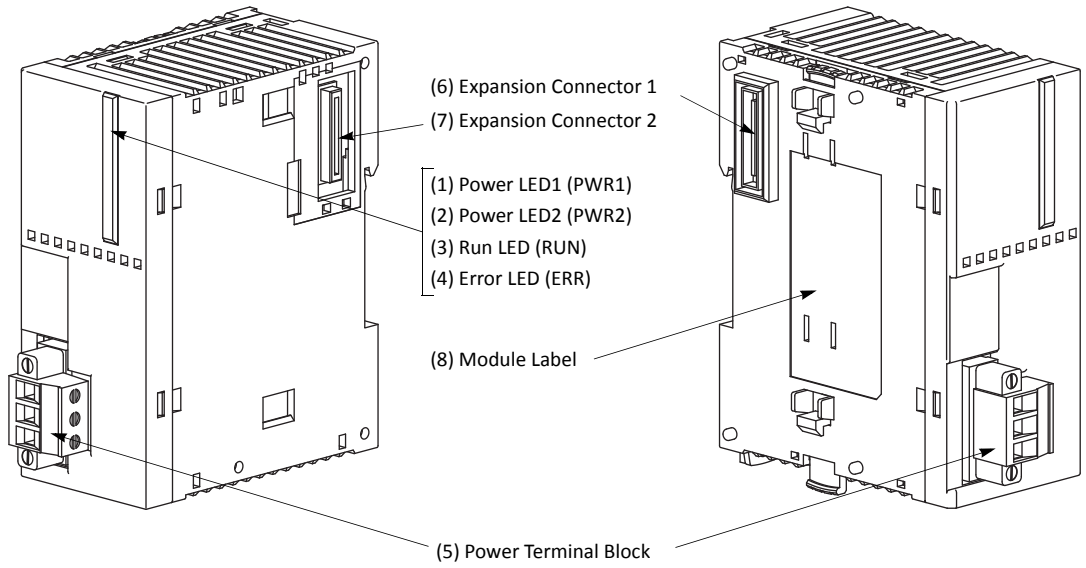
For the separate mounting, expansion interface master module FC5A-EXM1M and expansion interface slave module FC5A-EXM1S are used. The expansion interface master module is mounted at the end of I/O modules, the expansion interface slave module is used at the beginning of the other I/O modules, and the master and slave modules are connected with expansion interface cable FC5A-KX1C.

Expansion Interface Module Type Number

Module Name	Type No.	Remarks
Expansion Interface Module	FC5A-EXM2	For integrated mounting
Expansion Interface Master Module	FC5A-EXM1M	For separate mounting
Expansion Interface Slave Module	FC5A-EXM1S	
Expansion Interface Cable	FC5A-KX1C	

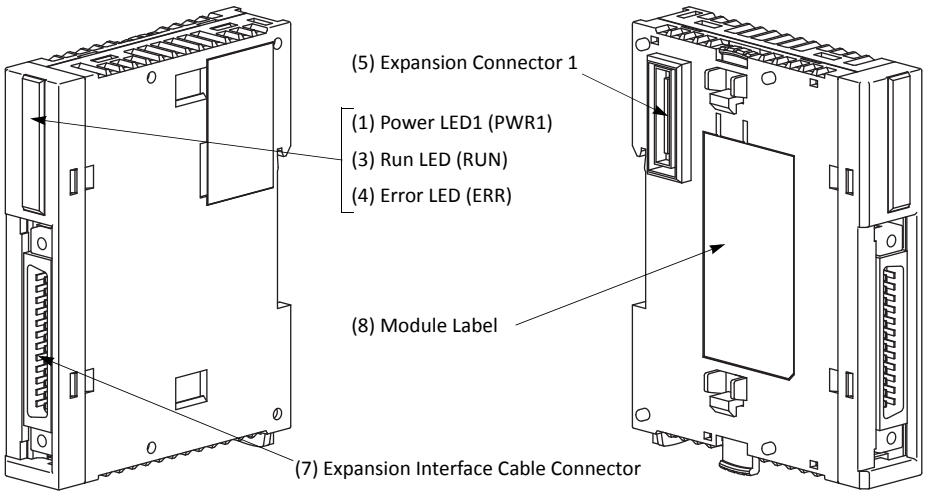
Parts Description

Expansion Interface Module FC5A-EXM2

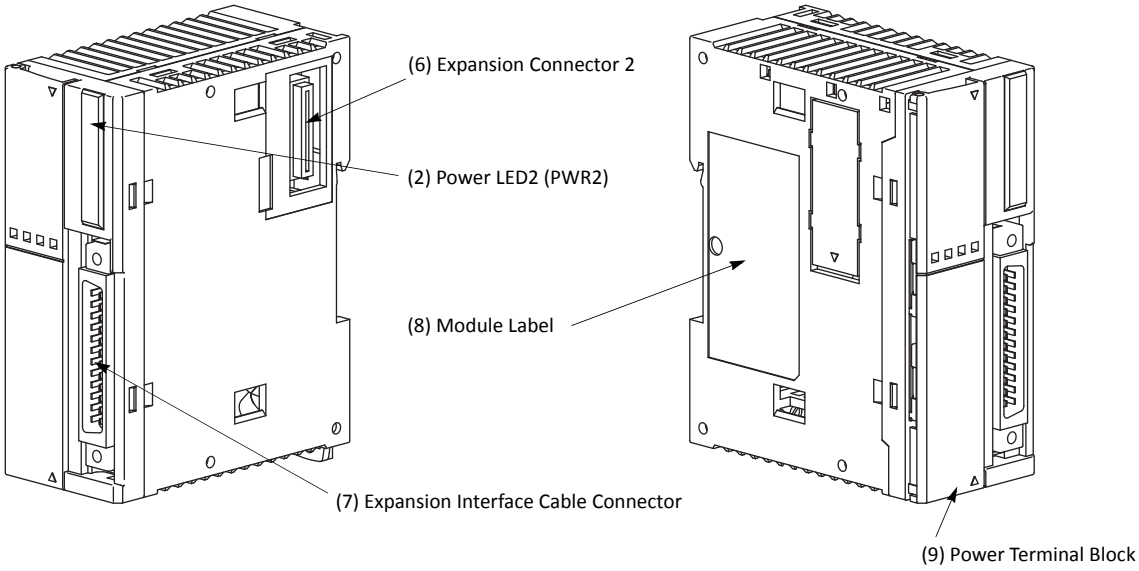


(1) Power LED1 (PWR1)	Turns on when power is supplied from the CPU module.
(2) Power LED2 (PWR2)	Turns on when power is supplied to trailing I/O modules.
(3) Run LED (RUN)	Turns on when the expansion interface module is executing I/O refresh.
(4) Error LED (ERR)	Turns on or flashes when an error occurs in the expansion interface module.
(5) Power Terminal Block	Connect 24V DC power to these terminals.
(6) Expansion Connector 1	Connects to I/O and function modules mounted on the CPU module side.
(7) Expansion Connector 2	Connects to trailing I/O modules.
(8) Module Label	Indicates the expansion interface module Type No. and specifications.

Expansion Interface Master Module FC5A-EXM1M



Expansion Interface Slave Module FC5A-EXM1S



(1) Power LED1 (PWR1) Turns on when power is supplied to the expansion interface module.

(2) Power LED2 (PWR2) Turns on when power is supplied to trailing I/O modules.

(3) Run LED (RUN) Turns on when the expansion interface module is executing I/O refresh.

(4) Error LED (ERR) Turns on or flashes when an error occurs in the expansion interface module.

(5) Expansion Connector 1 Connects to I/O and function modules mounted on the CPU module side.

(6) Expansion Connector 2 Connects to trailing I/O modules.

(7) Expansion Interface Cable Connector Connects the expansion interface cable.

(8) Module Label Indicates the expansion interface module Type No. and specifications.

(9) Power Terminal Block Connect 24V DC power to these terminals.

General Specifications (Expansion Interface Module)

Type No.		FC5A-EXM2 Expansion Interface Module	FC5A-EXM1M Expansion Interface Master Module	FC5A-EXM1S Expansion Interface Slave Module
Rated Power Voltage		24V DC (supplied from external power)	—	24V DC (supplied from external power)
Allowable Voltage Range		20.4 to 26.4V DC (including ripple)	—	20.4 to 26.4V DC (including ripple)
Current Draw		Internal power (supplied from CPU module): 50 mA (5V DC) 0 mA (24V DC) External power: With I/O modules (Note 1) 750 mA (26.4V DC)	Internal power (supplied from CPU module): 90 mA (5V DC) 0 mA (24V DC)	Internal power (supplied from CPU module): 0 mA (5V DC) 0 mA (24V DC) External power: With I/O modules (Note 1) 750 mA (26.4V DC)
Maximum Power Consumption (External Power) (Note 1)		19W (26.4V DC)	—	19 (26.4V DC)
Allowable Momentary Power Interruption		10 ms minimum (24V DC)	—	10 ms minimum (24V DC)
Applicable CPU Module		Slim type CPU modules		
I/O Expansion		Between CPU module and expansion interface module: 7 I/O modules maximum (6 modules maximum incl. a maximum of 2 AS-Interface master modules) Beyond the expansion interface module: 8 digital I/O modules maximum (AC input modules are not applicable) (Note 2)		
I/O Refresh Time		See page A-5.		
Communication through Expansion Interface Cable		—	Proprietary protocol	
Isolation from Internal Circuit		Not isolated	Only communication interface part is isolated.	
Dielectric Strength		Between power and ⏚ terminals: 500V AC, 1 minute		
Insulation Resistance		Between power and ⏚ terminals: 10 MΩ minimum (500V DC megger)		
Noise Resistance		DC power terminals: 1.0 kV, 50 ns to 1 µs Expansion interface cable (coupling clamp): 1.5 kV, 50 ns to 1 µs		
Inrush Current		50A maximum (24V DC)		
Grounding Wire		UL1015 AWG22, UL1007 AWG18		
Power Supply Wire		UL1015 AWG22, UL1007 AWG18		
EMC Compliant Cable Length		—	1m (FC5A-KX1C)	
Power Supply Connector	Connector on Mother Board	MSTB2.5/3-GF-5.08BK (Phoenix Contact)	—	MKDSN1.5/3-5.08-BK (Phoenix Contact)
	Connector Insertion/ Removal Durability	100 times minimum	—	—
Expansion Cable Connector	Connector on Mother Board	—	FCN-365P024-AU (Fujitsu Component)	FCN-365P024-AU (Fujitsu Component)
	Connector Insertion/ Removal Durability	—	100 times minimum	100 times minimum
Effect of Improper Power Supply Connection		Reverse polarity: No operation, no damage Improper voltage: Permanent damage may be caused Improper lead connection: Permanent damage may be caused		
Effect of Improper Expansion Cable Connection		—	Reverse polarity: Permanent damage may be caused Improper voltage Permanent damage may be caused Improper lead connection: Permanent damage may be caused	
Weight		140g	70g	135g

Note 1: Power consumption by the expansion interface module and eight I/O modules

Note 2: The maximum number of relay outputs that can be turned on simultaneously is 54 points.

Error LED

The ERR LED on expansion interface modules flashes and turns on depending on the error condition.

Error LED	Description
Turns ON	When the CPU module has an error. When the scan time exceeds 1000 ms. (Do not set the constant scan time of special data register D8022 to longer than 1000 ms.)
Flashes (500ms period)	When the expansion interface module or the expansion interface slave module is not powered by the external power supply.
Flashes (1000ms period)	When an initialization error occurred in an I/O module connected to the right of the expansion interface module. When more than eight I/O modules are mounted to the right of the expansion interface module. When any module other than digital I/O modules is mounted to the right of the expansion interface module.

Note: When an AC input module is mounted to the right of the expansion interface module, the ERR LED does not turn on.

Special Data Register for Expansion Interface Module

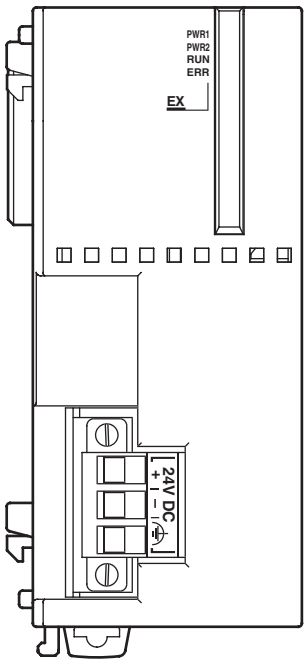
Slim type CPU modules have a special data register for the expansion interface module. Special data register D8252 stores the refresh time (in units of 100 μs) of additional expansion I/O modules mounted to the right of the expansion interface module.

DR No.	Data Register Function	DR Value Updated	R/W
D8252	Expansion interface module I/O refresh time (×100 μs)	Every scan	R

Expansion Interface Module Terminal Arrangement

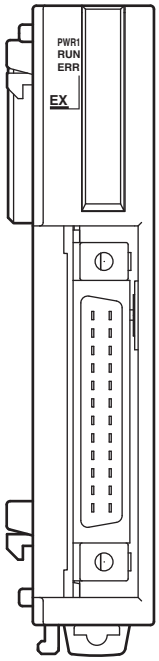
FC5A-EXM2 (Expansion Interface Module)

Applicable Terminal Block: MSTB2.5/3-GF-5.08BK (supplied with the expansion interface module)



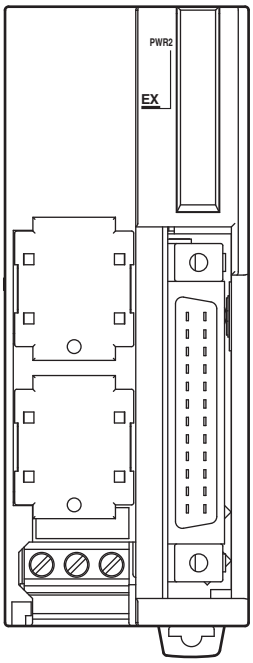
• For power wiring precautions, see page 2-77.

FC5A-EXM1M (Expansion Interface Master Module)



Applicable Cable: FC5A-KX1C

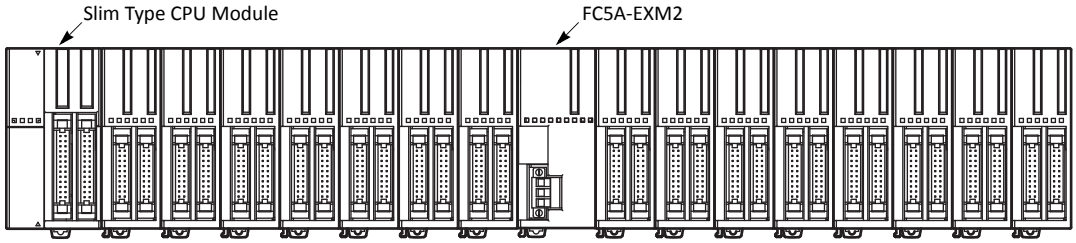
FC5A-EXM1S (Expansion Interface Slave Module)



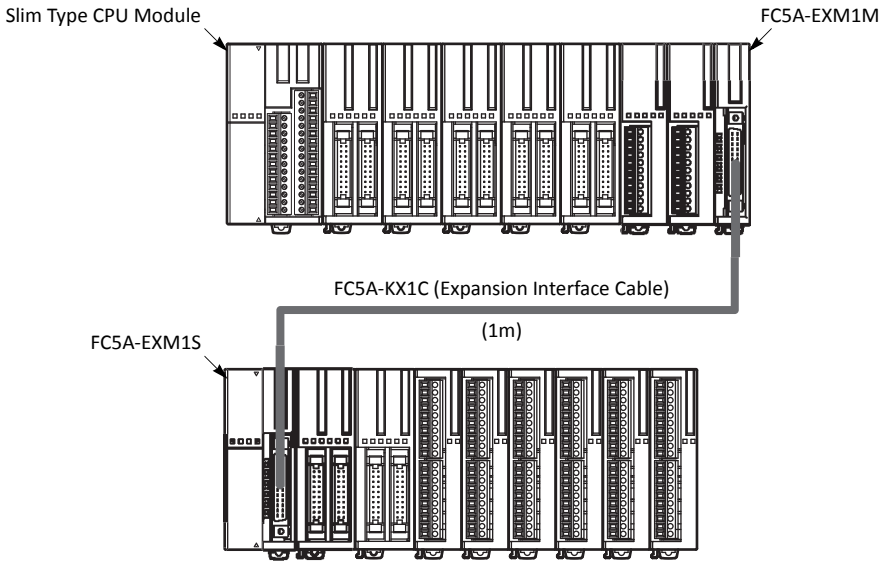
• For power wiring precautions, see page 2-77.

Expansion Interface Module System Setup

FC5A-EXM2 (Expansion Interface Module)



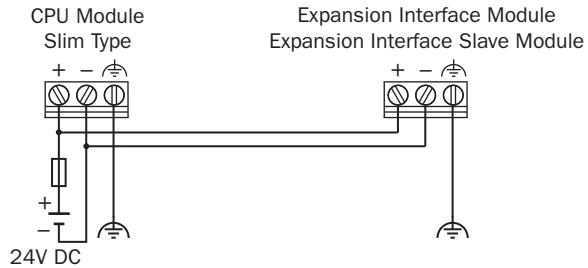
FC5A-EXM1M and FC5A-EXM1S (Expansion Interface Master and Slave Modules)



Notes:

- Use one power supply to power the CPU module and the expansion interface module or expansion interface slave module.
- When using a separate power supply, power up the expansion interface module or expansion interface slave module first, followed by the CPU module, otherwise the CPU module causes an error and cannot start and stop operation.
- Use the optional expansion interface cable FC5A-KX1C for connection between the expansion interface master and slave modules.
- If the expansion interface cable is disconnected during operation, the I/O modules connected to the expansion interface slave module are reset and all I/O points are turned off automatically. Then, turn off the power to the CPU module and the expansion interface slave module, connect the cable, and turn on the power again.
- Only one expansion interface module can be used with the CPU module.
- AC input module, analog I/O modules, expansion RS232C/RS485 communication modules, and AS-Interface master module cannot be connected to the right of the expansion interface module. When AC input module is connected, the ERR LED on the CPU module does not turn on. Make sure that AC input module is not connected to the right of the expansion interface module.

Power Supply Wiring Example



AS-Interface Master Module

The AS-Interface master module can be used with the all-in-one 24-I/O type and any slim type CPU modules to communicate digital data with slaves, such as sensor, actuator, and remote I/O data.

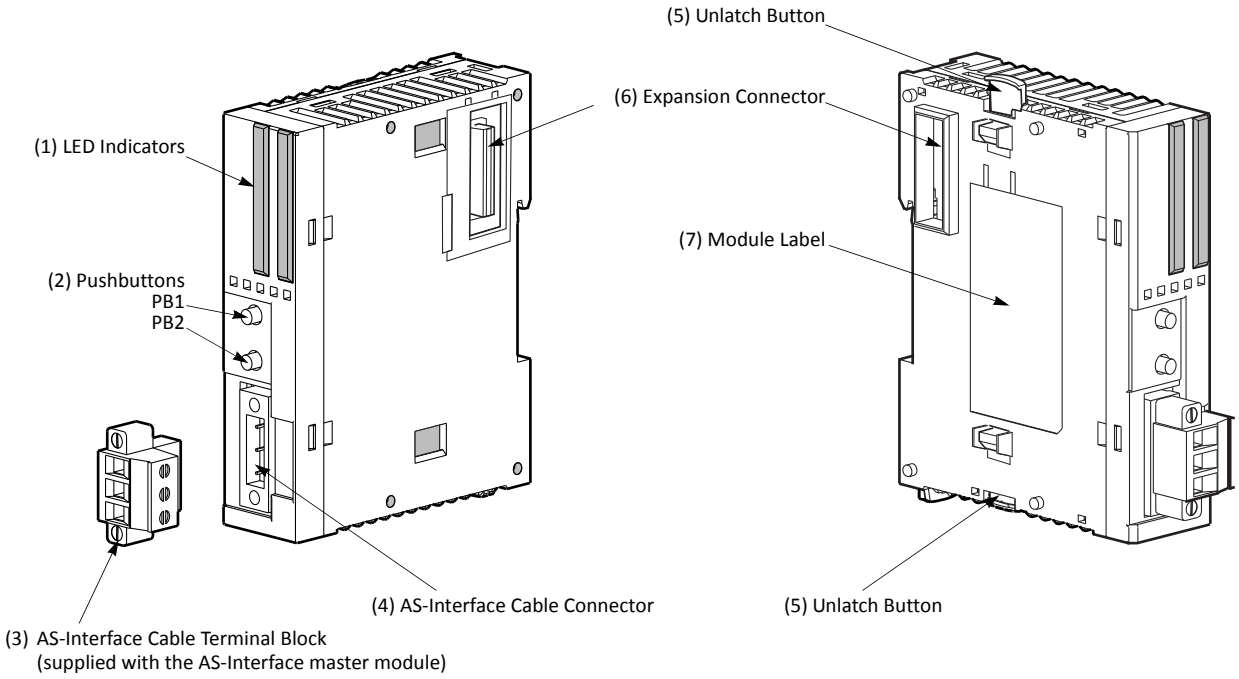
One or two AS-Interface master modules can be used with one CPU module. The AS-Interface master module can connect a maximum of 62 digital I/O slaves. A maximum of seven analog I/O slaves can also be connected to the AS-Interface master module (compliant with AS-Interface ver. 2.1 and analog slave profile 7.3).

For details about AS-Interface communication, see page 24-1 (Advanced Vol.).

AS-Interface Master Module Type Number

Module Name	Type No.
AS-Interface Master Module	FC4A-AS62M

Parts Description



(1) LED Indicators

Status LEDs:	Indicate the AS-Interface bus status.
I/O LEDs:	Indicate the I/O status of the slave specified by the address LEDs.
Address LEDs:	Indicate slave addresses.

(2) Pushbuttons Used to select slave addresses, change modes, and store configuration.

(3) AS-Interface Cable Terminal Block

Connects the AS-Interface cable.
One terminal block is supplied with the AS-Interface master module.
When ordering separately, specify Type No. FC4A-PMT3P and quantity (package quantity: 2).

(4) AS-Interface Cable Connector

Installs the AS-Interface cable terminal block.

(5) Unlatch Button Used to unlatch the AS-Interface master module from the CPU or I/O module.

(6) Expansion Connector Connects to the CPU and other I/O modules.

(7) Module Label Indicates the AS-Interface master module Type No. and specifications.

General Specifications (AS-Interface Module)

Operating Temperature	0 to 55°C (operating ambient temperature, no freezing)
Storage Temperature	–25 to +70°C (no freezing)
Relative Humidity	Level RH1, 30 to 95% (non-condensing)
Pollution Degree	2 (IEC 60664)
Degree of Protection	IP20
Corrosion Immunity	Free from corrosive gases
Altitude	Operation: 0 to 2,000m (0 to 6,565 feet) Transport: 0 to 3,000m (0 to 9,840 feet)
Vibration Resistance	When mounted on a DIN rail: 10 to 57 Hz amplitude 0.075 mm, 57 to 150 Hz acceleration 9.8 m/s^2 2 hours per axis on each of three mutually perpendicular axes When mounted on a panel surface: 2 to 25 Hz amplitude 1.6 mm, 25 to 100 Hz acceleration 39.2 m/s^2 90 minutes per axis on each of three mutually perpendicular axes
Shock Resistance	147 m/s^2, 11 ms duration, 3 shocks per axis, on three mutually perpendicular axes (IEC 61131)
External Power Supply	AS-Interface power supply, 29.5 to 31.6V DC
AS-Interface Current Draw	65 mA (normal operation) 110 mA maximum
Effect of Improper Input Connection	No damage
Connector on Mother Board	MSTB2.5/3-GF-5.08BK (Phoenix Contact)
Connector Insertion/Removal Durability	100 times minimum
Internal Current Draw	80 mA (5V DC) 0 mA (24V DC)
AS-Interface Master Module Power Consumption	540 mW
Weight	85g

Communication Specifications (AS-Interface Module)

Maximum Bus Cycle		When 1 through 19 slaves are connected: 3 ms When 20 through 62 slaves are connected: 0.156 × (1 + N) ms where N is the number of active slaves 5 ms maximum when 31 standard or A/B slaves are connected 10 ms maximum when 62 A/B slaves are connected	
Maximum Slaves	(Note)	Standard slaves: 31 A/B slaves: 62 When using a mix of standard slaves and A/B slaves together, the standard slaves can only use addresses 1(A) through 31(A). Also, when a standard slave takes a certain address, the B address of the same number cannot be used for A/B slaves.	
Maximum I/O Points	(Note)	Standard slaves: 248 total (124 inputs + 124 outputs) A/B slaves: 434 total (248 inputs + 186 outputs)	
Maximum Cable Length		AS-Interface cable 2-wire flat cable	When using no repeater or extender: 100m When using a total of 2 repeaters or extenders: 300m
		Single wires	200 mm
Rated Bus Voltage		30V DC	

Note: When using two AS-Interface modules, these quantities are doubled.

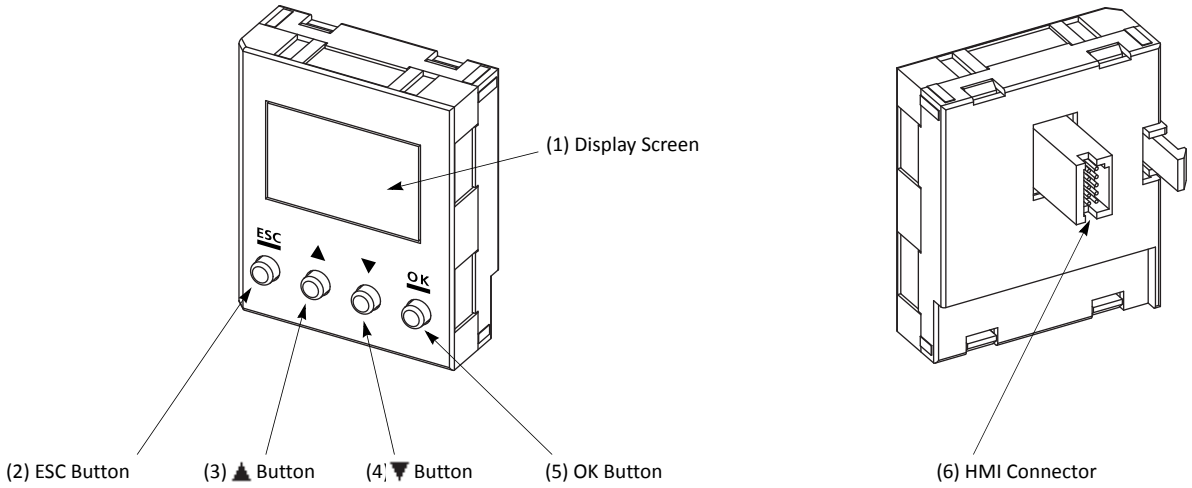
HMI Module

The optional HMI module can mount on any all-in-one type CPU module, and also on the HMI base module mounted next to any slim type CPU module. The HMI module makes it possible to manipulate the RAM data in the CPU module without using the Online menu options in WindLDR. For details about operating the HMI module, see page 5-60. For installing and removing the HMI module, see pages 3-3 and 3-4.

HMI Module Type Number

Module Name	Type No.
HMI Module	FC4A-PH1

Parts Description



(1) Display Screen	The liquid crystal display shows menus, devices, and data.
(2) ESC Button	Cancels the current operation, and returns to the immediately preceding operation.
(3) ▲ Button	Scrolls up the menu, or increments the selected device address or value.
(4) ▼ Button	Scrolls down the menu, or decrements the selected device address or value.
(5) OK Button	Goes into each control screen, or enters the current operation.
(6) HMI Connector	Connects to the all-in-one CPU module or HMI base module.

HMI Module Specifications

Type No.	FC4A-PH1
Power Voltage	5V DC (supplied from the CPU module)
Internal Current Draw	200 mA DC
Weight	20g

⚠ Caution

- Turn off the power to the MicroSmart before installing or removing the HMI module to prevent electrical shocks and damage to the HMI module.
- Do not touch the connector pins with hand, otherwise contact characteristics of the connector may be impaired.

HMI Base Module

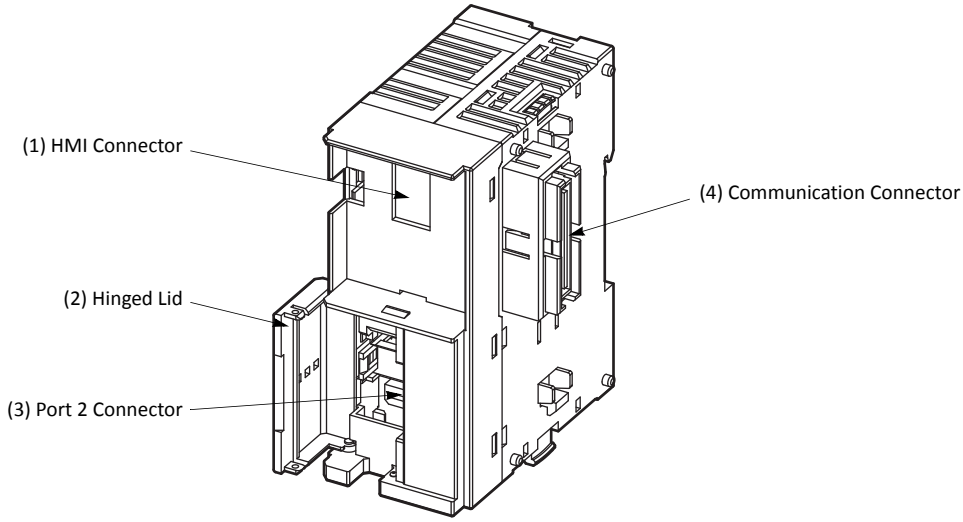
The HMI base module is used to install the HMI module when using the slim type CPU module. The HMI base module also has a port 2 connector to attach an optional RS232C or RS485 communication adapter.

When using the all-in-one type CPU module, the HMI base module is not needed to install the HMI module.

HMI Base Module Type Number

Module Name	Type No.
HMI Base Module	FC4A-HPH1

Parts Description



(1) HMI Connector	For installing the HMI module.
(2) Hinged Lid	Open the lid to gain access to the port 2 connector.
(3) Port 2 Connector	For installing an optional RS232C or RS485 communication adapter.
(4) Communication Connector	Connects to the slim type CPU module.

Communication Adapters and Communication Modules

All MicroSmart CPU modules have communication port 1 for RS232C communication. In addition, all-in-one type CPU modules have a port 2 connector. An optional communication adapter can be installed on the port 2 connector for RS232C or RS485 communication.

A communication module can be attached to any slim type CPU module to use port 2 for additional RS232C or RS485 communication. When the HMI base module is attached to a slim type CPU module, a communication adapter can be installed to the port 2 connector on the HMI base module.

When using the RS232C communication adapter or communication module for port 2, maintenance communication, user communication, and modem communication are made possible. With the RS485 communication adapter or communication module installed, maintenance communication, user communication, data link communication, and Modbus master and slave communication can be used on port 2.

Communication Adapter and Communication Module Type Numbers

Name	Termination	Type No.
RS232C Communication Adapter	Mini DIN connector	FC4A-PC1
RS485 Communication Adapter	Mini DIN connector	FC4A-PC2
	Screw Terminal Block	FC4A-PC3
RS232C Communication Module	Mini DIN connector	FC4A-HPC1
RS485 Communication Module	Mini DIN connector	FC4A-HPC2
	Screw Terminal Block	FC4A-HPC3

Communication Adapter and Communication Module Specifications

Type No.	FC4A-PC1 FC4A-HPC1	FC4A-PC2 FC4A-HPC2	FC4A-PC3 FC4A-HPC3
Standards	EIA RS232C	EIA RS485	EIA RS485
Communication Method	Asynchronous	Asynchronous	Asynchronous
Port No.	2	2	2
Maximum Connectable Quantity	1	1	1
Maximum Baud Rate	115,200 bps (Note 1)	115,200 bps (Note 1)	115,200 bps (Note 1)
Maintenance Communication (Computer Link)	Possible	Possible	Possible
User Communication	Possible	Possible	Possible
Modem Communication	Possible	—	—
Data Link Communication	—	Possible (31 slaves max.) (Note 2)	Possible (31 slaves max.) (Note 2)
Modbus ASCII/RTU Communication	Possible	Possible	Possible
Modbus TCP Communication (Note 3)	Possible	Possible	Possible
Maximum Cable Length	Special cable (Note 4)	Special cable (Note 4)	200m (Note 5)
Isolation between Internal Circuit and Communication Port	Not isolated	Not isolated	Not isolated

Note 1: Maximum baud rate is 57,600 bps when using CPU modules apart from for FC5A-D12K1E/S1E.

Note 2: Maximum baud rate when using data link communication is 57,600 bps.

Note 3: Though Modbus TCP communication cannot be used on port 2 of FC5A-D12K1E and FC5A-D12S1E, it can be used on the built-in Ethernet port.

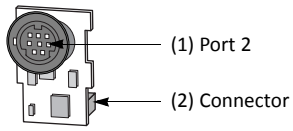
Note 4: For special cables, see page A-12.

Note 5: Recommended cable for RS485: Twisted-pair shielded cable with a minimum core wire of 0.3 mm^2.
Conductor resistance 85 Ω/km maximum, shield resistance 20 Ω/km maximum.

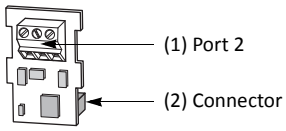
The proper tightening torque of the terminal screws on the RS485 communication adapter and RS485 communication module is 0.22 to 0.25 N·m. For tightening the screws, use screwdriver SZS 0,4 x 2,5 (Phoenix Contact).

Parts Description

RS232C Communication Adapter (Mini DIN)
RS485 Communication Adapter (Mini DIN)

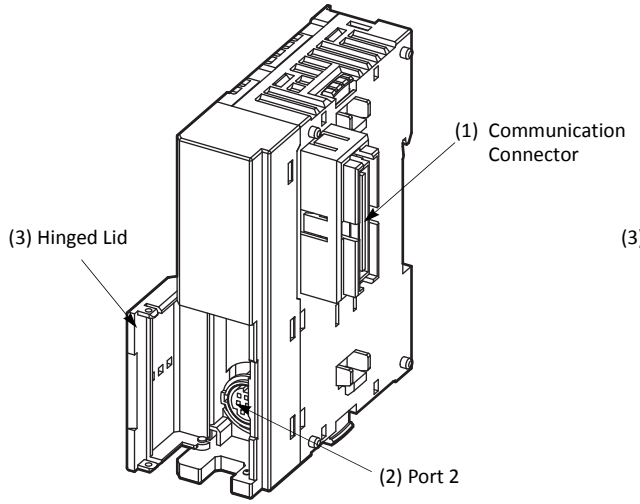


RS485 Communication Adapter (Screw Terminal)

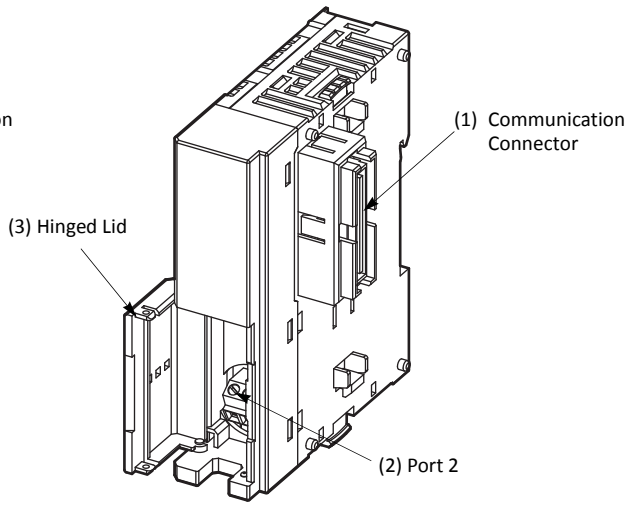


(1) Port 2 RS232C or RS485 communication port 2.
(2) Connector Connects to the port 2 connector on the all-in-one type CPU module or HMI base module.

RS232C Communication Module (Mini DIN)
RS485 Communication Module (Mini DIN)



RS485 Communication Module (Screw Terminal)



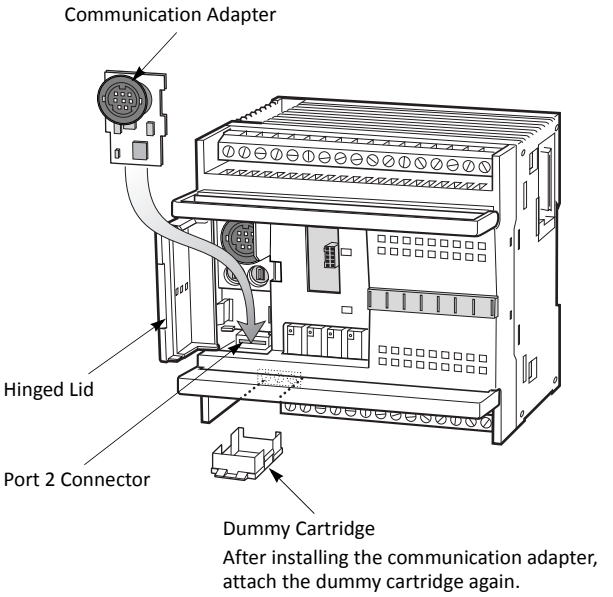
(1) Communication Connector Connects to the slim type CPU module.
(2) Port 2 RS232C or RS485 communication port 2.
(3) Hinged Lid Open the lid to gain access to port 2.

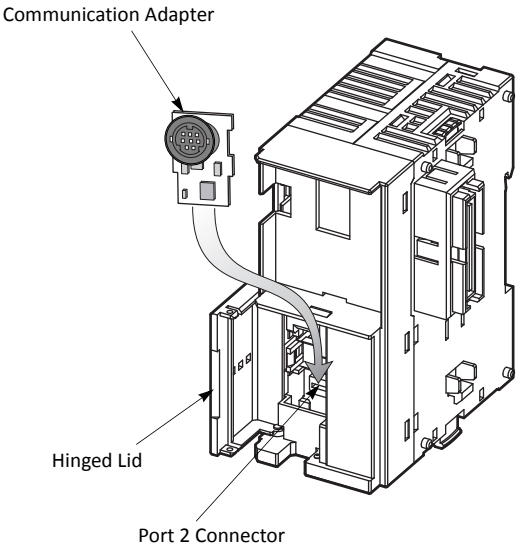
Installing the Communication Adapter and Communication Module

> **⚠ Caution**
> • Before installing the communication adapter or communication module, turn off the power to the MicroSmart CPU module. Otherwise, the communication adapter or CPU module may be damaged, or the MicroSmart may not operate correctly.

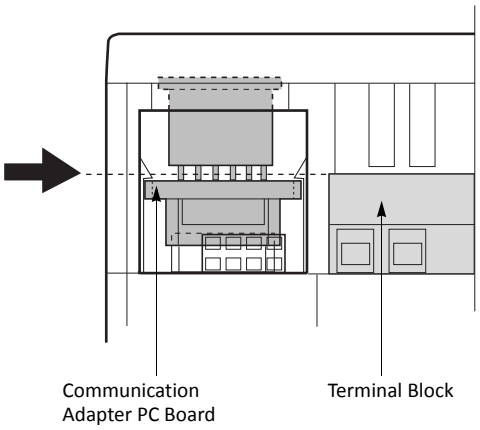
Communication Adapter

To install the communication adapter on the all-in-one type CPU module, open the hinged lid and remove the dummy cartridge. Push the communication adapter into the port 2 connector from the front until it bottoms and is secured by the latches. Similarly, when installing the communication adapter on the HMI base module, open the hinged lid, and push the communication adapter into the port 2 connector from the front until it bottoms and is secured by the latches.





After installing the communication adapter on an all-in-one type CPU module, view the communication adapter through the dummy cartridge opening, and check to see that the PC board of the communication adapter is in a lower level than the top of the terminal block.

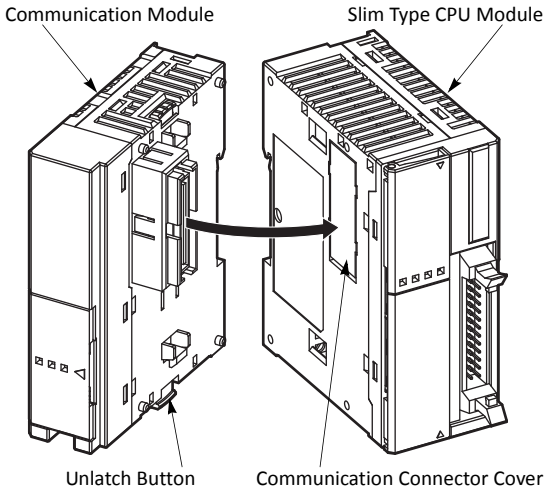


Communication Module

When installing a communication module on the slim type CPU module, remove the communication connector cover from the slim type CPU module. See page 3-7.

Place the communication module and CPU module side by side. Put the communication connectors together for easy alignment.

With the communication connectors aligned correctly and the blue unlatch button in the down position, press the communication module and CPU module together until the latches click to attach the modules together firmly. If the unlatch button is in the up position, push down the button to engage the latches.



Removing the Communication Adapter and Communication Module

⚠ Caution

- Before removing the communication adapter or communication module, turn off the power to the MicroSmart CPU module. Otherwise, the communication adapter or CPU module may be damaged, or the MicroSmart may not operate correctly.

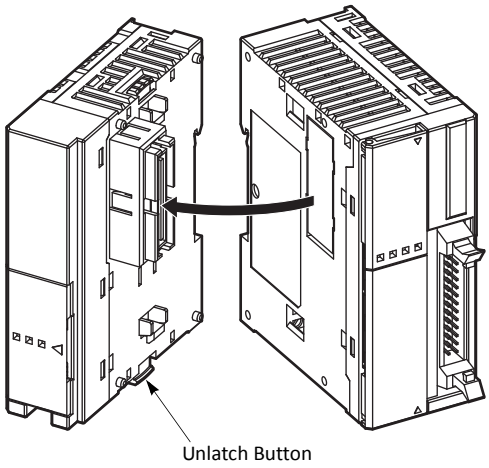
Communication Adapter

To remove the communication adapter from the all-in-one type CPU module, first remove the dummy cartridge. While pushing up the communication adapter PC board with a finger through the dummy cartridge opening, disengage the latches from the communication adapter using a flat screwdriver. Pull out the communication adapter from the port 2 connector. When removing the communication adapter from the HMI module, take similar steps.

Communication Module

If the modules are mounted on a DIN rail, first remove the modules from the DIN rail as described on page 3-8.

Push up the blue unlatch button to disengage the latches, and pull the modules apart as shown on the right.

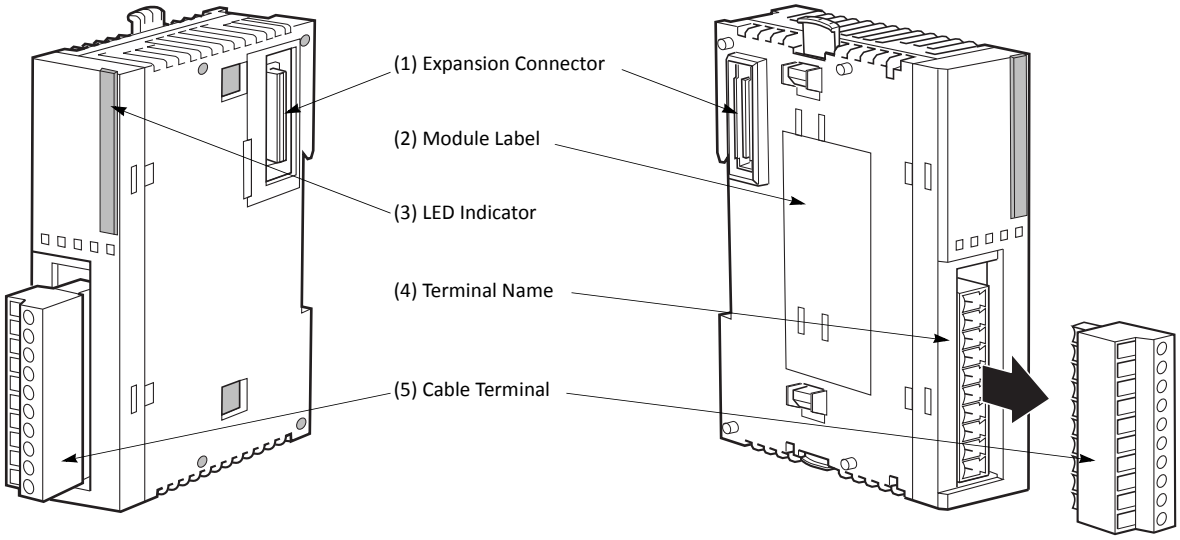


Expansion RS232C/RS485 Communication Modules

The expansion RS232C/RS485 communication modules can be attached to the CPU modules to add RS232C or RS485 communication port 3 through port 7. The FC5A-SIF2 expansion RS232C communication module is an expansion module used with CPU modules system program version 110 or higher. The FC5A-SIF4 expansion RS485 communication module is an expansion module used with CPU modules system program version 220 or higher.

For details about expansion RS232C/RS485 communication, see page 25-1 (Advanced Vol.).

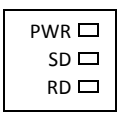
Parts Description



(1) Expansion Connector Connects to the CPU and other I/O modules.
(All-in-one 10- and 16-I/O type CPU modules cannot be connected.)

(2) Module Label Indicates the expansion RS232C/RS485 communication module Type No. and specifications. Expansion RS232C/RS485 communication modules have the version number indicated on the module label attached to the side of the module. Confirm the version number because some specifications differ depending on the version number. For the position of the version number printed on the module label, see page 2-56.

(3) LED Indicators



PWR: Turns on when this module is powered up.
Flashes when the power supply to FC5A-SIF4 is insufficient.

SD: Turns on when this module is sending data.

RD: Turns on when this module is receiving data.

(4) Terminal Name Indicates terminal names.

(5) Cable Terminal Screw terminals for wiring.

Expansion RS232C/RS485 Communication Module Specifications

General Specifications

Type No.		FC5A-SIF2	FC5A-SIF4
Quantity of Channels		1	
Synchronization		Start-stop synchronization	
Electrical Characteristics		EIA RS232C compliant	EIA RS485 compliant
Terminal Arrangement		See page 2-89.	See page 2-90.
Operating Temperature		0 to 55°C	
Relative Humidity		10 to 95% (no condensation)	
Cable Specifications	**Cable Type**	Shielded multi-core cable 24AWG x 6	Shielded twisted-pair cable with a minimum core wire of 0.3 mm^2 (AWG22)
	Dielectric strength	2000 V/min	700V AC/min
	Insulation resistance	100 MΩ/km	
Maximum Cable Length		3m	1200m
Maximum Nodes		2 (1:1 Communication)	32
Connector on Mother Board		MC1.5/10-G-3.81BK (Phoenix Contact) Applicable terminal block:FC4A-PMT10P	
Connector Insertion/Removal Durability		100 times minimum	
Isolation from Internal Circuit		Transformer isolated	
Effect of Improper Input Connection	**Incorrect Wiring**	Malfunction may be caused.	
	Improper Voltage	If any input exceeding the rated value is applied, permanent damage may be caused.	
Dielectric Strength		Between communication terminals and internal circuit: 500V AC, 1 minute	
Quantity of Applicable Expansion RS232C/ RS485 Communication Modules		All-in-one 24-I/O type CPU module:3 maximum Slim type CPU module:5 maximum	
Internal Current Draw		40 mA [85 mA](5V DC) 40 mA [0 mA] (24V DC)	40 mA (5V DC) 40 mA (24V DC)
Weight		100g	

Notes:

- The quantity of expansion RS232C/RS485 communication modules is the total number of FC5A-SIF2 and FC5A-SIF4 connected to the CPU module.
- The stability of communication depends on the quantity of the connected expansion RS232C/RS485 communication modules, the cable length, and the communication speed. If communication is unstable, confirm and adjust those factors.
- Values indicated in square brackets represent FC5A-SIF2 earlier than version 200.

Communication Specifications

Type No.		FC5A-SIF2	FC5A-SIF4
Communication Parameters	Baud Rate (bps)	1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 (Note 1)	1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200
	Data Bits	7 or 8	
	Parity	Even, Odd, None	
	Stop Bits	1 or 2	
Protocol (Note 3)	Maintenance Communication	Possible (Note 2)	Possible (Note 2)
	User Communication	Possible	Possible
	Data Link	—	Possible
	Modbus Communication	Possible (Note 4)	Possible
	Modem Communication	—	—

Note 1: 57600 and 115200 bps are supported with version 200 or higher.

Note 2: Transfer mode must be set to ASCII to download or upload user program. Run-time program download cannot be used.

Note 3: The communication protocols that can be used depend on the system program version of the CPU module and the version of the connected expansion RS232C/RS485 communication modules. For the combination of the version numbers and supported protocols, see page A-17.

Note 4: Modbus communication is supported with version 200 or higher.

Data Communication Processing Time

The CPU module processes data communication with expansion RS232C/RS485 communication modules in the END processing every scan. The CPU module also processes data communication during the scan when COMRF instructions are executed or every 10 ms when “Every 10 ms” under “Communication Refresh for Port 3 through port 7” is selected in the Function Area Settings dialog.

One expansion RS232C/RS485 communication module requires a communication processing time shown in the table below. Therefore, when an expansion RS232C/RS485 communication module sends or receives communication, the scan time extends accordingly.

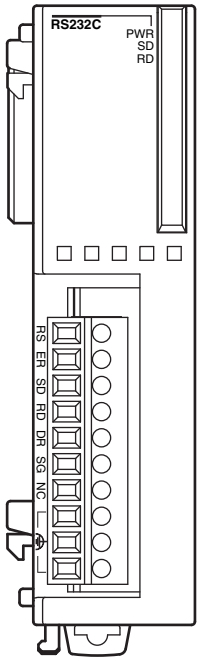
CPU Module system program version	Expansion RS232C/RS485 Communication Module version	Maximum Delay in One Scan (Note 1)
Earlier than 220	Earlier than 200	Approx. 4 ms
	200 or higher	
220 or higher	Earlier than 200	
	200 or higher	Approx. 10 ms

Note 1: The values are the maximum delay of scan time when one expansion RS232C/RS485 communication module performs communication. When multiple expansion RS232C/RS485 communication modules perform communication at the same time, the delay is multiplied by the quantity of the expansion RS232C/RS485 communication modules.

Expansion RS232C Communication Module Terminal Arrangement and Wiring Diagrams

FC5A-SIF2 — Screw Terminal Type

Applicable Terminal Block: **FC4A-PMT10P (supplied with the expansion RS232C communication module)**



Terminal	I/O	Description
RS (RTS)	Output	Request to Send (constant voltage terminal)
ER (DTR)	Output	Data Terminal Ready
SD (TXD)	Output	Transmit Data
RD (RXD)	Input	Receive Data
DR (DSR)	Input	Data Set Ready
SG (SG)	—	Signal Ground
NC	—	—
⏚	—	Functional ground
⏚	—	Functional ground
⏚	—	Functional ground

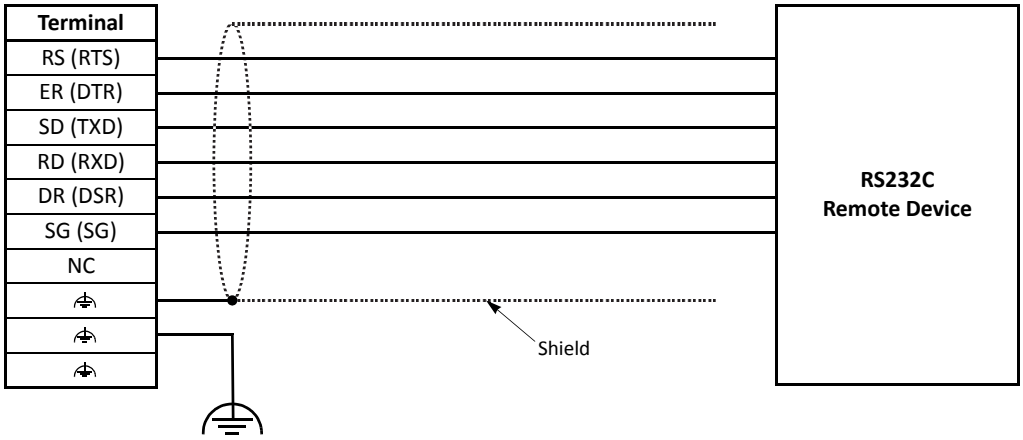
Note: The ⏚ terminals can be used as junction terminals of functional ground.

Wiring Example

Caution

- Use a recommended cable or a similar shielded cable for wiring the expansion RS232C communication terminals. For the recommended cable, see page 2-87 and prepare the cable.
- When the expansion RS232C communication module may malfunction due to external noise, connect the shield of the cable to a proper ground.
- Before wiring, read the user's manual for the remote device connected to the expansion RS232C communication module.

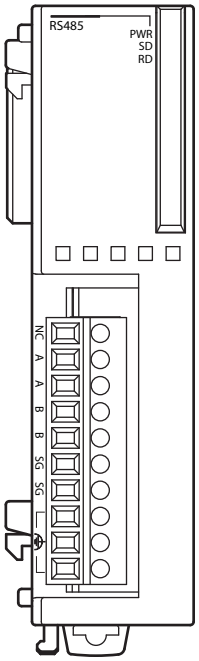
FC5A-SIF2



Expansion RS485 Communication Module Terminal Arrangement and Wiring Diagrams

FC5A-SIF4 — Screw Terminal Type

Applicable Terminal Block: FC4A-PMT10P (supplied with the expansion RS485 communication module)



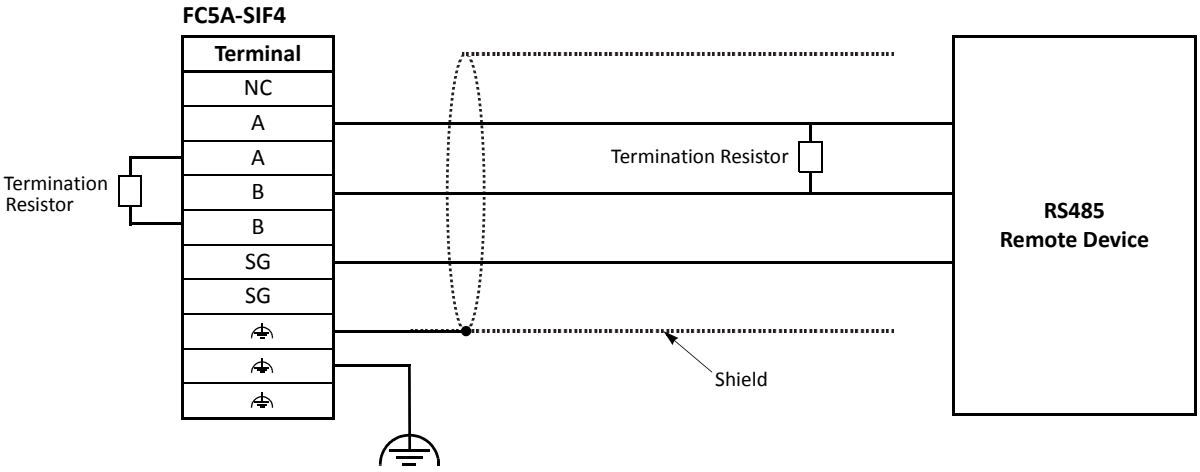
Terminal	I/O	Description
NC	—	—
A	Input and Output	Data A
A	Input and Output	Data A
B	Input and Output	Data B
B	Input and Output	Data B
SG	—	Signal Ground
SG	—	Signal Ground
⏚	—	Functional ground
⏚	—	Functional ground
⏚	—	Functional ground

- Two A terminals are interconnected.
- Two B terminals are interconnected.
- Two SG terminals are interconnected.
- Three ⏚ terminals are interconnected. The ⏚ terminals can be used as junction terminals of functional ground.

Wiring Example

Caution

- Use a recommended cable or a similar shielded cable for wiring the expansion RS485 communication terminals. For the recommended cable, see page 2-87 and prepare the cable.
- When the expansion RS485 communication module may malfunction due to external noise, connect the shield of the cable to a proper ground.
- Before wiring, read the user's manual for the remote device connected to the expansion RS485 communication module.
- Insert appropriate termination resistors matched to the characteristic impedance of the cable. When the recommended cable is used, insert 100Ω 1/2W resistors.



Memory Cartridge

A user program can be stored on an optional memory cartridge installed on a MicroSmart CPU module from a computer running WindLDR, and the memory cartridge can be installed on another MicroSmart CPU module of the same type. Using a memory cartridge, the CPU module can exchange user programs without using a computer.

User programs can be uploaded and downloaded between a memory cartridge and WindLDR, and downloaded from a memory cartridge to the CPU module. These features are available on all models of FC5A CPU modules.

In addition, a use program can be uploaded from the CPU module to a memory cartridge. This feature is available on CPU modules with system program version 200 or higher.

Memory Cartridge Type Number

Module Name	Type No.
32KB Memory Cartridge	FC4A-PM32
64KB Memory Cartridge	FC4A-PM64
128KB Memory Cartridge	FC4A-PM128

User Program Execution Priority

Depending whether a memory cartridge is installed on the MicroSmart CPU module or not, a user program stored on the memory cartridge or on the CPU module EEPROM is executed, respectively.

Memory Cartridge	User Program Execution Priority
Installed on the CPU Module	When a memory cartridge is installed on the CPU module, the user program stored in the memory cartridge is executed. The memory cartridge download function makes it possible to download the user program in the memory cartridge to the CPU module. The memory cartridge upload function makes it possible to upload the user program from the CPU module and store it in the memory cartridge.
Not installed on the CPU Module	The user program stored on the EEPROM in the CPU module is executed.

Memory Cartridge Specifications

Type No.	FC4A-PM32	FC4A-PM64	FC4A-PM128
Memory Type	EEPROM		
Accessible Memory Capacity	32 KB	64 KB	128 KB
Hardware for Storing Data	CPU module		
Software for Storing Data	WindLDR		
Quantity of Stored Programs	One user program can be stored on one memory cartridge.		

Note: The optional clock cartridge (FC4A-PT1) and the memory cartridge cannot be used together on the all-in-one type CPU module. The clock cartridge and the memory cartridge can be used together on the slim type CPU module.

User Program Compatibility

The CPU module can execute only user programs created for the same CPU module type. When installing a memory cartridge, make sure that the user program stored on the memory cartridge matches the CPU module type. If the user program is not for the same CPU module type, a user program syntax error occurs and the CPU module cannot run the user program.

⚠ Caution

- **Compatibility of User Program with CPU Modules**
  When a memory cartridge contains a user program for higher functionality, do not install the memory cartridge into CPU modules with lower functionality, otherwise the user program is not executed correctly. Make sure that the user program in the memory cartridge is compatible with the CPU module.

Downloading and Uploading User Program to and from Memory Cartridge Using WindLDR

When a memory cartridge is installed on the CPU module, a user program is downloaded to and uploaded from the memory cartridge using WindLDR on a computer. When a memory cartridge is not installed on the CPU module, a user program is downloaded to and uploaded from the CPU module. For the procedures to download a user program from WindLDR on a computer, see page 4-11.

With a memory cartridge installed on a CPU module, if the user program stored on the memory cartridge does not match the CPU module type, downloading is possible, but uploading is not possible. To upload a user program, make sure that the existing user program stored on the memory cartridge matches the CPU module type. Downloading is always possible to new blank memory cartridges installed on any type of CPU modules.

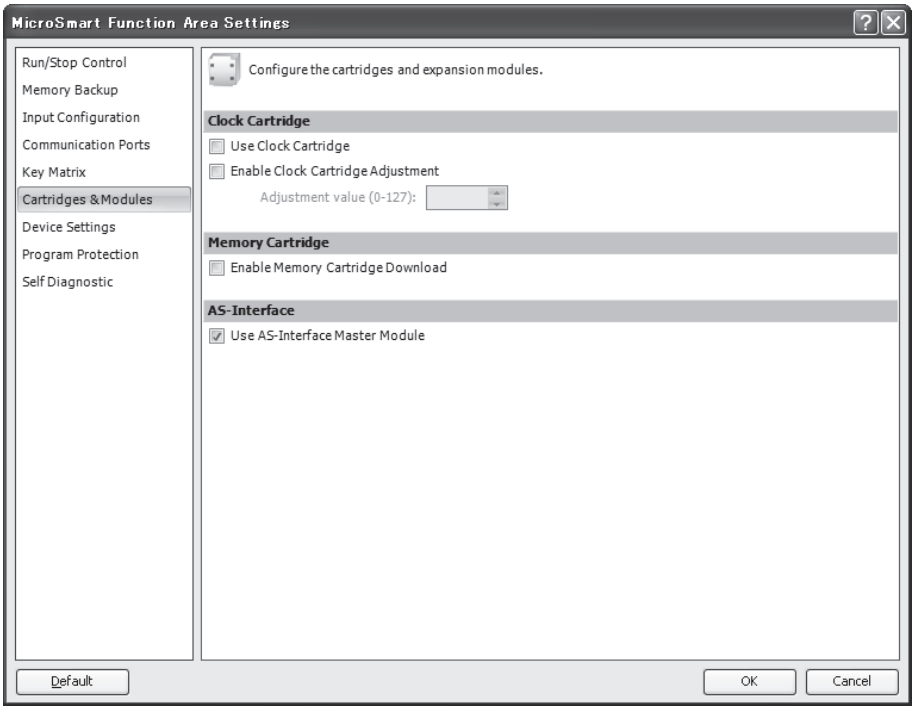
Downloading User Program from Memory Cartridge to the CPU Module

To designate user program download from the memory cartridge, install a memory cartridge on the CPU module connected to a PC, and power up the CPU module.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Cartridges & Modules**.

The Function Area Settings dialog box for Cartridges & Modules appears.



2. Under **Memory Cartridge**, click the check box to the left of **Enable Memory Cartridge Download**.

Checked: The user program is downloaded from the memory cartridge to the CPU module.

Unchecked: The user program is not downloaded from the memory cartridge to the CPU module.

3. Click the **OK** button.

4. Download the user program to the memory cartridge to complete the designation in the memory cartridge.

5. Shut down the CPU module and remove the memory cartridge. Install the memory cartridge on another CPU module. Power up the CPU module, then the user program is downloaded from the memory cartridge to the CPU module.

If the user program in the CPU module is write-protected or read/write-protected, the user program can be downloaded only when the password in the memory cartridge matches the password in the CPU module. For user program protection password, see page 5-44.

Memory Cartridge Upload

The user program in the MicroSmart CPU module can be uploaded and stored to a memory cartridge installed on the CPU module. In order to enable user program upload, the memory cartridge has to be configured using WindLDR. When the configured memory cartridge is installed on the CPU module and the CPU module is powered up, the user program is uploaded from the CPU module and stored to the memory cartridge.

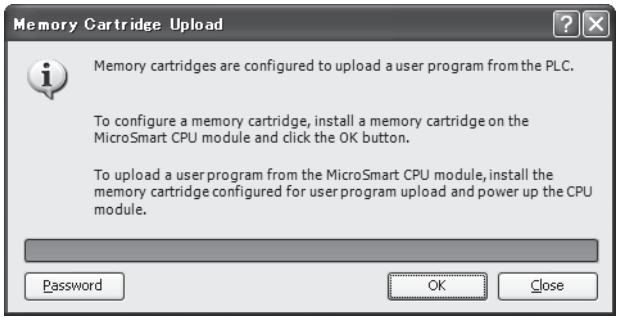
The configured memory cartridge can upload a user program only once because the user program upload configuration of the memory cartridge is cleared when the memory cartridge stores the uploaded user program.

Memory cartridge upload can be used on CPU modules with system program version 200 or higher.

Programming WindLDR

1. Install a memory cartridge on a CPU module. Connect the CPU module to the PC and power up the CPU module.
2. From the WindLDR menu bar, select **Online** > **Upload** > **Memory Cartridge Upload**.

The Memory Cartridge Upload dialog box appears.



3. If the user program to upload from the CPU module is read-protected with a password, click the **Password** button.

The Password Setting dialog box appears. Enter the same password. When finished, press the **OK** button and return to the Memory Cartridge Upload dialog box.

4. On the Memory Cartridge Upload dialog box, click the **OK** button to configure the memory cartridge for user program upload. Then, the user program stored on the memory cartridge is cleared.
5. Turn off the power to the CPU module and remove the memory cartridge from the CPU module. The memory cartridge has been configured for user program upload.
6. Install the memory cartridge to a CPU module of the same type and power up the CPU module. The user program in the CPU module is uploaded and stored to the memory cartridge.

Notes:

User program writing error occurs and the user program is not uploaded to the memory cartridge, turning on the ERR LED on the CPU module and stopping the CPU operation in the following cases:

- If the configured memory cartridge is installed on a different type of CPU module or installed on a CPU module with system program version lower than 200, user program writing error occurs when the CPU module is powered up. System program version 200 or higher is needed for configuring memory cartridges and uploading user programs.
- If the configured memory cartridge is a 32KB memory cartridge (FC4A-PM32) and is installed on a CPU module containing a user program of larger than 30,000 bytes, user program writing error occurs when the CPU module is powered up. A 32KB memory cartridge can upload a user program of 30,000 bytes maximum.
- If the user program in the CPU module is read-prohibited, the user program cannot be uploaded to the memory cartridge. If the user program in the CPU module is read-protected and the passwords do not match between the user programs in the memory cartridge and the CPU module, user program writing error occurs when the CPU module is powered up. For the user program protection, see page 5-44.

Installing and Removing the Memory Cartridge

⚠ Caution

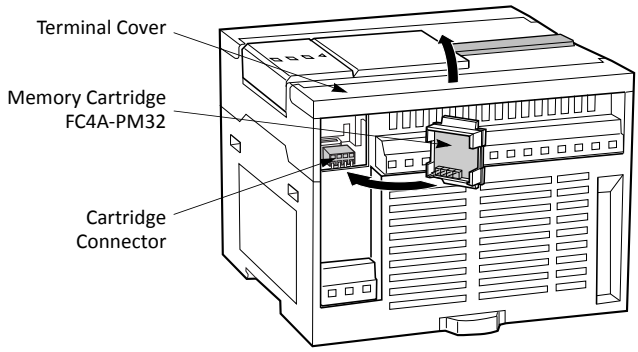
- Before installing or removing the memory cartridge, turn off the power to the MicroSmart CPU module. Otherwise, the memory cartridge or CPU module may be damaged, or the MicroSmart may not operate correctly.
- Do not touch the connector pins with hand, otherwise electrostatic discharge may damage the internal elements.

All-in-One Type CPU Module

The cartridge connector is normally closed with a dummy cartridge. To install the memory cartridge, open the terminal cover and remove the dummy cartridge from the CPU module. Make sure of correct orientation of the memory cartridge. Insert the memory cartridge into the cartridge connector until it bottoms. Do not insert the memory cartridge diagonally, otherwise the terminal pins will be deformed.

After installing the memory cartridge, close the terminal cover.

To remove the memory cartridge, hold both edges of the memory cartridge and pull it out.

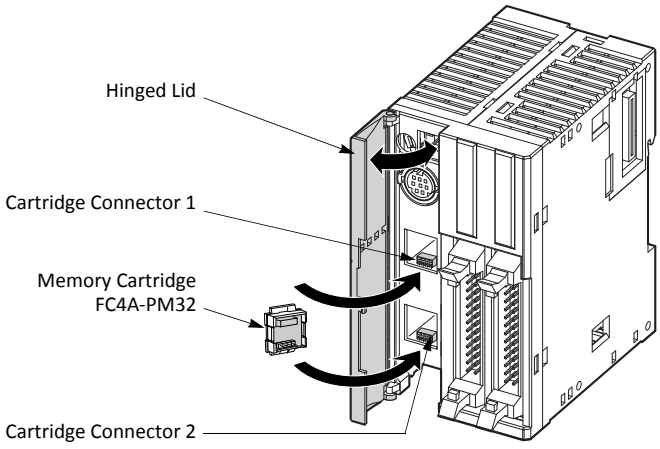


Slim Type CPU Module

Cartridge connectors 1 and 2 are normally closed with a dummy cartridge. To install the memory cartridge, open the hinged lid and remove the dummy cartridge from the CPU module. Make sure of correct orientation of the memory cartridge, and insert the memory cartridge into cartridge connector 1 or 2 until it bottoms. After installing the memory cartridge, close the hinged lid.

Only one memory cartridge can be installed to either cartridge connector 1 or 2 on the slim type CPU module. A memory cartridge and a clock cartridge can be installed at the same time.

To remove the memory cartridge, hold both edges of the memory cartridge and pull it out.



Clock Cartridge

With the optional clock cartridge installed on any type of MicroSmart CPU modules, the MicroSmart can be used for time-scheduled control such as illumination and air conditioners. For setting the calendar/clock, see page 9-6 (Advanced Vol.).

Clock Cartridge Type Number

Module Name	Type No.
Clock Cartridge	FC4A-PT1

Clock Cartridge Specifications

Accuracy	±30 sec/month (typical) at 25°C
Backup Duration	Approx. 30 days (typical) at 25°C after backup battery fully charged
Battery	Lithium secondary battery
Charging Time	Approx. 10 hours for charging from 0% to 90% of full charge
Battery Life	Approx. 100 recharge cycles after discharging down to 10% of full charge
Replaceability	Not possible to replace battery

The optional memory cartridge (FC4A-PM32) and the clock cartridge cannot be used together on the all-in-one type CPU module. The memory cartridge and the clock cartridge can be used together on the slim type CPU module.

Installing and Removing the Clock Cartridge

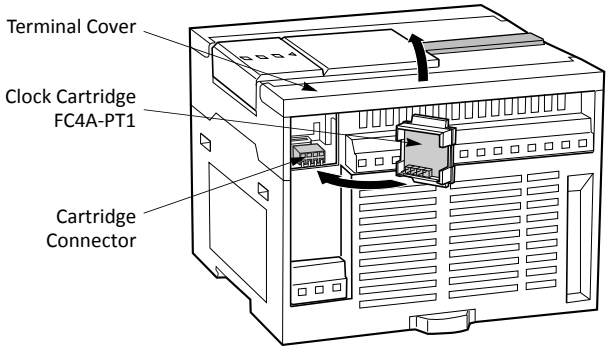
⚠ Caution

- Before installing or removing the clock cartridge, turn off the power to the MicroSmart CPU module. Otherwise, the clock cartridge or CPU module may be damaged, or the MicroSmart may not operate correctly.
- After installing the clock cartridge, set the calendar/clock using WindLDR. If the calendar/clock is set before installing the clock cartridge, clock IC error occurs, turning on the ERR LED.

All-in-One Type CPU Module

The cartridge connector is normally closed with a dummy cartridge. To install the clock cartridge, open the terminal cover and remove the dummy cartridge from the CPU module. Make sure of correct orientation of the clock cartridge. Insert the clock cartridge into the cartridge connector until it bottoms. Do not insert the clock cartridge diagonally, otherwise the terminal pins will be deformed. After installing the clock cartridge, close the terminal cover.

To remove the clock cartridge, hold both edges of the clock cartridge and pull it out.

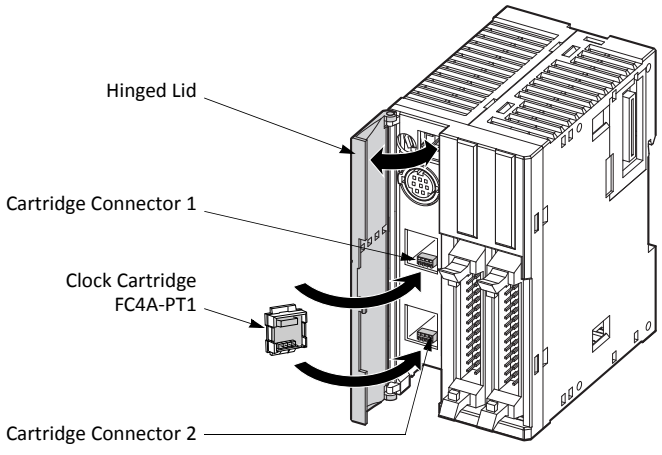


Slim Type CPU Module

To install the clock cartridge, open the hinged lid and remove the dummy cartridge from the CPU module. Make sure of correct orientation of the clock cartridge, and insert the clock cartridge into cartridge connector 1 or 2 until it bottoms. After installing the clock cartridge, close the hinged lid.

Only one clock cartridge can be installed to either cartridge connector 1 or 2 on the slim type CPU module. A clock cartridge and a memory cartridge can be installed at the same time.

To remove the clock cartridge, hold both edges of the clock cartridge and pull it out.

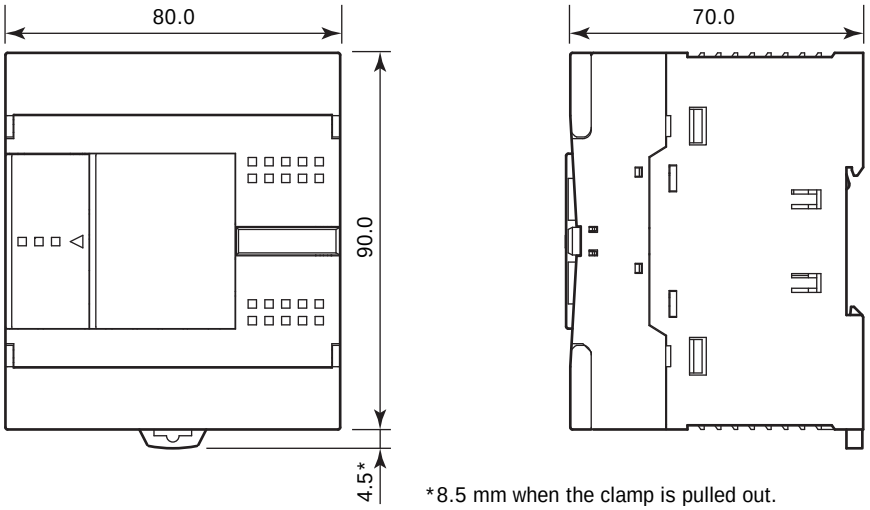


Dimensions

All MicroSmart modules have the same profile for consistent mounting on a DIN rail.

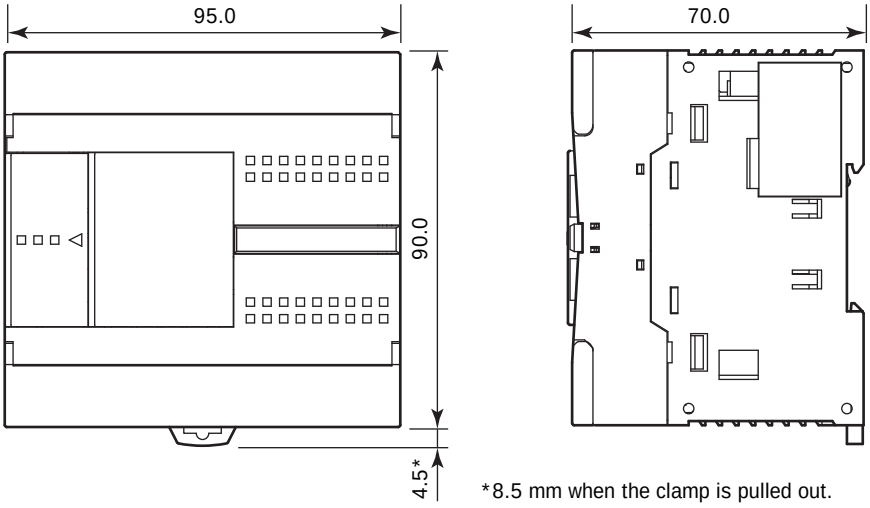
CPU Modules

FC5A-C10R2, FC5A-C10R2C, FC5A-C10R2D, FC5A-C16R2, FC5A-C16R2C, FC5A-C16R2D



*8.5 mm when the clamp is pulled out.

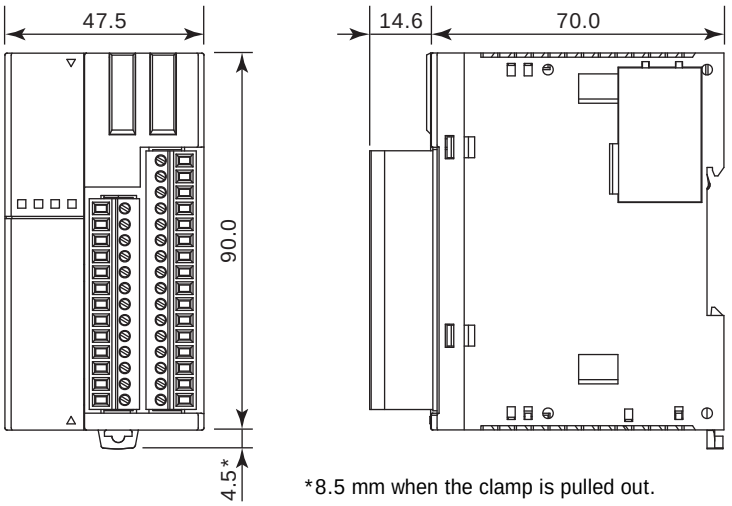
FC5A-C24R2, FC5A-C24R2C, FC5A-C24R2D



*8.5 mm when the clamp is pulled out.

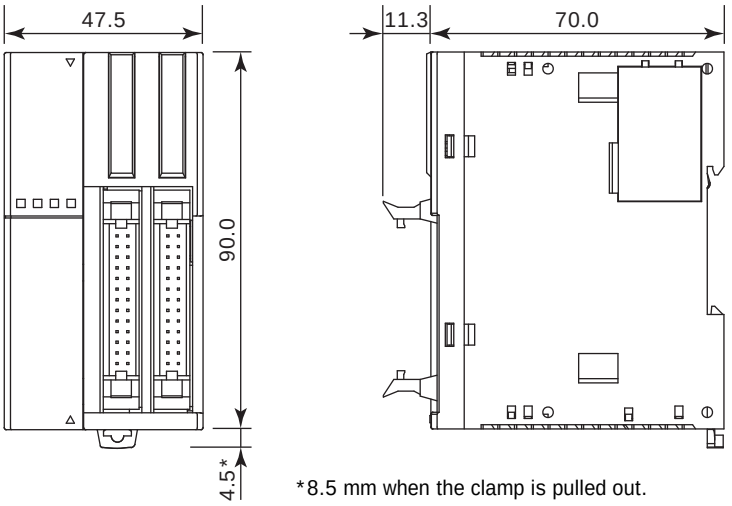
All dimensions in mm.

FC5A-D16RK1, FC5A-D16RS1



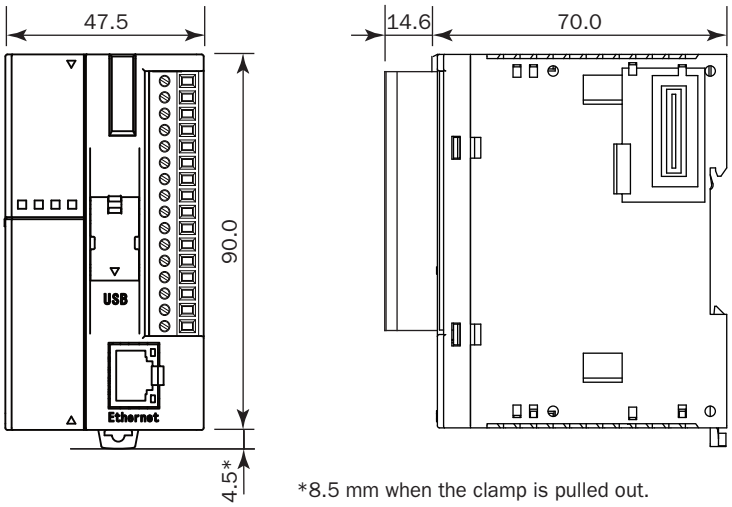
*8.5 mm when the clamp is pulled out.

FC5A-D32K3, FC5A-D32S3



*8.5 mm when the clamp is pulled out.

FC5A-D12K1E, FC5A-D12S1E

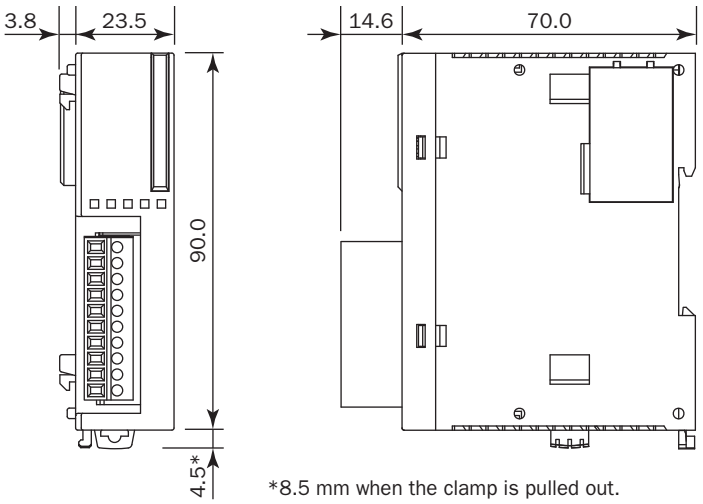


*8.5 mm when the clamp is pulled out.

All dimensions in mm.

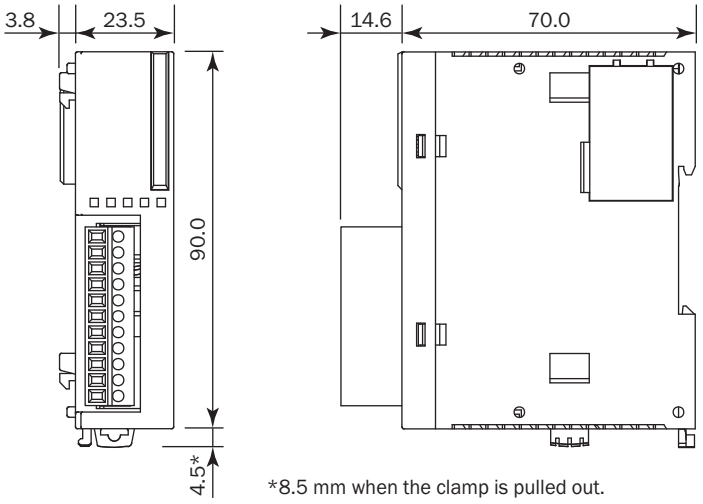
I/O Modules

FC4A-N08B1, FC4A-T08K1, FC4A-T08S1, FC5A-SIF2, FC5A-SIF4, FC4A-K2C1



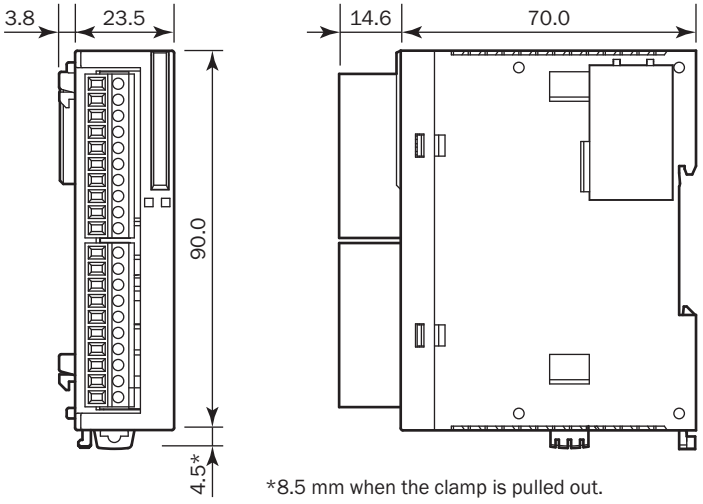
*8.5 mm when the clamp is pulled out.

FC4A-N08A11, FC4A-R081, FC4A-M08BR1,
FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-K1A1, FC4A-K4A1



*8.5 mm when the clamp is pulled out.

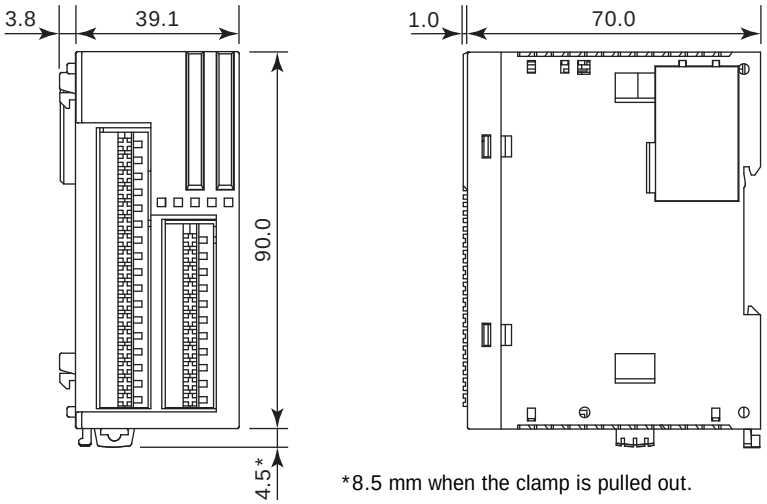
FC4A-N16B1, FC4A-R161, FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1



*8.5 mm when the clamp is pulled out.

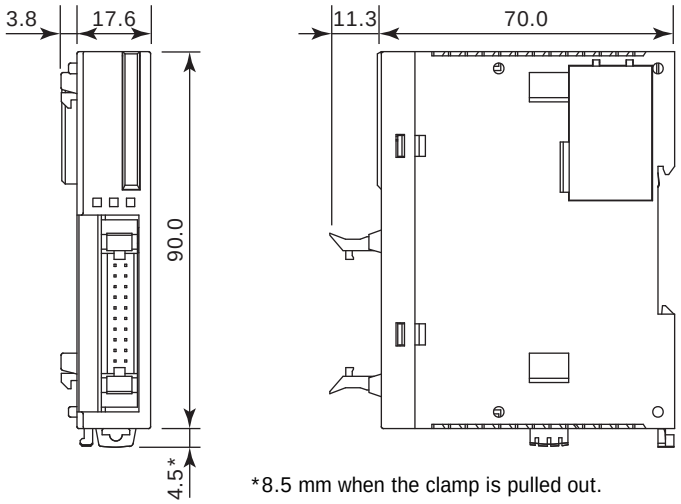
All dimensions in mm.

FC4A-M24BR2



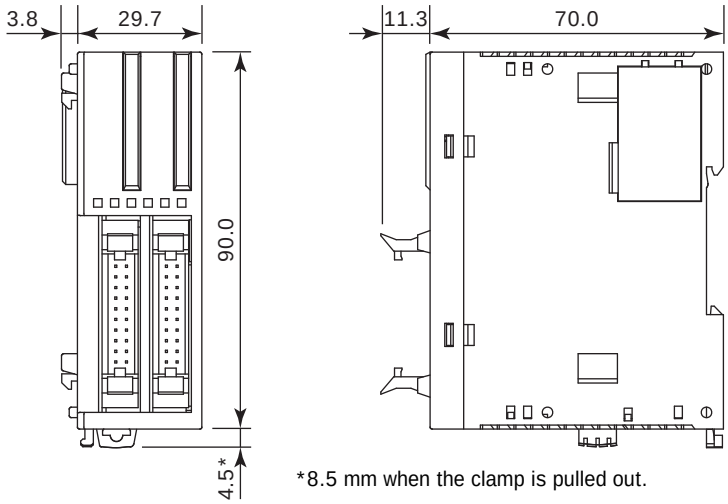
*8.5 mm when the clamp is pulled out.

FC4A-N16B3, FC4A-T16K3, FC4A-T16S3



*8.5 mm when the clamp is pulled out.

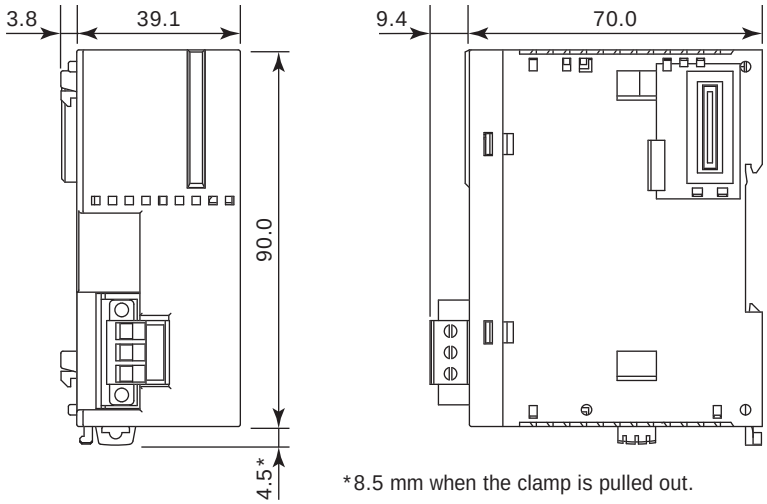
FC4A-N32B3, FC4A-T32K3, FC4A-T32S3



*8.5 mm when the clamp is pulled out.

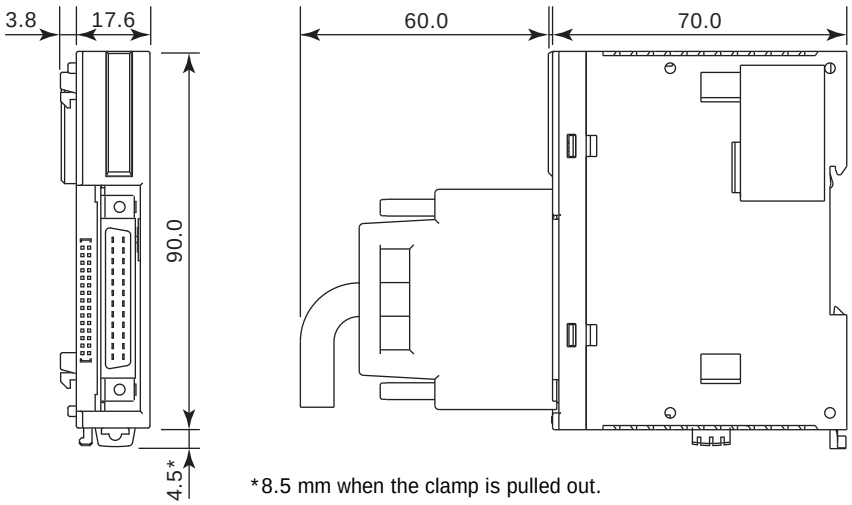
All dimensions in mm.

Expansion Interface Module FC5A-EXM2



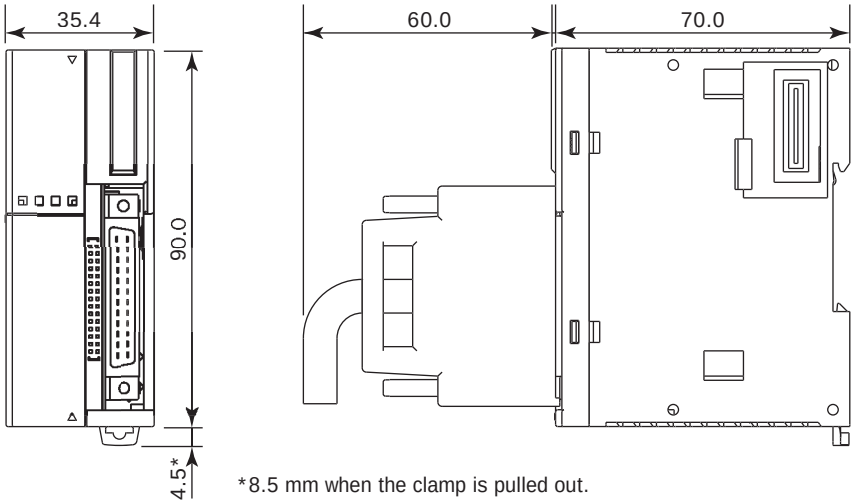
*8.5 mm when the clamp is pulled out.

Expansion Interface Master Module FC5A-EXM1M



*8.5 mm when the clamp is pulled out.

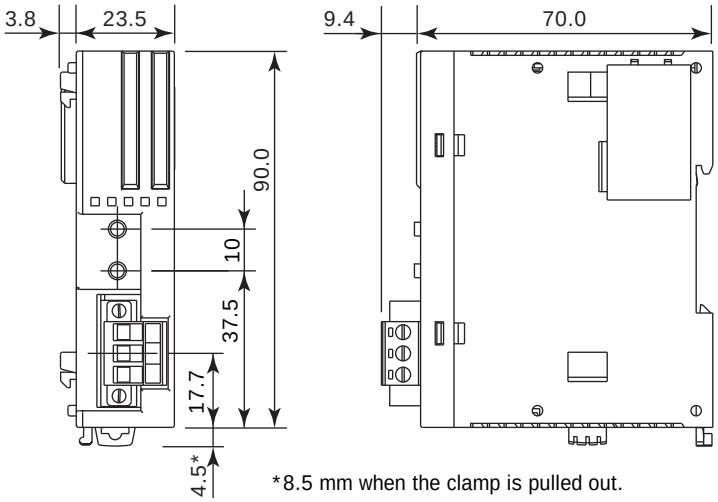
Expansion Interface Slave Module FC5A-EXM1S



*8.5 mm when the clamp is pulled out.

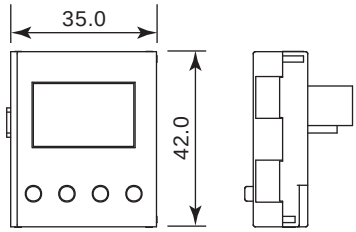
All dimensions in mm.

AS-Interface Module FC4A-AS62M

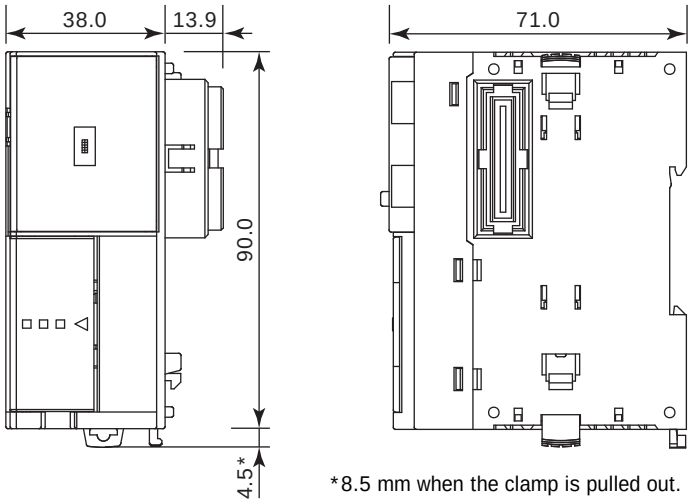


*8.5 mm when the clamp is pulled out.

HMI Module FC4A-PH1



HMI Base Module FC4A-HPH1

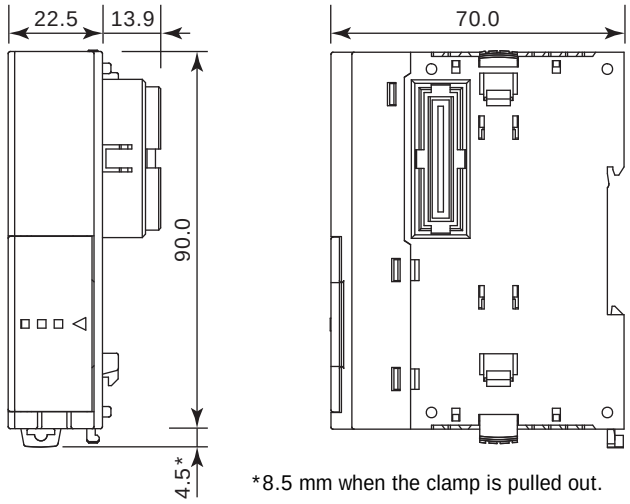


*8.5 mm when the clamp is pulled out.

All dimensions in mm.

Communication Modules

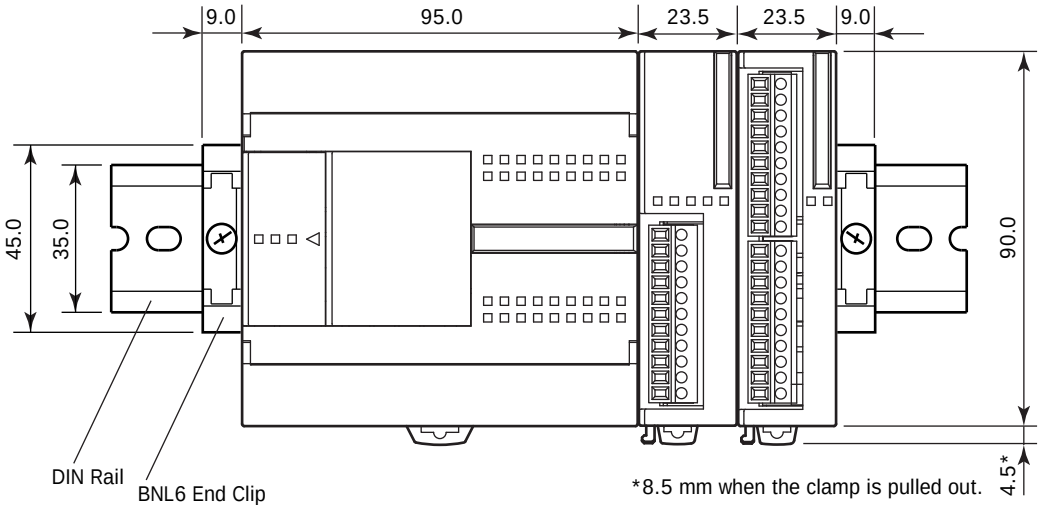
FC4A-HPC1, FC4A-HPC2, FC4A-HPC3



*8.5 mm when the clamp is pulled out.

Example:

The following figure illustrates a system setup consisting of the all-in-one 24-I/O type CPU module, an 8-point relay output module, and a 16-point DC input module mounted on a 35-mm-wide DIN rail using BNL6 end clips.



All dimensions in mm.

3: INSTALLATION AND WIRING

Introduction

This chapter describes the methods and precautions for installing and wiring MicroSmart modules.

Before starting installation and wiring, be sure to read "Safety Precautions" in the beginning of this manual and understand precautions described under Warning and Caution.

⚠ Warning

- Turn off the power to the MicroSmart before starting installation, removal, wiring, maintenance, and inspection of the MicroSmart. Failure to turn power off may cause electrical shocks or fire hazard.
- Emergency stop and interlocking circuits must be configured outside the MicroSmart. If such a circuit is configured inside the MicroSmart, failure of the MicroSmart may cause disorder of the control system, damage, or accidents.
- Special expertise is required to install, wire, program, and operate the MicroSmart. People without such expertise must not use the MicroSmart.

⚠ Caution

- Prevent metal fragments and pieces of wire from dropping inside the MicroSmart housing. Put a cover on the MicroSmart modules during installation and wiring. Ingress of such fragments and chips may cause fire hazard, damage, or malfunction.
- Do not touch the connector pins with hand, otherwise electrostatic discharge may damage the internal elements.
- Keep the MicroSmart wiring away from motor lines.

Installation Location

The MicroSmart must be installed correctly for optimum performance.

The MicroSmart is designed for installation in a cabinet. Do not install the MicroSmart outside a cabinet.

The environment for using the MicroSmart is "Pollution degree 2." Use the MicroSmart in environments of pollution degree 2 (according to IEC 60664-1).

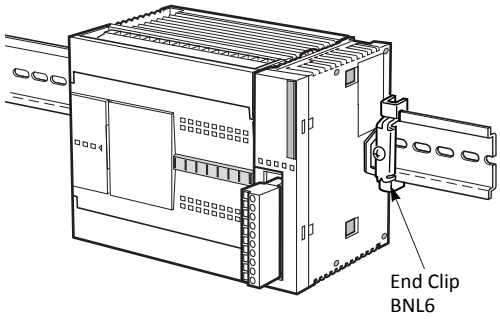
Make sure that the operating temperature does not drop below 0°C or exceed 55°C. If the temperature does exceed 55°C, use a fan or cooler.

Mount the MicroSmart on a vertical plane as shown at right.

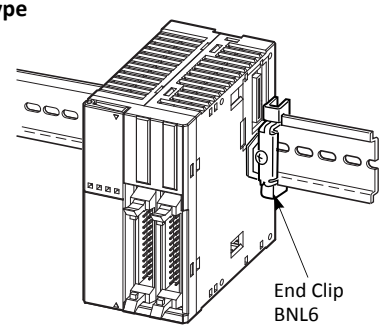
To eliminate excessive temperature build-up, provide ample ventilation. Do not install the MicroSmart near, and especially above, any device which generates considerable heat, such as a heater, transformer, or large-capacity resistor. The relative humidity should be above 30% and below 95%.

The MicroSmart should not be exposed to excessive dust, dirt, salt, direct sunlight, vibrations, or shocks. Do not use the MicroSmart in an area where corrosive chemicals or flammable gases are present. The modules should not be exposed to chemical, oil, or water splashes.

All-in-One Type



Slim Type



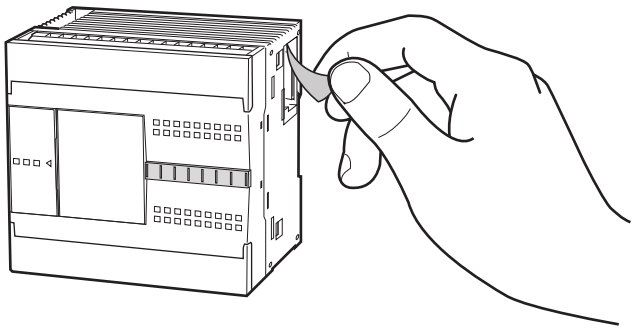
Assembling Modules

Caution

- Assemble MicroSmart modules together before mounting the modules onto a DIN rail. Attempt to assemble modules on a DIN rail may cause damage to the modules.
- Turn off the power to the MicroSmart before assembling the modules. Failure to turn power off may cause electrical shocks.

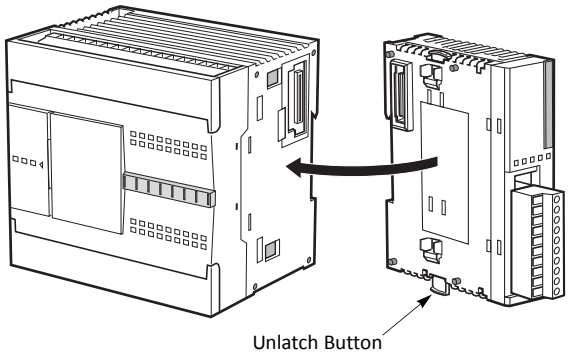
The following example demonstrates the procedure for assembling the all-in-one 24-I/O type CPU module and an I/O module together. When assembling slim type CPU modules, take the same procedure.

1. When assembling an input or output module, remove the expansion connector seal from the 24-I/O type CPU module.



2. Place the CPU module and I/O module side by side. Put the expansion connectors together for easy alignment.

3. With the expansion connectors aligned correctly and the blue unlatch button in the down position, press the CPU module and I/O module together until the latches click to attach the modules together firmly. If the unlatch button is in the up position, push down the button to engage the latches.



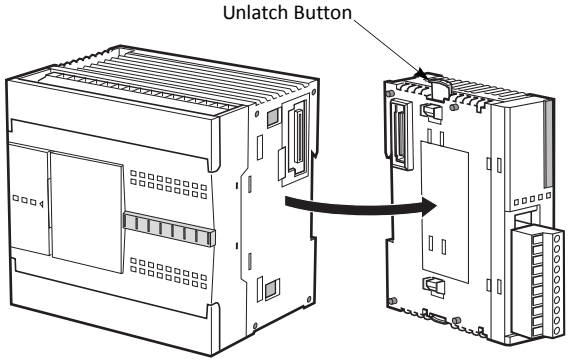
Disassembling Modules

Caution

- Remove the MicroSmart modules from the DIN rail before disassembling the modules. Attempt to disassemble modules on a DIN rail may cause damage to the modules.
- Turn off the power to the MicroSmart before disassembling the modules. Failure to turn power off may cause electrical shocks.

1. If the modules are mounted on a DIN rail, first remove the modules from the DIN rail as described on page 3-8.

2. Push up the blue unlatch button to disengage the latches, and pull the modules apart as shown. When disassembling slim type CPU modules, take the same procedure.



Installing the HMI Module

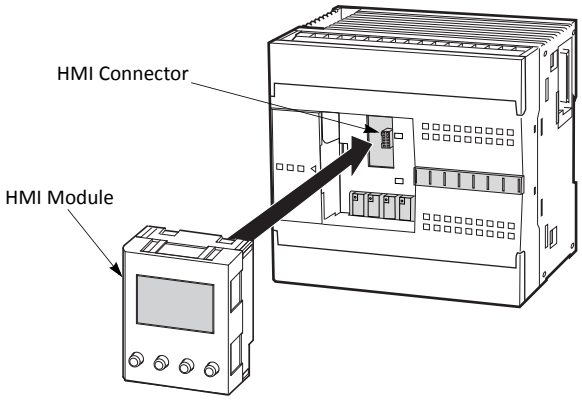
⚠ Caution

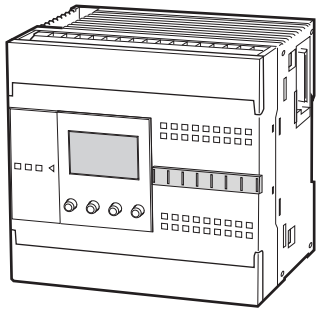
- Turn off the power to the MicroSmart before installing or removing the HMI module to prevent electrical shocks.
- Do not touch the connector pins with hand, otherwise electrostatic discharge may damage the internal elements.

The optional HMI module (FC4A-PH1) can mount on any all-in-one type CPU module, and also on the HMI base module mounted next to any slim type CPU module. For specifications of the HMI module, see page 2-80. For details about operating the HMI module, see page 5-60.

All-in-One Type

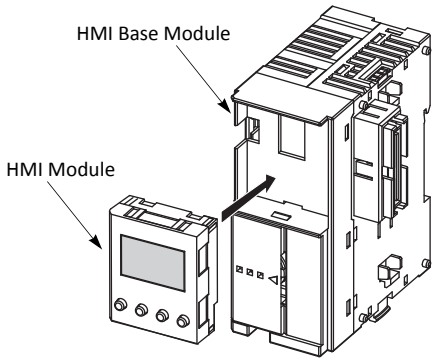
1. Remove the HMI connector cover from the CPU module. Locate the HMI connector inside the CPU module.
2. Push the HMI module into the HMI module connector in the CPU module until the latch clicks.



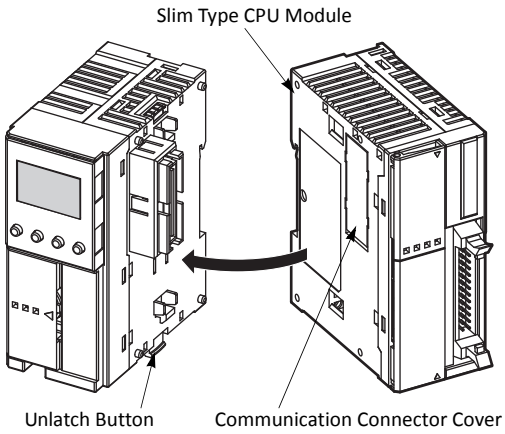


Slim Type

1. When using the HMI module with the slim type CPU module, prepare the optional HMI base module (FC4A-HPH1). See page 2-81.
2. Locate the HMI connector inside the HMI base module. Push the HMI module into the HMI connector in the HMI base module until the latch clicks.



3. Remove the communication connector cover from the slim type CPU module. See page 3-7.
4. Place the HMI base module and CPU module side by side. With the communication connectors aligned correctly and the blue unlatch button in the down position, press the HMI base module and CPU module together until the latches click to attach the modules together firmly. If the unlatch button is in the up position, push down the button to engage the latches.



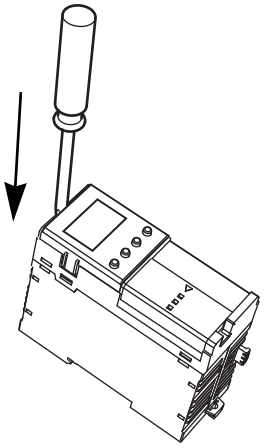
Removing the HMI Module

Caution

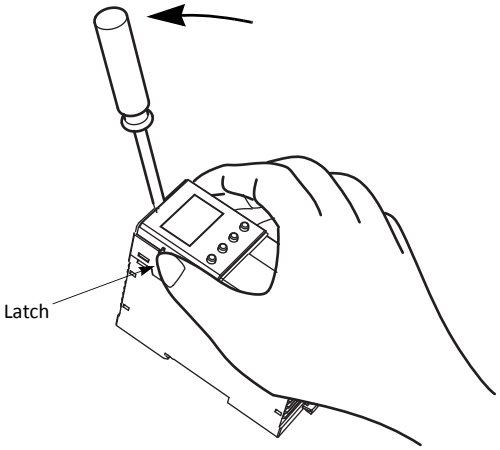
- Turn off the power to the MicroSmart before installing or removing the HMI module to prevent electrical shocks.
- Do not touch the connector pins with hand, otherwise electrostatic discharge may damage the internal elements.

This section describes the procedures for removing the HMI module from the optional HMI base module mounted next to any slim type CPU module.

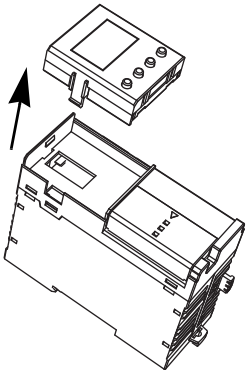
1. Insert a thin flat screwdriver (ø3.0 mm maximum) between the gap on top of the HMI module until the tip of the screwdriver bottoms.



2. While turning the screwdriver in the direction as shown, disengage the latch on the HMI module and pull out the HMI module.



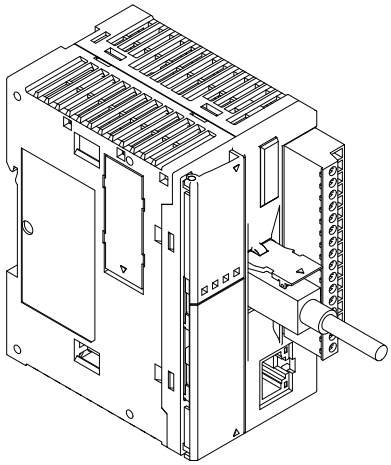
3. Remove the HMI module from the HMI base module.



Securing USB Extension Cable Using Cable Tie

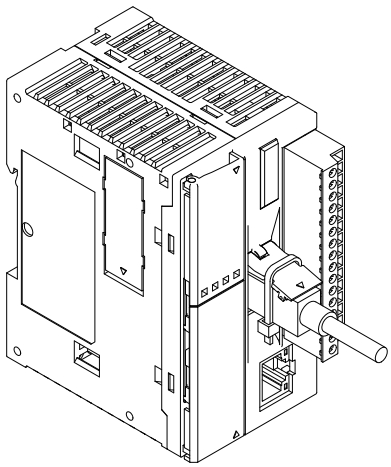
When FC5A-D12K1E/S1E is installed in a control panel, it is possible to extend the USB Mini-B port of the PLC to the panel surface using a USB extension cable (Note 1). When using the USB extension cable, it is recommended that the USB extension cable is secured to the USB port cover of the PLC using a cable tie (Note 2) so that the USB extension cable does not come loose from the USB port of the PLC. This section describes the procedure to secure the USB extension cable to the USB port cover using the cable tie.

1. Open the USB port cover and insert the USB extension cable into the USB port.



2. Pass a cable tie around the USB cable cover and the USB extension cable, taking care to route the cable tie through the notches on the USB cover.

3. Insert the tip of the cable tie through the locking section to make a loop. Tighten the loop until it is the suitable size and trim the excess cable tie using wire cutters.



Note 1: IDEC USB extension cable for USB Mini-B (HG9Z-XCE21) is recommended.

Note 2: HellermanTyton cable tie T18R-1000 is recommended.

Removing the Terminal Blocks

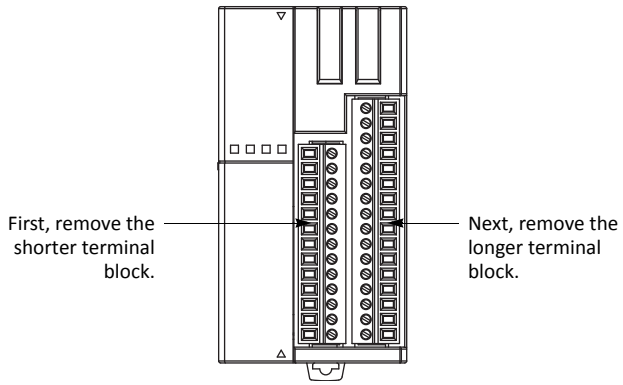
Caution

- Turn off the power to the MicroSmart before installing or removing the terminal blocks to prevent electrical shocks.
- Use the correct procedures to remove the terminal blocks, otherwise the terminal blocks may be damaged.

This section describes the procedures for removing the terminal blocks from slim type CPU modules FC5A-D16RK1, FC5A-D16RS1, FC5A-D12K1E and FC5A-D12S1E.

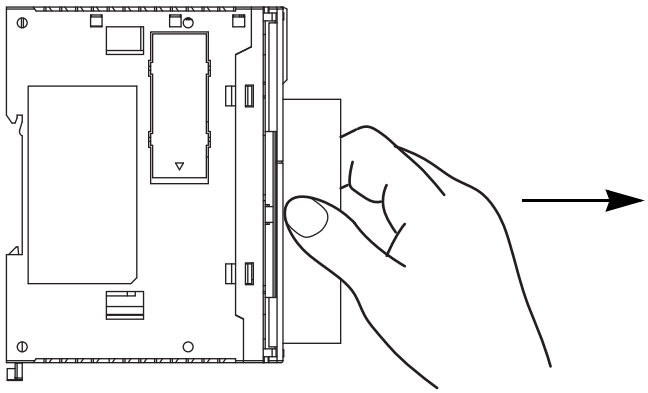
1. Before removing the terminal blocks, disconnect all wires from the terminal blocks.

Remove the shorter terminal block on the left first, then remove the longer one on the right.

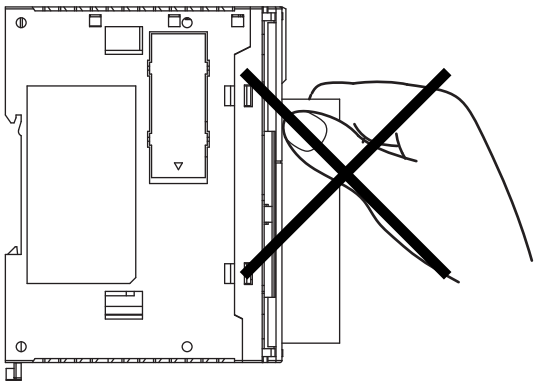


FC5A-D16RK1, FC5A-D16RS1, FC5A-D12K1E and FC5A-D12S1E

2. When removing the longer terminal block, hold the center of the terminal block, and pull it out straight.



3. Do not pull one end of the longer terminal block, otherwise the terminal block may be damaged.

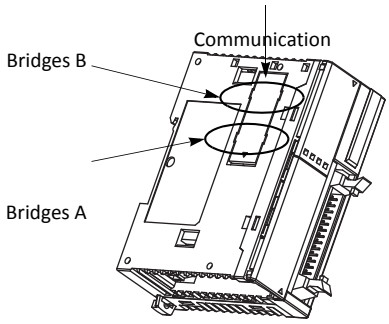


Removing the Communication Connector Cover

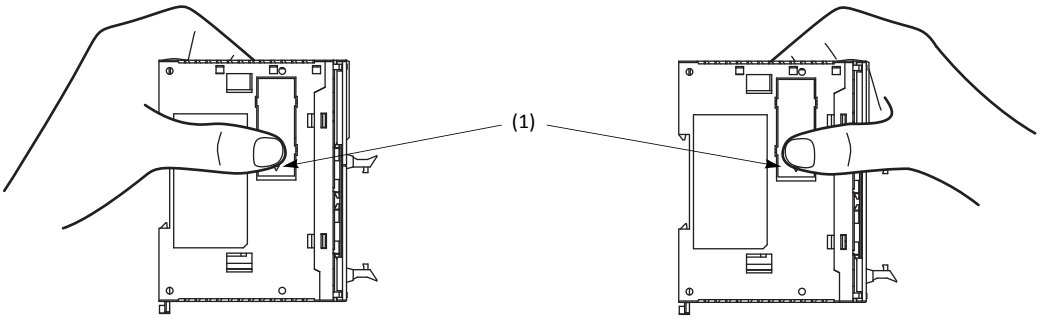
Caution

- When using a thin screwdriver to pull out the communication connector cover, insert the screwdriver carefully and do not damage the electronic parts inside the CPU module.
- When first pushing in the communication connector cover to break, take care not to injure your finger.

Before mounting a communication module or HMI base module next to the slim type CPU module, the communication connector cover must be removed from the CPU module. Break the communication connector cover on the slim type CPU module as described below.



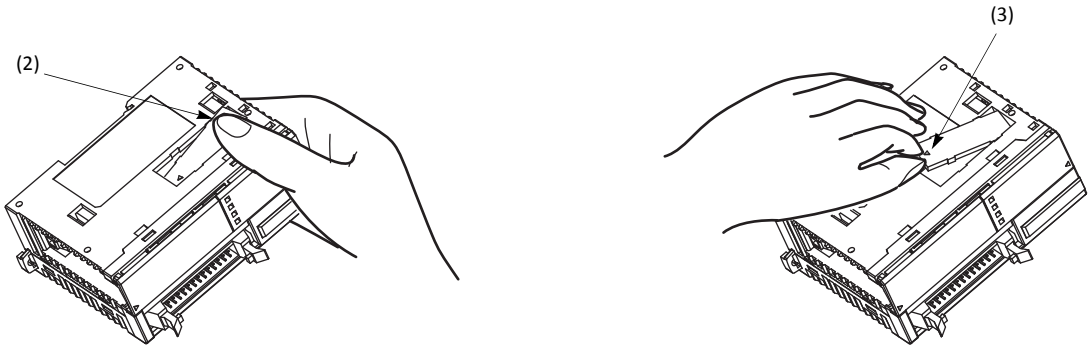
1. Carefully push in the communication connector cover at position (1) to break bridges A as shown in either figure below.



2. The other end (2) of the communication connector cover will come out as shown at left below. Push in this end.

3. Then, the opposite end (3) will come out. If the end does not come out, insert a thin screwdriver into the gap and pull out the end (3).

Hold the communication connector cover at (3), and pull off the communication connector cover to break bridges B.

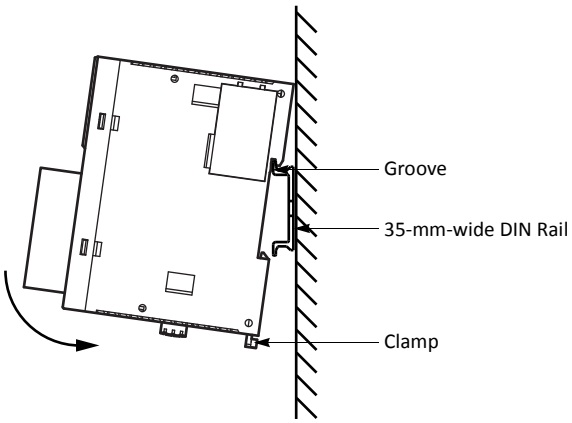


Mounting on DIN Rail

Caution

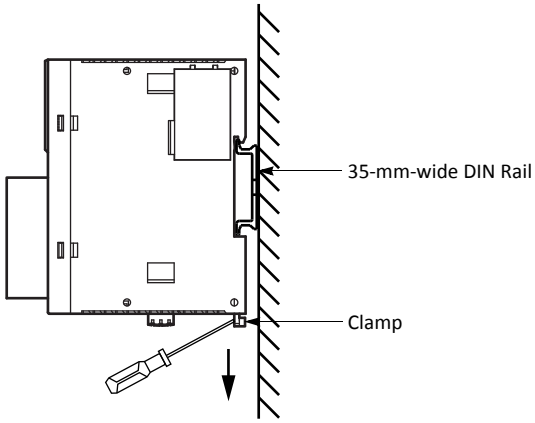
- Install the MicroSmart modules according to instructions described in this user's manual. Improper installation will result in falling, failure, or malfunction of the MicroSmart.
- Mount the MicroSmart modules on a 35-mm-wide DIN rail or a panel surface. Applicable DIN rail: IDEC's BAA1000PN10 or BAP1000PN10 (1000mm/39.4" long)

1. Fasten the DIN rail to a panel using screws firmly.
2. Pull out the clamp from each MicroSmart module, and put the groove of the module on the DIN rail. Press the modules towards the DIN rail and push in the clamps as shown on the right.
3. Use BNL6 end clips on both sides of the MicroSmart modules to prevent moving sideways.



Removing from DIN Rail

1. Insert a flat screwdriver into the slot in the clamp.
2. Pull out the clamps from the modules.
3. Turn the MicroSmart modules bottom out.

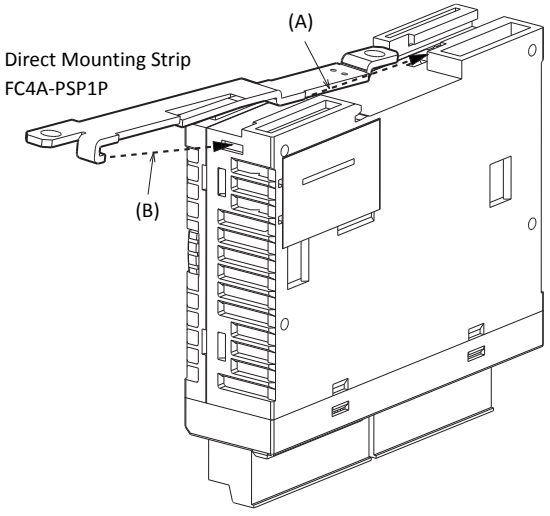


Direct Mounting on Panel Surface

MicroSmart modules can also be mounted on a panel surface inside a console. When mounting a slim type CPU module, digital I/O module, analog I/O module, HMI base module, or communication module, use optional direct mounting strip FC4A-PSP1P as described below.

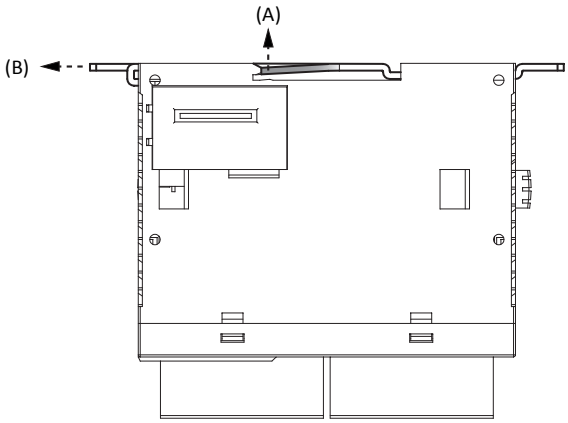
Installing the Direct Mounting Strip

1. Remove the clamp from the module by pushing the clamp inward.
2. Insert the direct mounting strip into the slot where the clamp has been removed (A). Further insert the direct mounting strip until the hook enters into the recess in the module (B).



Removing the Direct Mounting Strip

1. Insert a flat screwdriver under the latch of the direct mounting strip to release the latch (A).
2. Pull out the direct mounting strip (B).

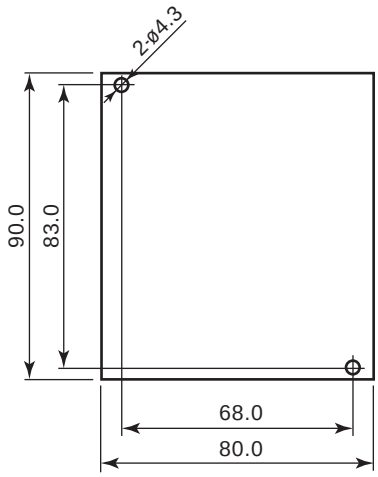


Mounting Hole Layout for Direct Mounting on Panel Surface

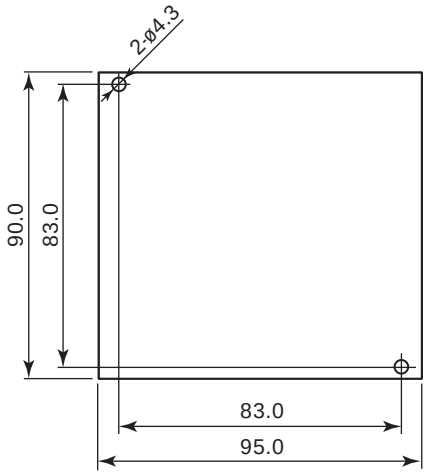
Make mounting holes of ø4.3 mm as shown below and use M4 screws (6 or 8 mm long) to mount the MicroSmart modules on the panel surface.

- **CPU Modules**

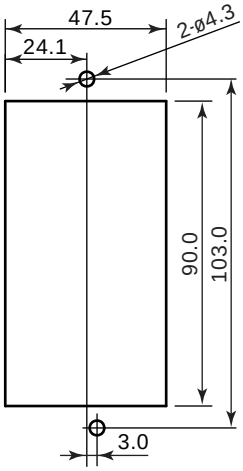
FC5A-C10R2, FC5A-C10R2C, FC5A-C10R2D, FC5A-C16R2, FC5A-C16R2C, FC5A-C16R2D



FC5A-C24R2, FC5A-C24R2C, FC5A-C24R2D



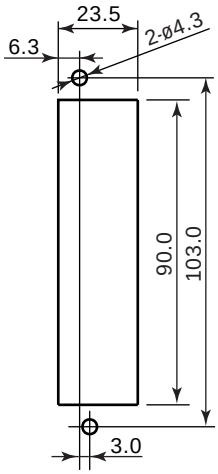
FC5A-D16RK1, FC5A-D16RS1, FC5A-D32K3, FC5A-D32S3, FC5A-D12K1E, FC5A-D12S1E



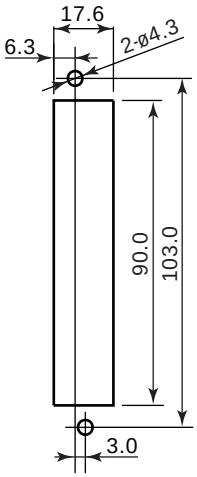
All dimensions in mm.

- **I/O Modules**

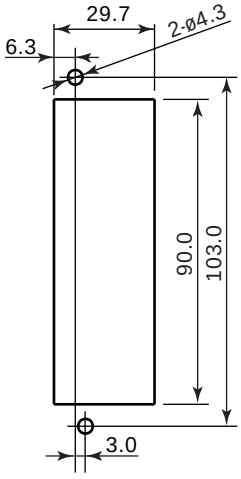
FC4A-N08B1, FC4A-N16B1, FC4A-N08A11, FC4A-R081, FC4A-R161, FC4A-T08K1, FC4A-T08S1, FC4A-M08BR1, FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, FC4A-K1A1, FC4A-K2C1, FC4A-K4A1, FC5A-SIF2, FC5A-SIF4



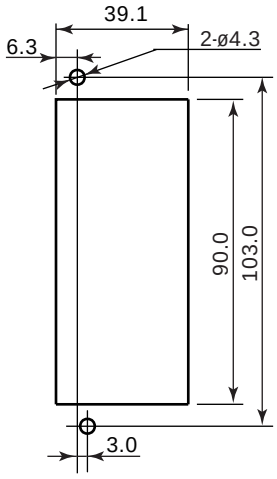
FC4A-N16B3, FC4A-T16K3, FC4A-T16S3



FC4A-N32B3, FC4A-T32K3, FC4A-T32S3

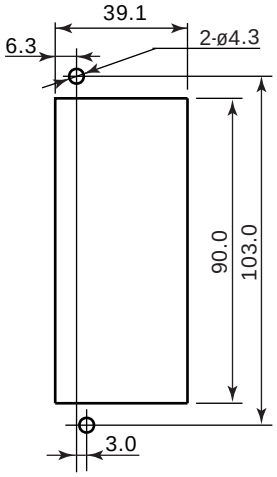


FC4A-M24BR2

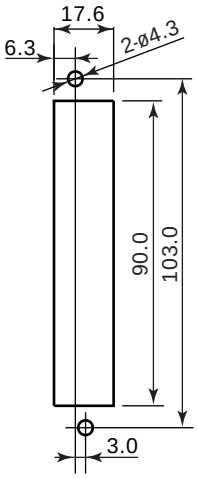


All dimensions in mm.

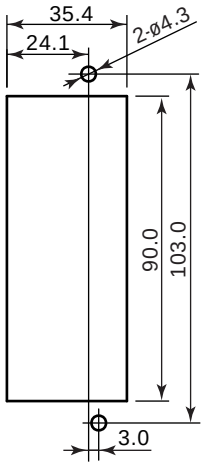
• **Expansion Interface Module**
FC5A-EXM2



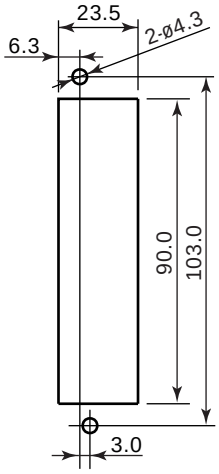
• **Expansion Interface Master Module**
FC5A-EXM1M



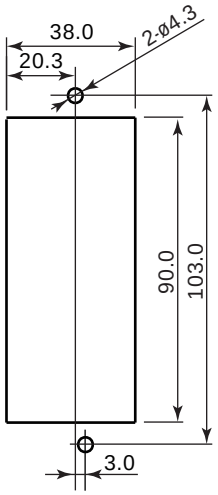
• **Expansion Interface Slave Module**
FC5A-EXM1S



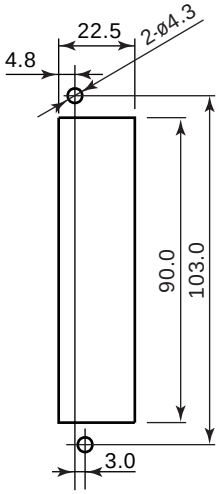
• **AS-Interface Module**
FC4A-AS62M



•**HMI Base Module**
FC4A-HPH1

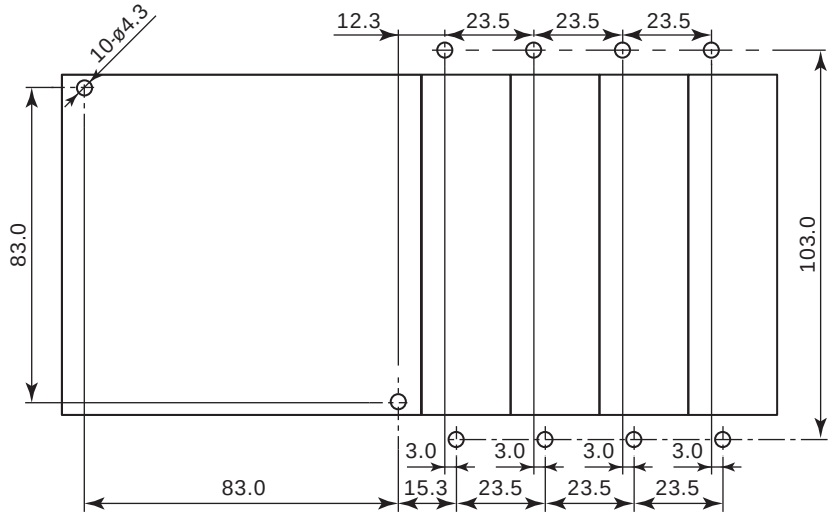


• **Communication Modules**
FC4A-HPC1, FC4A-HPC2, FC4A-HPC3



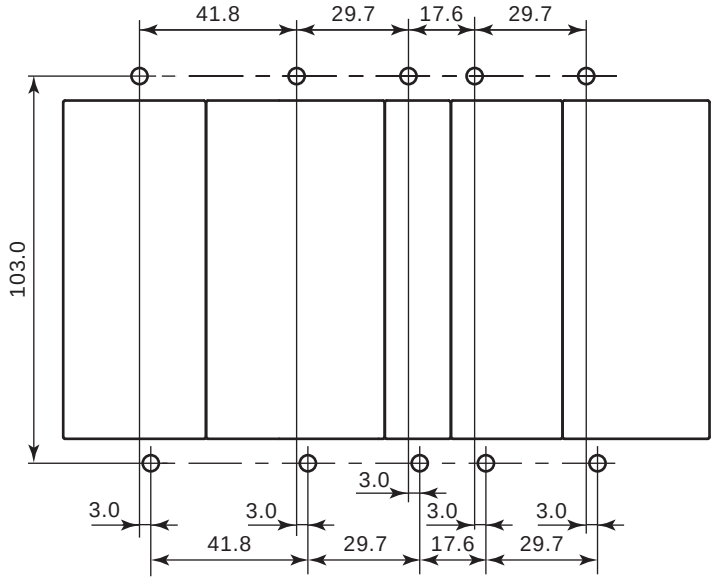
All dimensions in mm.

Example 1: Mounting hole layout for FC5A-C24R2 and 23.5-mm-wide I/O modules



Direct Mounting Strip
FC4A-PSP1P

Example 2: Mounting hole layout for, from left, FC4A-HPH1, FC5A-D16RK1, FC4A-N16B3, FC4A-N32B3, and FC4A-M24R2 modules



All dimensions in mm.

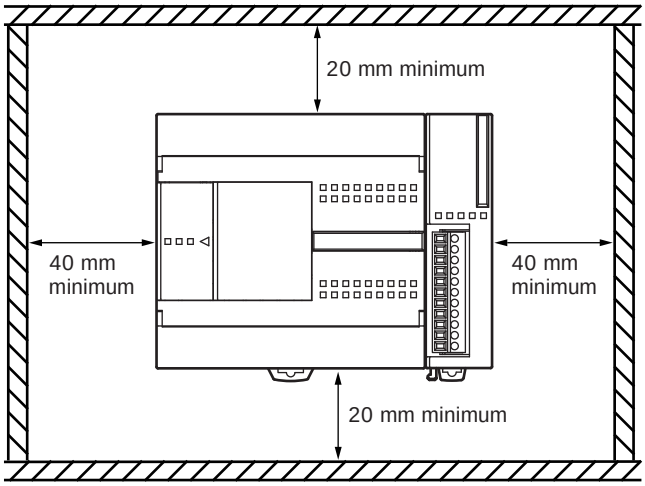
Installation in Control Panel

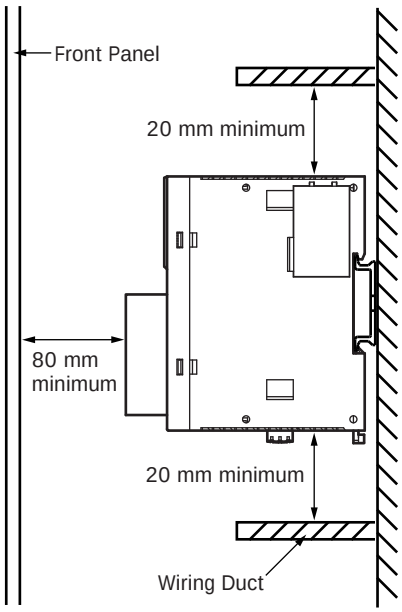
The MicroSmart modules are designed for installation in a cabinet. Do not install the MicroSmart modules outside a cabinet.

The environment for using the MicroSmart is “Pollution degree 2.” Use the MicroSmart in environments of pollution degree 2 (according to IEC 60664-1).

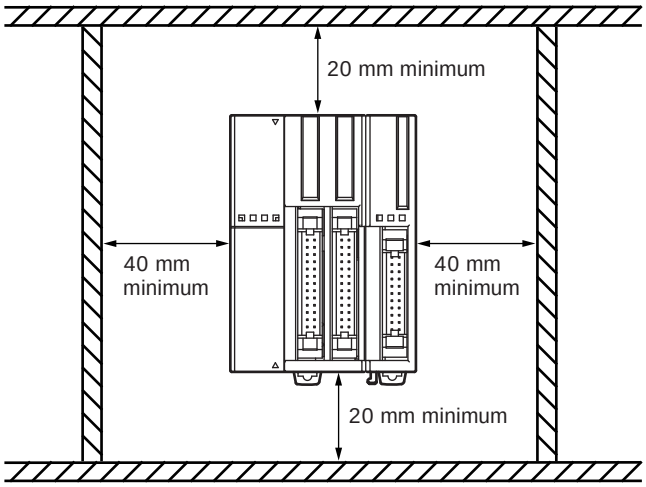
When installing the MicroSmart modules in a control panel, take the convenience of operation and maintenance, and resistance against environments into consideration.

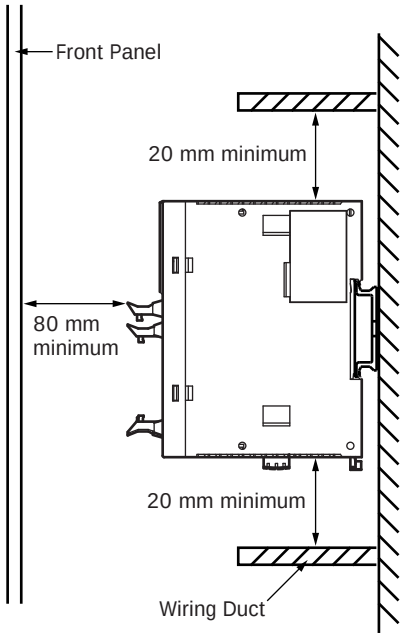
All-in-One Type CPU Module





Slim Type CPU Module



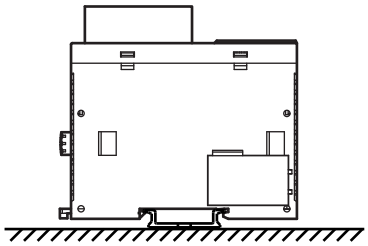


Mounting Direction

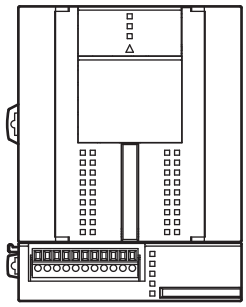
Mount the MicroSmart modules horizontally on a vertical plane as shown on the preceding page. Keep a sufficient spacing around the MicroSmart modules to ensure proper ventilation and keep the ambient temperature between 0°C and 55°C.

All-in-One Type CPU Module

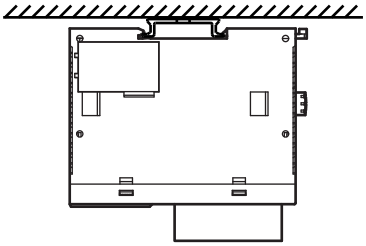
When the ambient temperature is 35°C or below, the all-in-one type CPU modules can also be mounted upright on a horizontal plane as shown at left below. When the ambient temperature is 40°C or below, the all-in-one type CPU modules can also be mounted sideways on a vertical plane as shown in the middle below.



Allowable Mounting Direction at 35°C or below



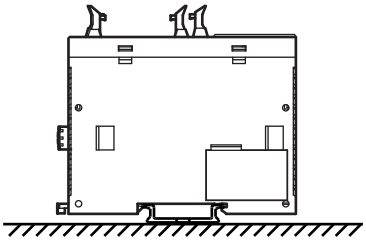
Allowable Mounting Direction at 40°C or below



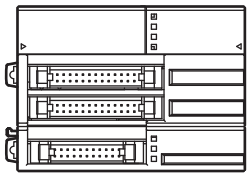
Incorrect Mounting Direction

Slim Type CPU Module

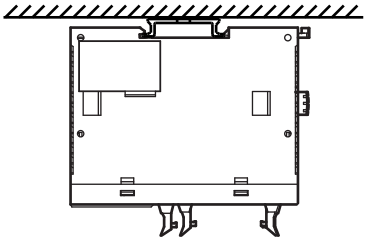
Always mount the slim type CPU modules horizontally on a vertical plane as shown on the preceding page. Any other mounting directions are not allowed.



Incorrect Mounting Direction



Incorrect Mounting Direction



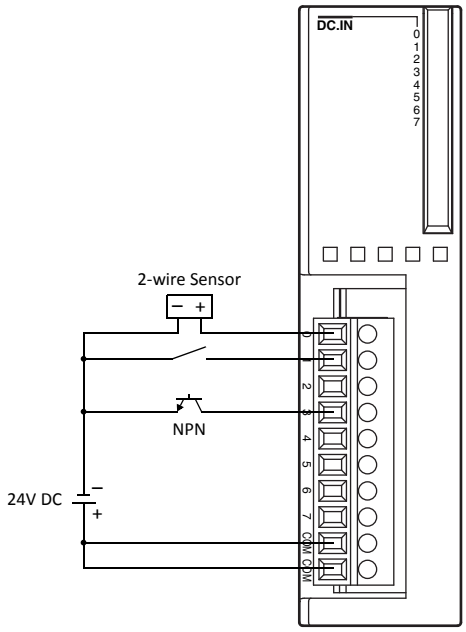
Incorrect Mounting Direction

Input Wiring

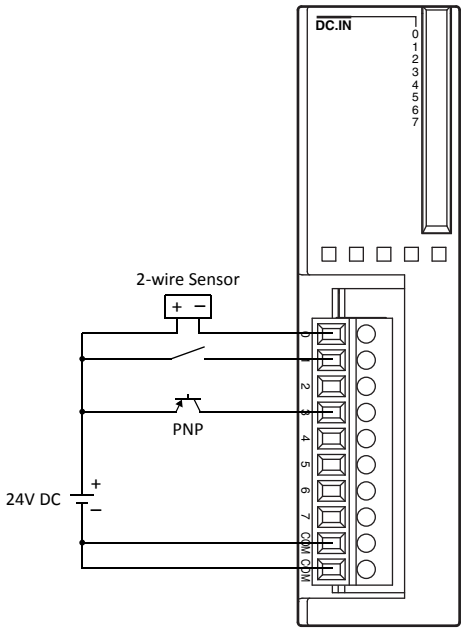
Caution

- Separate the input wiring from the output line, power line, and motor line.
- Use proper wires for input wiring.
  All-in-one type CPU modules: UL1015 AWG22 or UL1007 AWG18
  Slim type CPU and I/O modules: UL1015 AWG22

DC Source Input



DC Sink Input

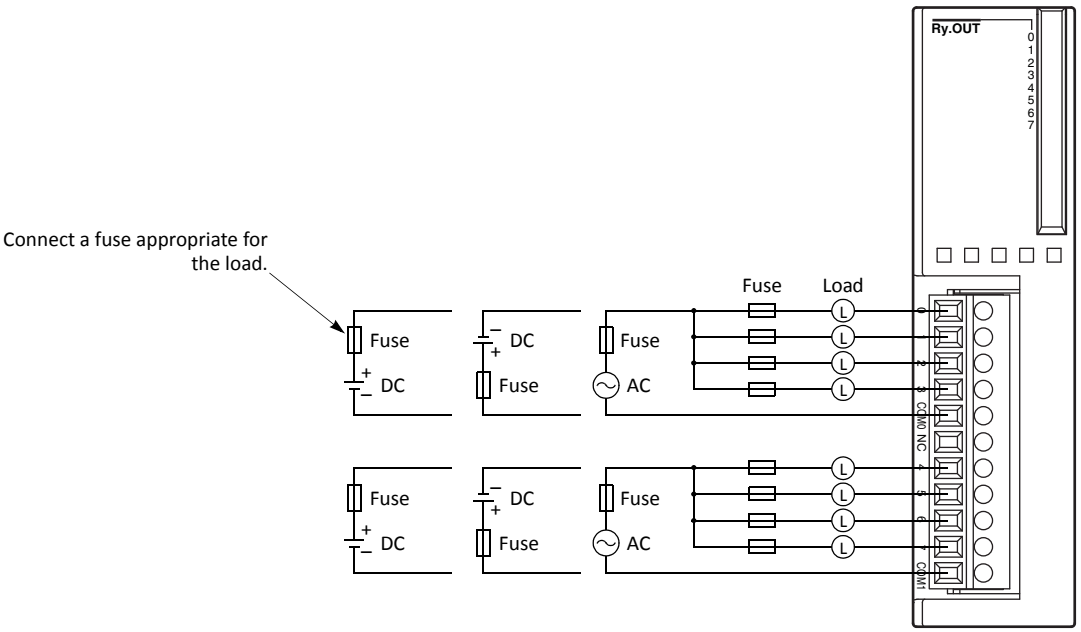


Output Wiring

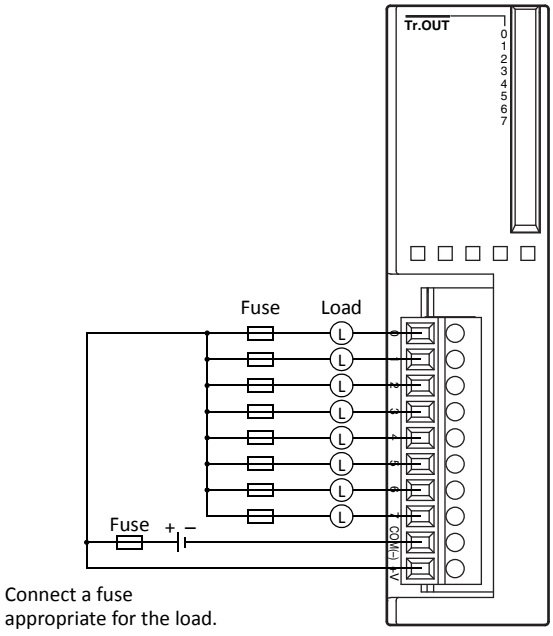
Caution

- If output relays or transistors in the MicroSmart CPU or output modules should fail, outputs may remain on or off. For output signals which may cause heavy accidents, provide a monitor circuit outside the MicroSmart.
- Connect a fuse to the output module, selecting a fuse appropriate for the load.
- Use proper wires for output wiring.
  All-in-one type CPU modules: UL1015 AWG22 or UL1007 AWG18
  Slim type CPU and I/O modules: UL1015 AWG22
- When equipment containing the MicroSmart is intended for use in European countries, insert an IEC 60127-approved fuse to each output of every module for protection against overload or short-circuit. This is required when equipment containing the MicroSmart is destined for Europe.

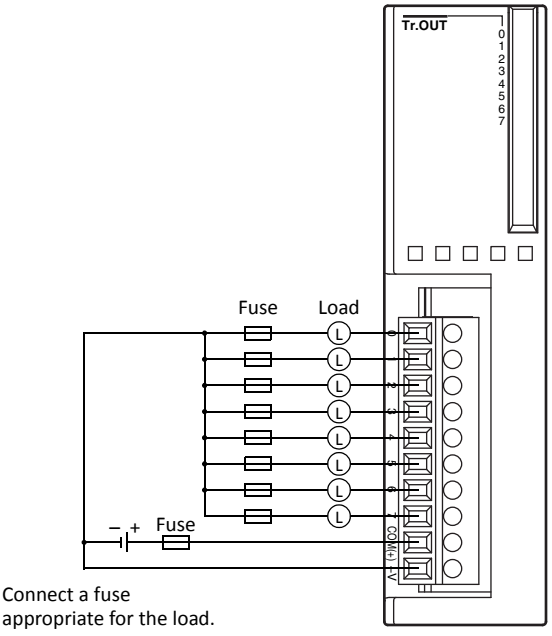
Relay Output



Transistor Sink Output



Transistor Source Output

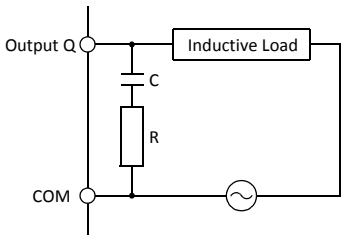


Contact Protection Circuit for Relay and Transistor Outputs

Depending on the load, a protection circuit may be needed for the relay output of the MicroSmart modules. Choose a protection circuit from A through D shown below according to the power supply and connect the protection circuit to the outside of the CPU or relay output module.

For protection of the transistor output of the MicroSmart modules, connect protection circuit C shown below to the transistor output circuit.

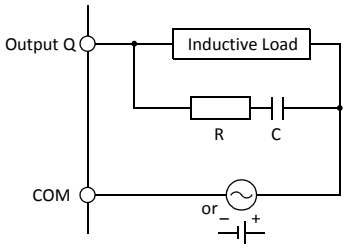
Protection Circuit A



This protection circuit can be used when the load impedance is smaller than the RC impedance in an AC load power circuit.

R: Resistor of approximately the same resistance value as the load
C: 0.1 to 1 μF

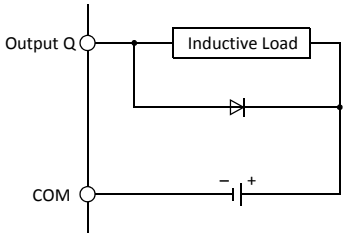
Protection Circuit B



This protection circuit can be used for both AC and DC load power circuits.

R: Resistor of approximately the same resistance value as the load
C: 0.1 to 1 μF

Protection Circuit C

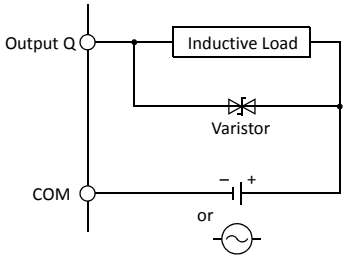


This protection circuit can be used for DC load power circuits.

Use a diode with the following ratings.

Reverse withstand voltage: Power voltage of the load circuit × 10
Forward current: More than the load current

Protection Circuit D



This protection circuit can be used for both AC and DC load power circuits.

Power Supply

All-in-One Type CPU Module (AC and DC Power)

⚠ Caution

- Use a power supply of the rated value. Use of a wrong power supply may cause fire hazard.
- The allowable power voltage range is 85 to 264V AC for the AC power type CPU module, 20.4 to 28.8V DC for the 24V DC power type CPU module, and 10.2 to 18.0V DC for the 12V DC power type CPU module. Do not use the MicroSmart CPU module on any other voltage.
- On the AC power type CPU module, if the power voltage turns on or off very slowly between 15 and 50V AC, the CPU module may run and stop repeatedly between these voltages.
- On the 12V DC power type CPU module, if the power voltage changes very slowly to turn on or off, the CPU module may run and stop repeatedly.
- When MicroSmart I/O signals are connected to a device which may cause a major accident in case of an error, take a measure to secure safety, such as providing a voltage monitoring circuit outside the MicroSmart.
- Use an IEC 60127-approved fuse on the power line outside the MicroSmart. This is required when equipment containing the MicroSmart is destined for Europe.

Power Supply Voltage

The allowable power voltage range for the all-in-one type MicroSmart CPU module is 85 to 264V AC (AC power type), 20.4 to 28.8V DC (24V DC power type), and 10.2 to 18.0V DC (12V DC power type). Do not use the MicroSmart CPU module on any other voltage.

Power failure detection voltage depends on the quantity of used input and output points. Basically, power failure is detected when the power voltage drops below 85V AC (AC power type), 20.4V DC (24V DC power type), and 10.2V DC (12V DC power type), stopping operation to prevent malfunction.

On AC power type CPU modules, a momentary power interruption for 10 ms or less is not recognized as a power failure at the rated voltage of 100 to 240V AC.

On DC power type CPU modules, a momentary power interruption for 10 ms or less is not recognized as a power failure at the rated voltage of 24 or 12V DC.

Inrush Current at Powerup

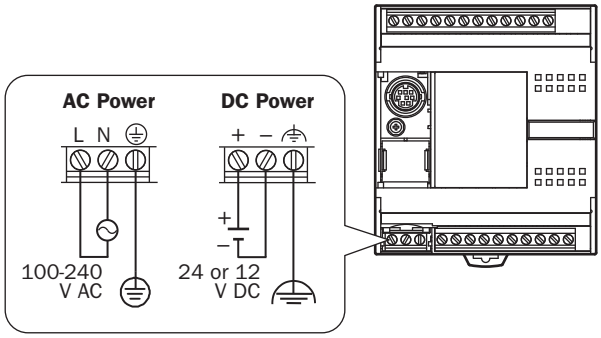
When the all-in-one AC or 24V DC power type CPU module is powered up, an inrush current of a maximum of 35A (10- and 16-I/O type CPU modules) or 40A (24-I/O type CPU module) flows.

When the 12V DC power type CPU module is powered up, an inrush current of a maximum of 20A flows.

Power Supply Wiring

Use a stranded wire of UL1015 AWG22 or UL1007 AWG18 for power supply wiring. Make the power supply wiring as short as possible.

Run the power supply wiring as far away as possible from motor lines.



Grounding

To prevent electrical shocks, connect the ⏚ or ⏚ terminal to a proper ground using a wire of UL1007 AWG16. The grounding also prevents malfunctioning due to noise.

Do not connect the grounding wire in common with the grounding wire of motor equipment.

Separate the grounding wires of the MicroSmart and external devices which can be a possible noise source.

Use a thick wire for grounding the MicroSmart and make the grounding wire as short as possible to make sure that noises from external devices can be conducted to the ground effectively.

Slim Type CPU Module and Expansion Interface Module (DC Power)

⚠ Caution

- Use a power supply of the rated value. Use of a wrong power supply may cause fire hazard.
- The allowable power voltage range for the slim type MicroSmart CPU module, expansion interface module FC5A-EXM2, and expansion interface slave module FC5A-EXM1S is 20.4 to 26.4V DC. Do not use the MicroSmart on any other voltage.
- If the power voltage turns on or off very slowly, the MicroSmart may run and stop repeatedly or I/O operation may fluctuate at a voltage lower than the rated voltage.
- When MicroSmart I/O signals are connected to a device which may cause a major accident in case of an error, take a measure to secure safety, such as providing a voltage monitoring circuit outside the MicroSmart.
- Use one power supply to power the CPU module and the expansion interface module or expansion interface slave module.
- When using a separate power supply, power up the expansion interface module or expansion interface slave module first, followed by the CPU module, otherwise the CPU module causes an error and cannot start and stop operation.
- Use an IEC 60127-approved fuse on the power line outside the MicroSmart. This is required when equipment containing the MicroSmart is destined for Europe.

Power Supply Voltage

The allowable power voltage range for the slim type MicroSmart CPU module is 20.4 to 26.4V DC.

Power failure detection voltage depends on the quantity of used input and output points. Basically, power failure is detected when the power voltage drops below 20.4V DC, stopping operation to prevent malfunction.

A momentary power interruption for 10 ms or less is not recognized as a power failure at the rated voltage of 24V DC.

Inrush Current at Powerup

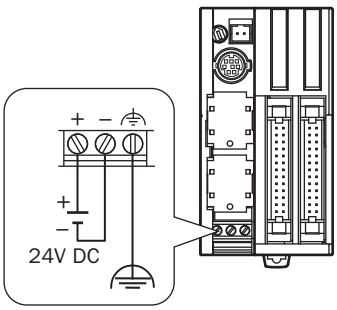
When the slim type CPU module, expansion interface module, or expansion interface slave module is powered up, an inrush current of a maximum of 50A flows.

Power Supply Wiring

Use a stranded wire of UL1015 AWG22 or UL1007 AWG18 for power supply wiring. Make the power supply wiring as short as possible.

Run the power supply wiring as far away as possible from motor lines.

For a power supply wiring example of expansion interface modules, see page 2-77.



Grounding

To prevent electrical shocks, connect the ⏚ terminal to a proper ground using a wire of UL1015 AWG22 or UL1007 AWG18. The grounding also prevents malfunctioning due to noise.

Do not connect the grounding wire in common with the grounding wire of motor equipment.

Separate the grounding wires of the MicroSmart and external devices which can be a possible noise source.

Use a thick wire for grounding the MicroSmart and make the grounding wire as short as possible to make sure that noises from external devices can be conducted to the ground effectively.

AS-Interface Master Module

The AS-Interface bus uses a dedicated 30V DC power supply (AS-Interface power supply). For AS-Interface power supply and power supply wiring, see pages 24-3 and 24-7 (Advanced Vol.).

Precautions for Connecting Communication Devices

When connecting communication devices to the MicroSmart, take possible external noise sources into consideration.

In a communication network consisting of a MicroSmart and an external device (a communication device which has a functional ground and a signal ground connected together internally [for example, IDEC's HG3F and HG4F operator interfaces]), if all devices are powered by a common AC or DC power source, noise generated by the external device may affect the internal circuits of the MicroSmart and the communication device. Take the following measures depending on the operating environment.

- Use a separate power supply for the external device generating noises so that a loop circuit to induce noises can not be formed.
- Disconnect the functional ground terminal of the communication device from the ground line. This measure may result in deterioration of EMC characteristics. When taking this measure, make sure that the EMC characteristics of the entire system are satisfactory.
- Connect the functional ground terminal of the communication device to the 0V line of the power supply so that the noises from the external device do not flow through the communication line.
- Connect an isolator to the communication line so that a loop circuit to induce noises can not be formed.

Maximum Quantity of Applicable Expansion Modules

This section describes precautions for installing the expansion RS232C communication module in connection with the internal current draw by other expansion modules.

The all-in-one 24-I/O type CPU module (except 12V DC power type) can mount a maximum of three expansion RS232C communication modules. The slim type CPU module can mount a maximum of five expansion RS232C communication modules.

Including expansion RS232C communication modules and other expansion modules, the all-in-one type CPU module can mount a maximum of four expansion modules, and the slim type CPU module can mount a maximum of seven expansion modules, unless the total internal current draw by all connected expansion modules exceeds the allowable current draw of the CPU module. Make sure that the total internal current draw does not exceed the current capacity of the CPU module.

Allowable Total Internal Current Draw

CPU Module	Quantity of Expansion RS232C Communication Modules	Quantity of Expansion Modules	Total Internal Current Draw (5V DC)
All-in-one 24-I/O Type CPU Module	3 maximum (Note)	4 maximum	260 mA maximum
Slim Type CPU Module	5 maximum	7 maximum	455 mA maximum

Note: The all-in-one 24-I/O type CPU module cannot use the expansion RS232C/RS485 communication module in combination with function modules listed below. When using the expansion RS232C/RS485 communication module and these function modules, use the slim type CPU module.

Function Module	Type No.
Analog I/O Module	FC4A-L03A1, FC4A-L03AP1, FC4A-J2A1, FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, FC4A-K1A1, FC4A-K2C1, FC4A-K4A1
AS-Interface Master Module	FC4A-AS62M

Internal Current Draw by Expansion Modules

Module	Type No.	Internal Current Draw (5V DC)	Module	Type No.	Internal Current Draw (5V DC)
Input Module	FC4A-N08B1	25 mA maximum	**Mixed I/O Module**	FC4A-M08BR1	25 mA maximum
	FC4A-N16B1	40 mA maximum		FC4A-M24BR2	65 mA maximum
	FC4A-N16B3	35 mA maximum	**Analog I/O Module**	FC4A-L03A1	50 mA maximum
	FC4A-N32B3	65 mA maximum		FC4A-L03AP1	50 mA maximum
	FC4A-N08A11	60 mA maximum	**Analog Input Module**	FC4A-J2A1	50 mA maximum
Relay Output Module	FC4A-R081	30 mA maximum		FC4A-J4CN1	50 mA maximum
	FC4A-R161	45 mA maximum		FC4A-J8C1	40 mA maximum
Transistor Output Module	FC4A-T08K1	10 mA maximum		FC4A-J8AT1	45 mA maximum
	FC4A-T08S1	10 mA maximum	**Analog Output Module**	FC4A-K1A1	50 mA maximum
	FC4A-T16K3	10 mA maximum		FC4A-K2C1	60 mA maximum
	FC4A-T16S3	10 mA maximum		FC4A-K4A1	65 mA maximum
	FC4A-T32K3	20 mA maximum			
	FC4A-T32S3	20 mA maximum			
AS-Interface Master Module (Note 1)				FC4A-AS62M	80 mA maximum
Expansion RS232C Communication Module				FC5A-SIF2	40 mA [85 mA] maximum (Note 2)
Expansion RS485 Communication Module				FC5A-SIF4	40 mA maximum
PID Module (Note 3)				FC5A-F2MR2	65 mA maximum
				FC5A-F2M2	65 mA maximum

Note 1: A maximum of two AS-Interface master modules can be mounted even if the total current draw is within the limits.

Only one expansion interface module or expansion interface master module can be mounted to a CPU module, and is not included in the calculation of the total current draw by expansion modules.

Note 2: Values indicated in square brackets represent FC5A-SIF2 earlier than version 200.

Note 3: For details about the PID module, see FC5A Series PID Module User's Manual.

Example: Installing five expansion RS232C communication modules to the slim type CPU module

Module	Type No.	Quantity	Internal Current Draw (5V DC)	Total Internal Current Draw
Expansion RS232C Communication Module	FC5A-SIF2 (Earlier than V200)	5	85 mA	425 mA
Maximum Applicable Expansion Modules (Slim CPU)		7	—	455 mA
Balance		2	—	30 mA

In the above example, two more expansion modules can be added, with a maximum total current draw of 30 mA. The following table shows an example of installing the maximum quantity of expansion modules.

Module	Type No.	Quantity	Internal Current Draw (5V DC)	Total Internal Current Draw
Expansion RS232C Communication Module	FC5A-SIF2 (Earlier than V200)	5	85 mA	425 mA
Transistor Output Module	FC4A-T08S1	1	10 mA	10 mA
	FC4A-T32K3	1	20 mA	20 mA
Total		7	—	455 mA

Example: Installing an expansion interface module and RS232C communication modules

When using an expansion interface module, the current draw by the expansion interface module is not included in the total of internal current draw the current capacity of the CPU module as shown in the example below.

Area	Module	Type No.	Quantity	Internal Current Draw (5V DC)	Total Internal Current Draw
Expansion	Expansion RS232C Communication Module	FC5A-SIF2 (Earlier than V200)	5	85 mA	425 mA
	Total		5	—	425 mA
Expansion Interface Module		FC5A-EXM2 or FC5A-EXM1M + FC5A-EXM1S			
Additional	Input Module	FC4A-N32B3	4	65 mA	260 mA
	Transistor Output Module	FC4A-T32K3	4	20 mA	80 mA
	Total		8	—	340 mA

In the additional area on the right of the expansion interface module (FC5A-EXM2, FC5A-EXM1M, and FC5A-EXM1S), a maximum of eight digital I/O modules can be mounted regardless of the internal current draw of the digital I/O modules.

Expansion RS232C communication modules cannot be mounted on the right of expansion interface module.

For details about the expansion interface modules, see page 2-72.

⚠ Warning

- This equipment is suitable for use in Class I, Division 2, Groups A, B, C, D or non-hazardous locations only.
- Explosion hazard — Substitution of components may impair suitability for Class I, Division 2.
- Explosion hazard — Do not disconnect equipment unless power has been switched off or the area is known to be non-hazardous.

⚠ Caution

- Make sure that the total internal current draw by all connected expansion modules does not exceed the allowable current draw of the CPU module. Otherwise the CPU and other modules do not operate correctly. The CPU module does not detect the excessive current draw.
- The expansion RS232C communication module cannot be mounted on the right of expansion interface modules (FC5A-EXM2, FC5A-EXM1M, and FC5A-EXM1S). Expansion interface modules can be mounted on the right of the expansion RS232C communication module.

Terminal Connection

Caution

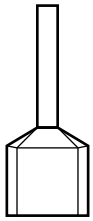
- Make sure that the operating conditions and environments are within the specification values.
- Be sure to connect the grounding wire to a proper ground, otherwise electrical shocks may be caused.
- Do not touch live terminals, otherwise electrical shocks may be caused.
- Do not touch terminals immediately after power is turned off, otherwise electrical shocks may be caused.
- When using ferrules, insert a wire to the bottom of the ferrule and crimp the ferrule.
- When connecting a stranded wire or multiple solid wires to a screw terminal block, use a ferrule. Otherwise the wire may slip off the screw terminal block.

Ferrules, Crimping Tool, and Screwdriver for Phoenix Terminal Blocks

The screw terminal block can be wired with or without using ferrules on the end of cable. Applicable ferrules for the Phoenix terminal blocks and crimping tool for the ferrules are listed below. The screwdriver is used for tightening the screw terminals on the MicroSmart modules. These ferrules, crimping tool, and screwdriver are made by Phoenix Contact and are available from Phoenix Contact.

Type numbers of the ferrules, crimping tool, and screwdriver listed below are the type numbers of Phoenix Contact. When ordering these products from Phoenix Contact, specify the Order No. and quantity listed below.

Ferrule Order No.



Quantity of Cables	Cable Size	Phoenix Type	Order No.	Pcs./Pkt.
For 1-wire connection	UL1007 AWG16	AI 1,5-8 BK	32 00 04 3	100
	UL1007 AWG18	AI 1-8 RD	32 00 03 0	100
	UL1015 AWG22	AI 0,5-8 WH	32 00 01 4	100
	UL2464 AWG24	AI 0,25-8 YE	32 03 03 7	100
For 2-wire connection	UL1007 AWG18	AI-TWIN 2 x 0,75-8 GY	32 00 80 7	100
	UL1015 AWG22	AI-TWIN 2 x 0,5-8 WH	32 00 93 3	100

Crimping Tool and Screwdriver Order No.

Tool Name		Phoenix Type	Order No.	Pcs./Pkt.
Crimping Tool		CRIMPFOX ZA 3	12 01 88 2	1
Screwdriver	For power supply terminals	SZS 0,6 x 3,5	12 05 05 3	10
	For I/O modules, communication adapter, communication module, expansion RS232C/RS485 communication modules	SZS 0,4 x 2,5	12 05 03 7	10

Screw Terminal Tightening Torque	CPU modules	0.5 N·m
	I/O modules Communication adapter Communication module Expansion RS232C/RS485 communication modules	0.22 to 0.25 N·m

4: OPERATION BASICS

Introduction

This chapter describes general information about setting up the basic MicroSmart system for programming, starting and stopping MicroSmart operation, and introduces simple operating procedures from creating a user program using WindLDR on a PC to monitoring the MicroSmart operation.

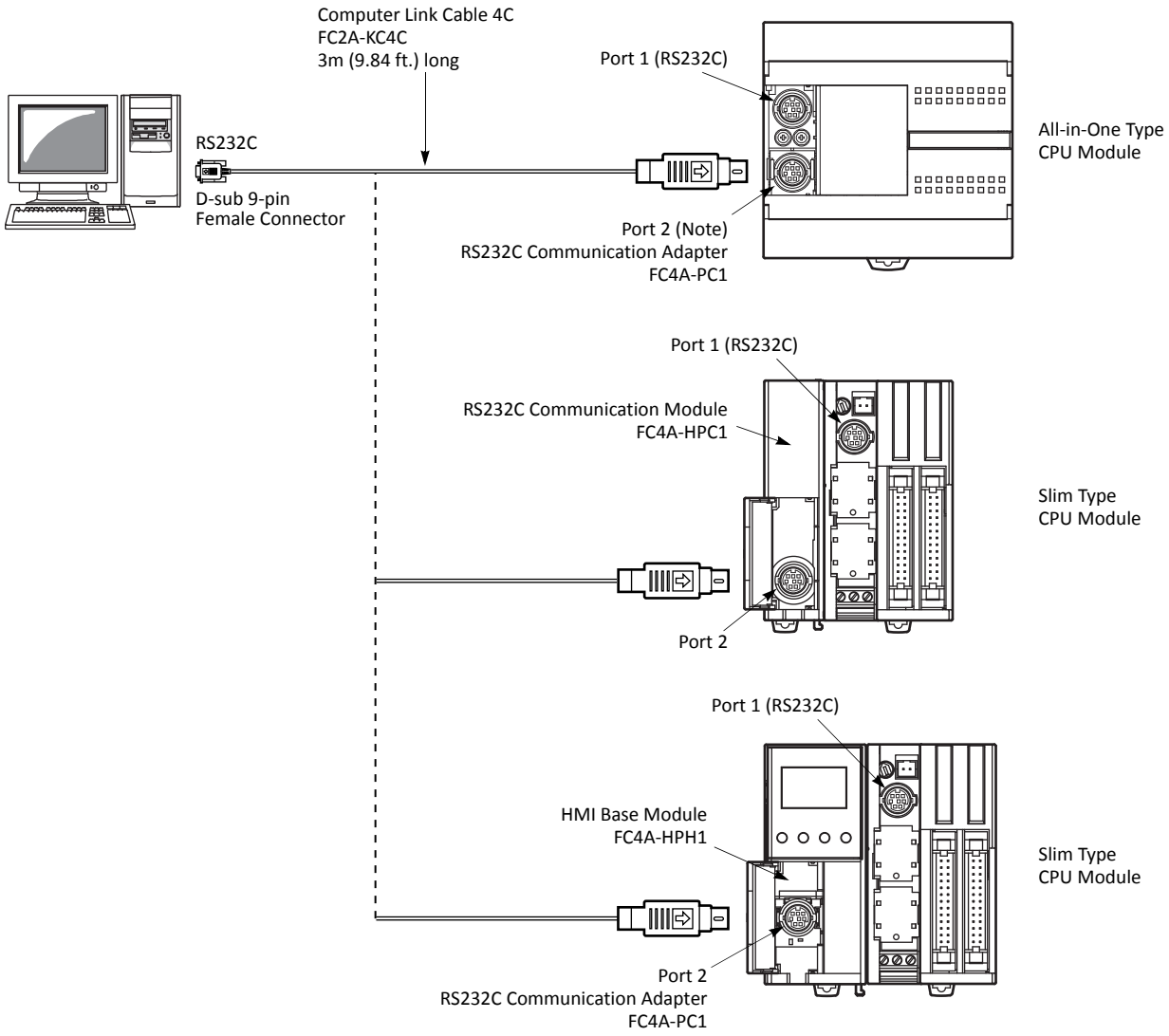
Connecting MicroSmart to PC (1:1 Computer Link System)

The MicroSmart can be connected to a Windows PC in two ways.

Computer Link through Port 1 or Port 2 (RS232C)

When connecting a Windows PC to the RS232C port 1 or port 2 on the MicroSmart CPU module, enable the maintenance protocol for the RS232C port using the Function Area Settings in WindLDR. See page 21-2 (Advanced Vol.).

To set up a 1:1 computer link system, connect a PC to the CPU module using the computer link cable 4C (FC2A-KC4C). The computer link cable 4C can be connected to port 1 directly. When connecting the cable to port 2 on the all-in-one type CPU module, install an optional RS232C communication adapter (FC4A-PC1) to the port 2 connector. When connecting to port 2 on the slim type CPU module, an optional RS232C communication module (FC4A-HPC1) is needed. The RS232C communication adapter can also be installed on the HMI base module (FC4A-HPH1).



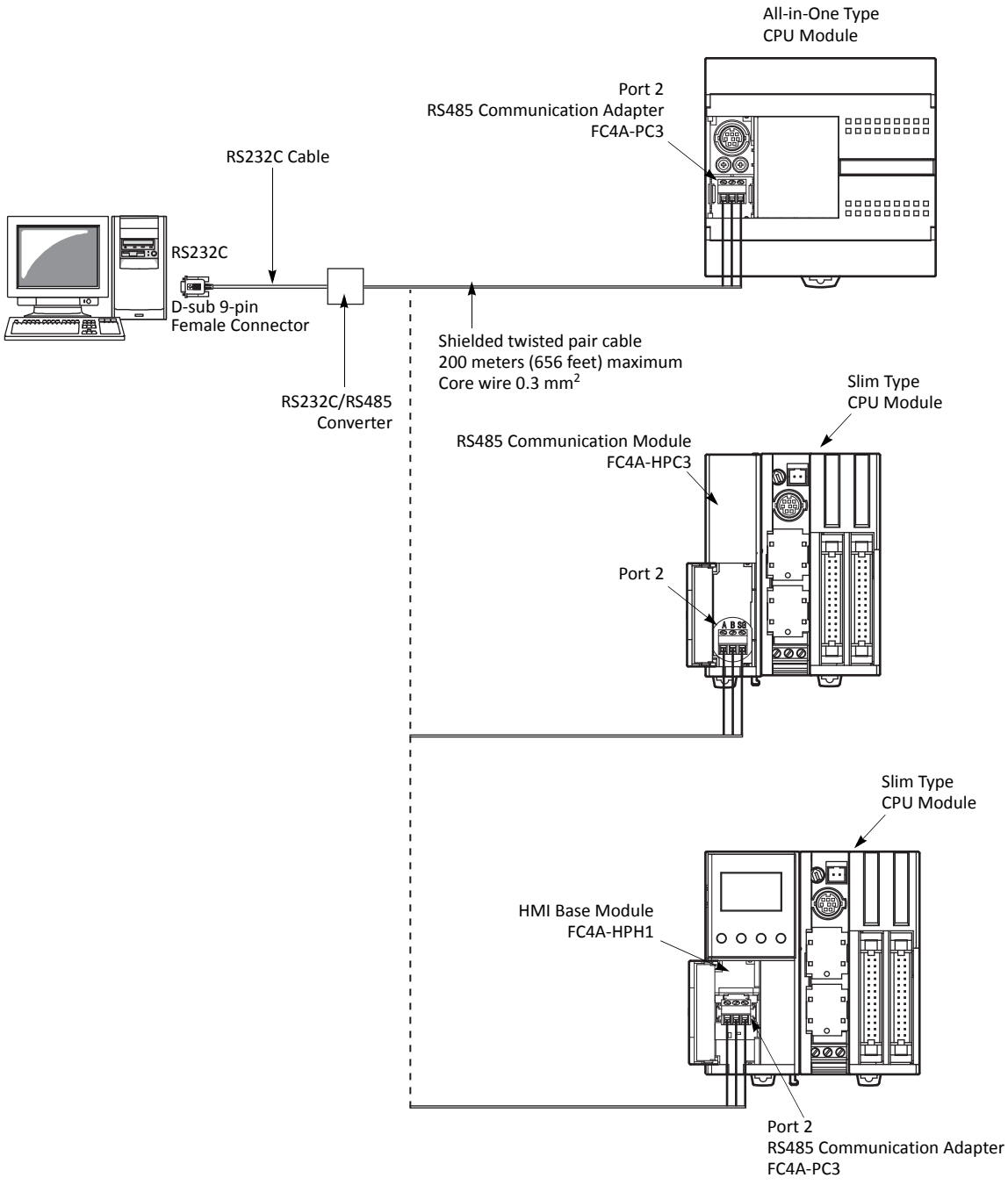
Computer Link through Port 2 (RS485)

When connecting a Windows PC to port 2 on the all-in-one type CPU module or slim type CPU module, enable the maintenance protocol for port 2 using the Function Area Settings in WindLDR. See page 21-2 (Advanced Vol.).

To set up a 1:1 computer link system using the all-in-one type CPU module, install an optional RS485 communication adapter (FC4A-PC3) to the port 2 connector. Connect a PC to the RS232C/RS485 converter using the RS232C cable. Connect the RS232C/RS485 converter to the CPU module using a shielded twisted pair cable. The RS232C/RS485 converter is powered by an 24V DC source or an AC adapter with 9V DC output. For details about the RS232C/RS485 converter, see page 21-4 (Advanced Vol.).

To set up a 1:1 computer link system using the slim type CPU module, an optional RS485 communication module (FC4A-HPC3) is needed. The RS485 communication adapter can also be installed on the HMI base module (FC4A-HPH1).

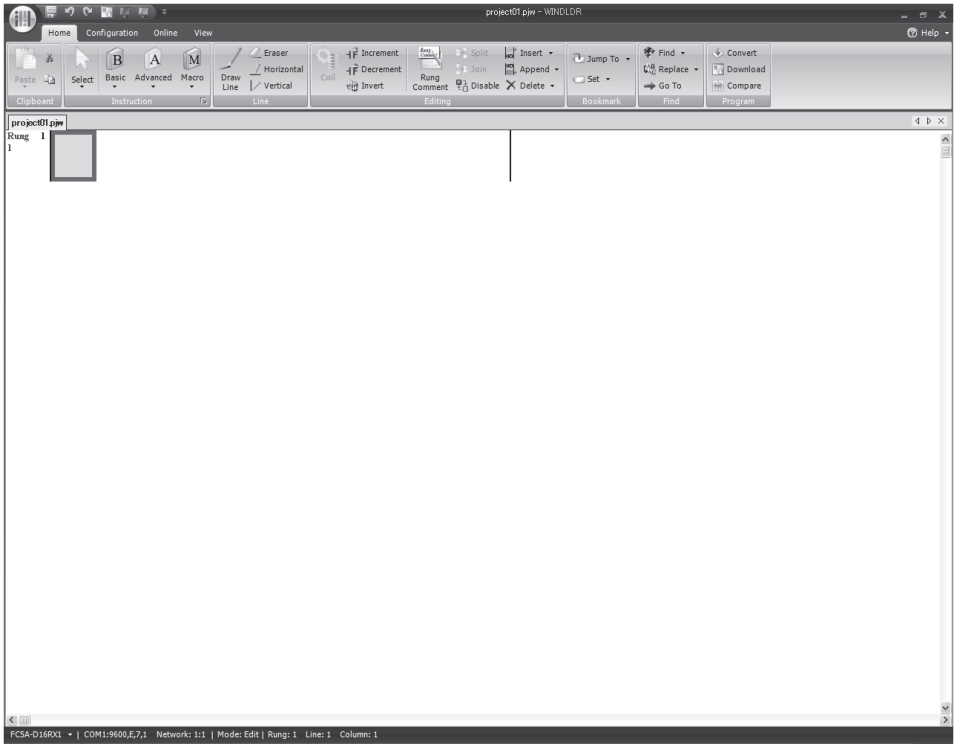
For setting up a 1:N computer link system, see page 21-1 (Advanced Vol.).



Start WindLDR

From the Start menu of Windows, select **Programs** > **Automation Organizer** > **WindLDR** > **WindLDR**.

WindLDR starts and a blank ladder editing screen appears with menus and tool bars shown on top of the screen.

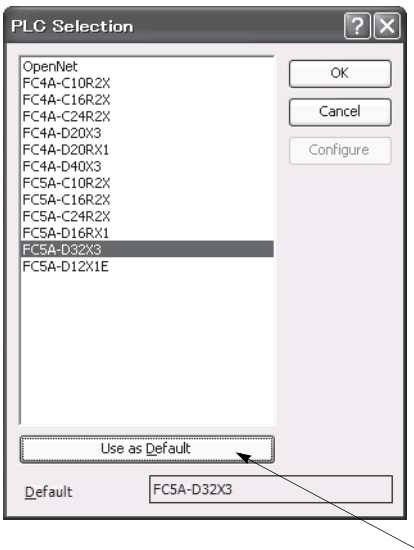


PLC Selection

Before programming a user program on WindLDR, select a PLC type.

1. Select **Configuration** from the WindLDR menu bar, then select **PLC Type**.

The PLC Selection dialog box appears.



PLC Selection Option	MicroSmart CPU Module Type No.
FC5A-C10R2X	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D
FC5A-C16R2X	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D
FC5A-C24R2X	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D
FC5A-D16RX1	FC5A-D16RK1 FC5A-D16RS1
FC5A-D32X3	FC5A-D32K3 FC5A-D32S3
FC5A-D12X1E	FC5A-D12K1E FC5A-D12S1E

2. Select a PLC type in the selection box.

Click **OK** to save the changes.

Press this button, then the same PLC will be selected as default when WindLDR is started next time.

Communication Port Settings for the PC

Depending on the communication port used, select the correct port in WindLDR.

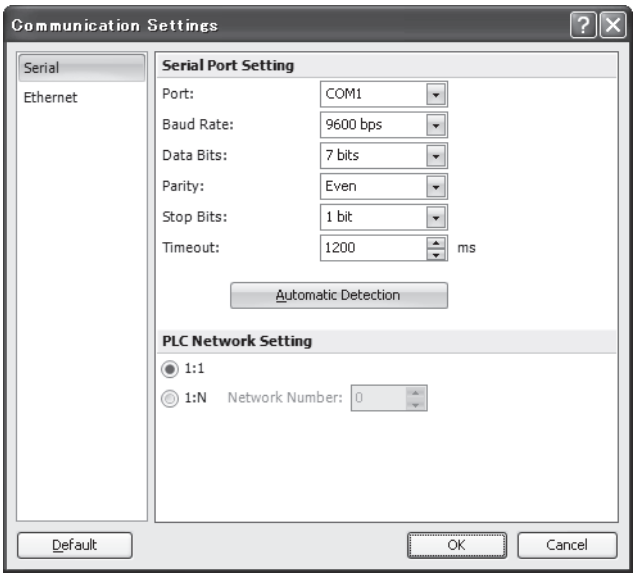
1. Select **Online** from the WindLDR menu bar, then select **Set Up**.

The Communication Settings dialog box appears.

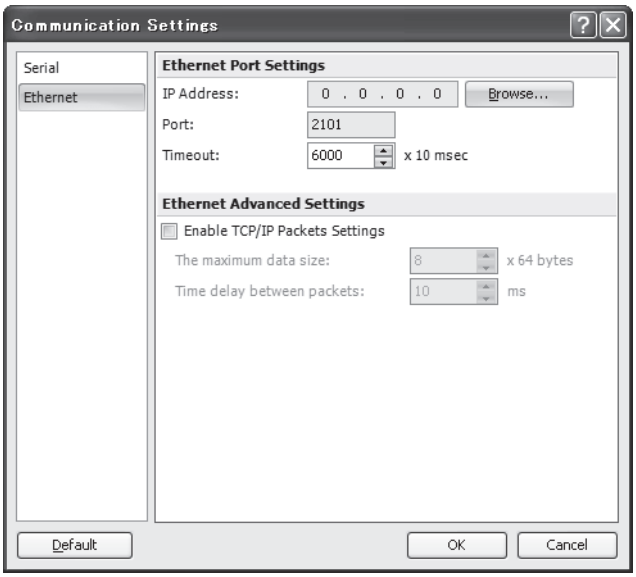
2. Select Serial Port in the Port selection box and click the **Automatic Detection** button.

Click **OK** to save the changes.

- **When Using a COM**



- **When Using Ethernet**



For details about the Ethernet communication settings, see the Web Server user's manual.

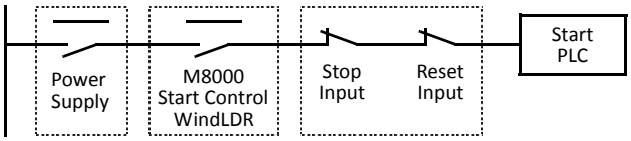
Start/Stop Operation

This section describes operations to start and stop the MicroSmart and to use the stop and reset inputs.

Caution
- Make sure of safety before starting and stopping the MicroSmart. Incorrect operation on the MicroSmart may cause machine damage or accidents.

Start/Stop Schematic

The start/stop circuit of the MicroSmart consists of three blocks; power supply, M8000 (start control special internal relay), and stop/reset inputs. Each block can be used to start and stop the MicroSmart while the other two blocks are set to run the MicroSmart.



Start/Stop Operation Using WindLDR

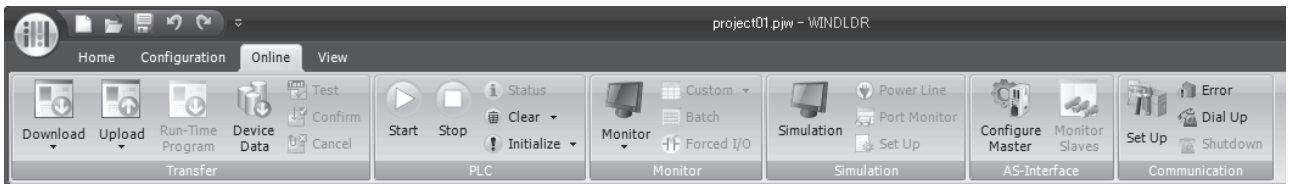
The MicroSmart can be started and stopped using WindLDR run on a Windows PC connected to the MicroSmart CPU module. When the **Start** button is pressed in the menu bar shown below, start control special internal relay M8000 is turned on to start the MicroSmart. When the **Stop** button is pressed, M8000 is turned off to stop the MicroSmart.

1. Connect the PC to the MicroSmart, start WindLDR, and power up the MicroSmart. See page 4-1.
2. Check that a stop input is not designated using **Configuration** > **Run/Stop Control** > **Stop and Reset Inputs**. See page 5-2.

Note: When a stop input is designated, the MicroSmart cannot be started or stopped by turning start control special internal relay M8000 on or off.

3. Select **Online** from the WindLDR menu bar.

The Online tab appears.



4. Click the **Start** button to start operation, then the start control special internal relay M8000 is turned on.
5. Click the **Stop** button to stop operation, then the start control special internal relay M8000 is turned off.

The PLC operation can also be started and stopped while WindLDR is in the monitor mode. Select **Online** > **Monitor** > **Monitor** and click the **Start** or **Stop** button.

Note: Special internal relay M8000 is a keep type internal relay and stores the status when power is turned off. M8000 retains its previous status when power is turned on again. However, when the backup battery is dead, M8000 loses the stored status, and can be turned on or off as programmed when the MicroSmart is powered up. The selection is made in **Configuration** > **Run/Stop Control** > **Run/Stop Selection at Memory Backup Error**. See page 5-3.

The backup duration is approximately 30 days (typical) at 25°C after the backup battery is fully charged.

Start/Stop Operation Using the Power Supply

The MicroSmart can be started and stopped by turning power on and off.

1. Power up the MicroSmart to start operation. See page 4-1.
2. If the MicroSmart does not start, check that start control special internal relay M8000 is on using WindLDR. If M8000 is off, turn it on. See page 4-5.
3. Turn power on and off to start and stop operation.

Note: If M8000 is off, the MicroSmart does not start operation when power is turned on. To start operation, turn power on, and turn M8000 on by clicking the **Start** button in WindLDR.

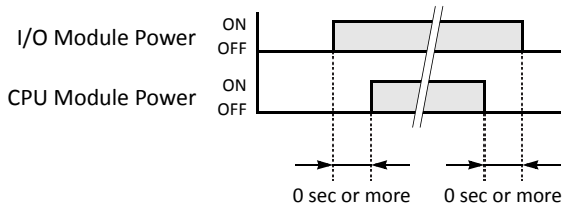
The response time of the MicroSmart at powerup depends on such factors as the contents of the user program, data link usage, and system setup. The table below shows an approximate time delay before starting operation after powerup.

Response time when no data link is used:

Program Size	After powerup, the CPU starts operation in
4,800 bytes (800 steps)	Approx. 0.5 second
15,000 bytes (2,500 steps)	Approx. 1.2 seconds
27,000 bytes (4,500 steps)	Approx. 2 seconds
62,400 bytes (10,400 steps)	Approx. 5 seconds

Order of Powerup and Powerdown

To ensure I/O data transfer, power up the I/O modules first, followed by the CPU module, or power up the CPU and I/O modules at the same time. When shutting down the system, power down the CPU first, followed by I/O modules, or power down the CPU and I/O modules at the same time.



Start/Stop Operation Using Stop Input and Reset Input

Any input terminal available on the CPU module can be designated as a stop or reset input using the Function Area Settings. The procedure for selecting stop and reset inputs is described on page 5-2.

Note: When using a stop and/or reset input to start and stop operation, make sure that start control special internal relay M8000 is on. If M8000 is off, the CPU does not start operation when the stop or reset input is turned off. M8000 is not turned on or off when the stop and/or reset input is turned on or off.

When a stop or reset input is turned on during program operation, the CPU stops operation, the RUN LED is turned off, and all outputs are turned off.

The reset input has priority over the stop input.

System Statuses at Stop, Reset, and Restart

The system statuses during running, stop, reset, and restart after stopping are listed below:

Mode	Output	Internal Relay, Shift Register, Counter, Data Register, Expansion DR, Extra DR		Timer Current Value
		Keep Type	Clear Type	
Run	Operating	Operating	Operating	Operating
Stop (Stop input ON)	OFF	Unchanged	Unchanged	Unchanged
Reset (Reset input ON)	OFF	OFF/Reset to zero	OFF/Reset to zero	Reset to zero
Restart	Unchanged	Unchanged	OFF/Reset to zero	Reset to preset

Note: Expansion data registers are available on slim type CPU modules. All expansion data registers are keep types.

Simple Operation

This section describes how to edit a simple program using WindLDR on a PC, transfer the program from the PC to the MicroSmart, run the program, and monitor the operation on the WindLDR screen.

Connect the MicroSmart to the PC as described on page 4-1.

Sample User Program

Create a simple program using WindLDR. The sample program performs the following operation:

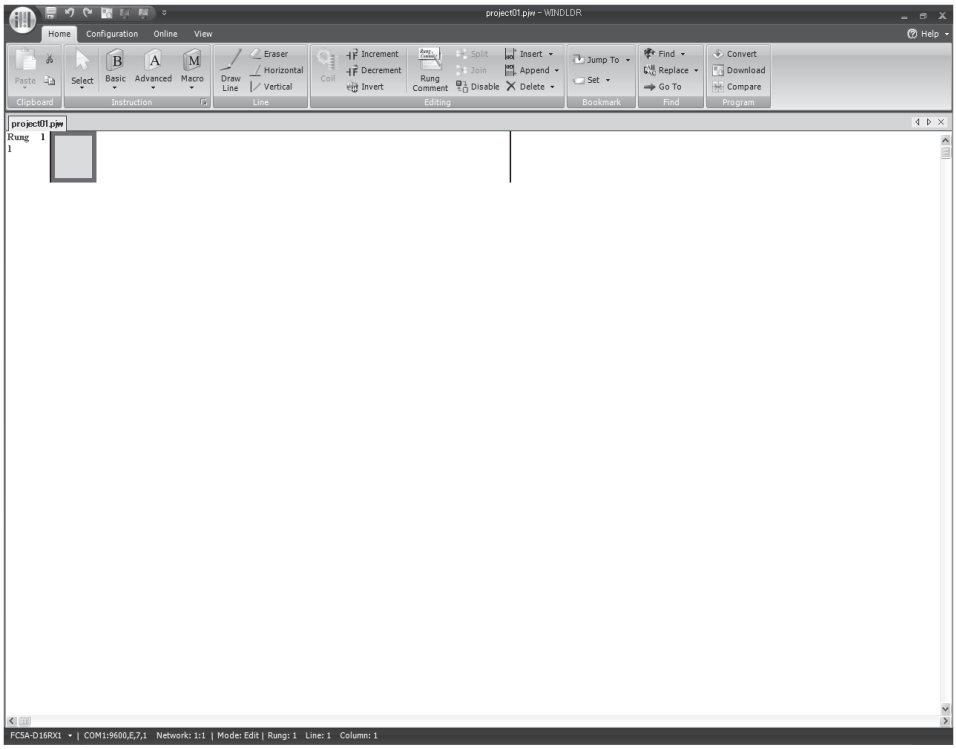
When only input I0 is turned on, output Q0 is turned on.
When only input I1 is turned on, output Q1 is turned on.
When both inputs I0 and I1 are turned on, output Q2 flashes in 1-sec increments.

Rung No.	Input I0	Input I1	Output Operation
1	ON	OFF	Output Q0 is turned ON.
2	OFF	ON	Output Q1 is turned ON.
3	ON	ON	Output Q2 flashes in 1-sec increments.

Start WindLDR

From the Start menu of Windows, select **Programs** > **Automation Organizer** > **WindLDR** > **WindLDR**.

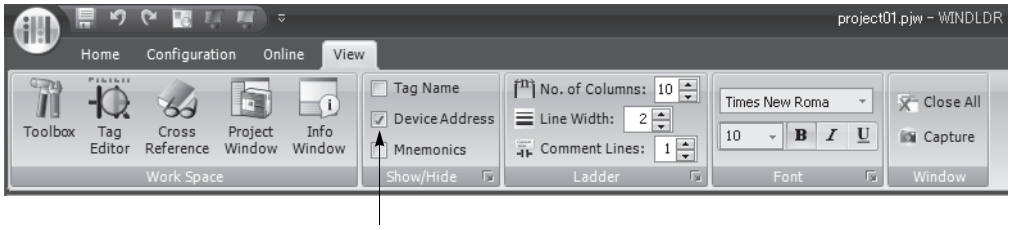
WindLDR starts and a blank ladder editing screen appears with menus and tool bars shown on top of the screen.



Disable Tag Function

The following example describes a simple procedure without using the tag function.

From the WindLDR menu bar, select **View**, then click the check box of Device Address.

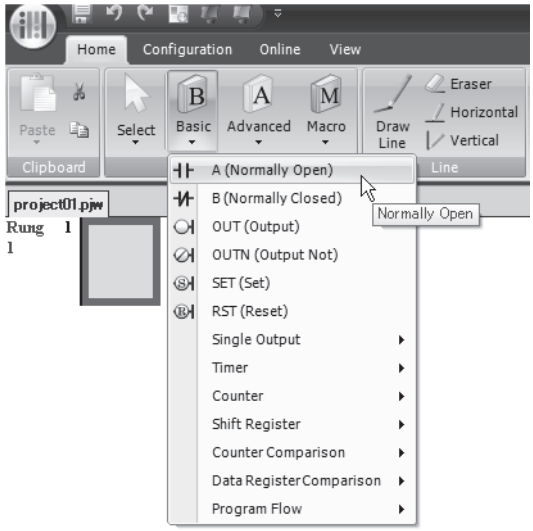


Check the Device Address check box.

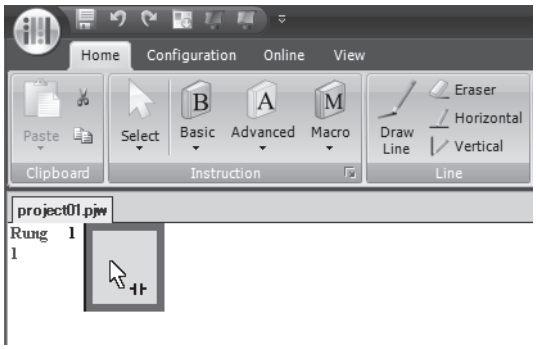
Edit User Program Rung by Rung

Start the user program with the LOD instruction by inserting a NO contact of input I0.

1. From the WindLDR menu bar, select **Home** > **Basic** > **A (Normally Open)**.



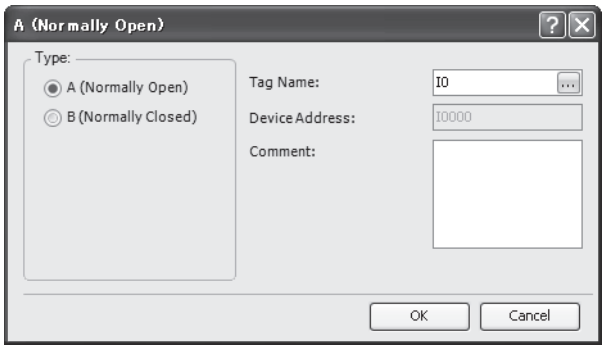
2. Move the mouse pointer to the first column of the first line where you want to insert a NO contact, and click the left mouse button.



Note: Another method to insert a NO (or NC) contact is to move the mouse pointer where you want to insert the contact, and type A (or B).

The Normally Open dialog box appears.

3. Enter **I0** in the Tag Name field, and click **OK**.



A NO contact of input I0 is programmed in the first column of the first ladder line.

Next, program the ANDN instruction by inserting a NC contact of input I1.

4. From the WindLDR menu bar, select **Home** > **Basic** > **B (Normally Closed)**.

5. Move the mouse pointer to the second column of the first ladder line where you want to insert a NC contact, and click the left mouse button.

The Normally Closed dialog box appears.

6. Enter **I1** in the Tag Name field, and click **OK**.

A NC contact of input I1 is programmed in the second column of the first ladder line.

At the end of the first ladder line, program the OUT instruction by inserting a NO coil of output Q0.

7. From the WindLDR menu bar, select **Home** > **Basic** > **OUT (Output)**.

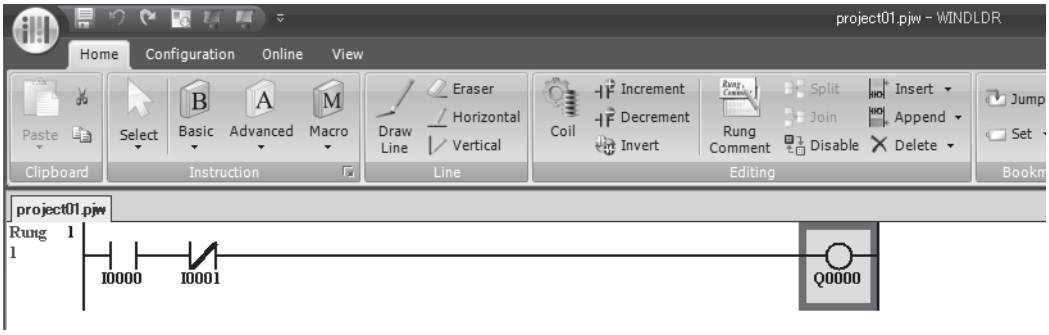
8. Move the mouse pointer to the third column of the first ladder line where you want to insert an output coil, and click the left mouse button.

Note: Another method to insert an instruction (either basic or advanced) is to type the instruction symbol, OUT, where you want to insert the instruction.

The Output dialog box appears.

9. Enter **Q0** in the Tag Name field, and click **OK**.

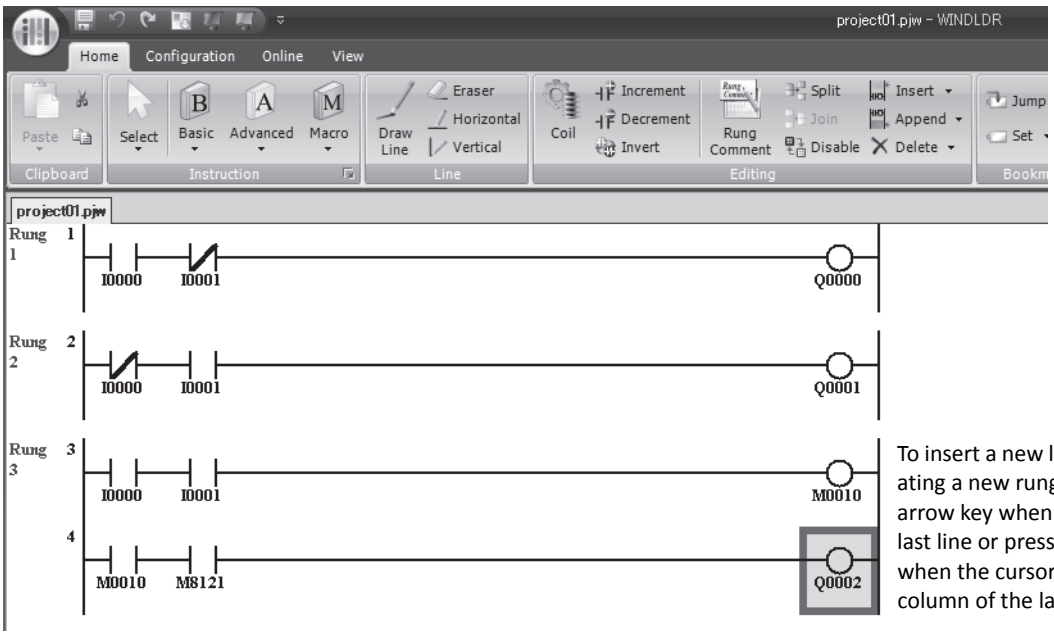
A NO output coil of output Q0 is programmed in the right-most column of the first ladder line. This completes programming for rung 1.



Continue programming for rungs 2 and 3 by repeating similar procedures.

A new rung is inserted by pressing the **Enter** key while the cursor is on the preceding rung. A new rung can also be inserted by selecting **Home** > **Append** > **Append a Rung**.

When completed, the ladder program looks like below.



To insert a new ladder line without creating a new rung, press the down arrow key when the cursor is on the last line or press the right arrow key when the cursor is at the right-most column of the last line.

The ladder program can be checked whether it contains any user program syntax error.

10. From the menu bar, select **Home** > **Convert (above Program)**.

When the instruction symbols are connected correctly, conversion is completed successfully. If any error is found, the errors are listed on the screen. Then, make corrections as necessary.

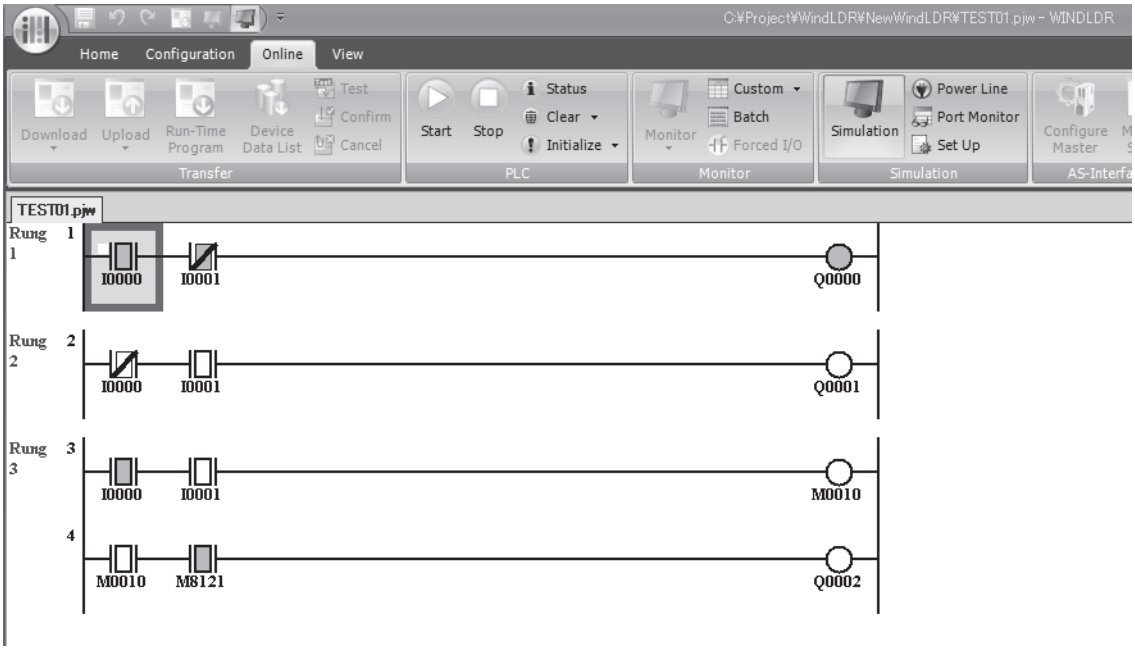
Now, save the file with a new name.

11. Select the WindLDR application button at the upper-left corner of the WindLDR screen, followed by **Save**, and type **TEST01** in the File Name field. Change the Folder or Drive as necessary.

Simulate Operation

Before downloading the user program, you can simulate the operation on the WindLDR screen without connecting the MicroSmart.

From the WindLDR menu bar, select **Online** > **Simulation**. The Simulation screen appears.



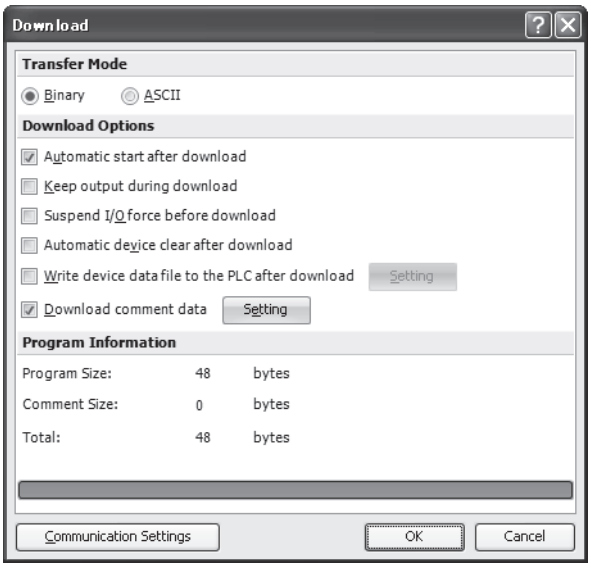
To change an input status, place the mouse pointer on the input and right-click the mouse. In the pop-up menu, select Set or Reset to set or reset the input.

To quit simulation, from the WindLDR menu bar, select **Online** > **Simulation**.

Download Program

You can download the user program from WindLDR running on a PC to the MicroSmart.

From the WindLDR menu bar, select **Online** > **Download**. The Download Dialog appears, then click the **OK** button. The user program is downloaded to the MicroSmart.



Note: The Download Dialog is also shown by selecting **Home** > **Download**.

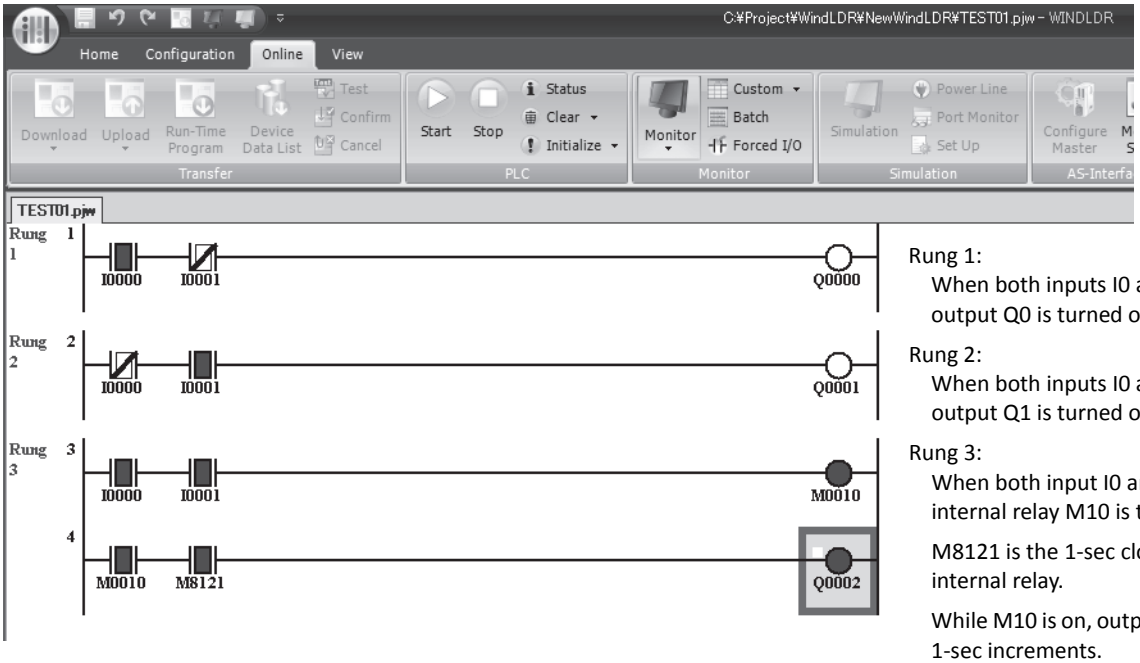
Note: When downloading a user program, all values and selections in the Function Area Settings are also downloaded to the MicroSmart. For Function Area Settings, see pages 5-1 through 5-44.

Monitor Operation

Another powerful function of WindLDR is to monitor the PLC operation on the PC. The input and output statuses of the sample program can be monitored in the ladder diagram.

From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**.

When both inputs I0 and I1 are on, the ladder diagram on the monitor screen looks as follows:



Rung 1:
When both inputs I0 and I1 are on, output Q0 is turned off.

Rung 2:
When both inputs I0 and I1 are on, output Q1 is turned off.

Rung 3:
When both input I0 and I1 are on, internal relay M10 is turned on.

M8121 is the 1-sec clock special internal relay.

While M10 is on, output Q2 flashes in 1-sec increments.

Quit WindLDR

When you have completed monitoring, you can quit WindLDR either directly from the monitor screen or from the editing screen. In both cases, from the WindLDR application button, click **Exit WindLDR**.

5: SPECIAL FUNCTIONS

Introduction

The MicroSmart features special functions such as stop/reset inputs, run/stop selection at memory backup error, keep designation for internal relays, shift registers, counters, and data registers. These functions are programmed using the Function Area Settings menu. Also included in the Function Area Settings are high-speed counter, catch input, interrupt input, communication protocol selection for port 1 through port 7, input filter, and user program read/write protection.

This chapter describes these special functions. Clock function, analog potentiometer function, memory cartridge, and constant scan features are also described in this chapter.

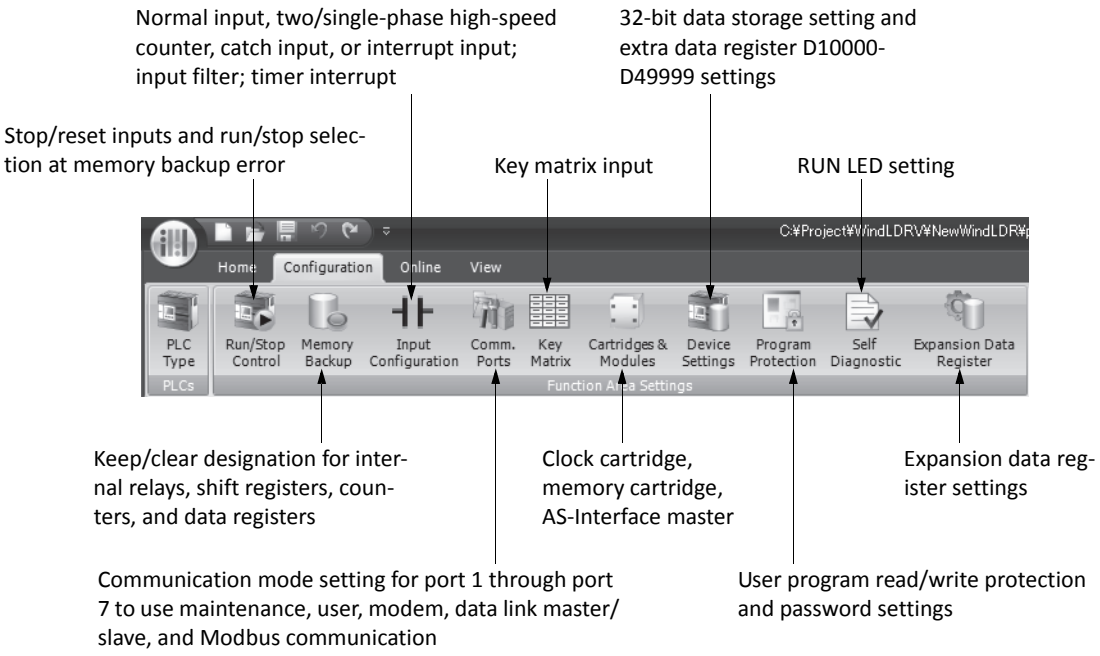
The Function Area Settings for communication functions are detailed in chapters 10 through 12 (Basic Vol.) and 21 through 25 (Advanced Vol.).

Caution

- Since all Function Area Settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Function Area Settings

Various special functions are programmed in the Function Area Settings. To call the Function Area Settings dialog box, start WindLDR on a Windows PC. From the WindLDR menu bar, select **Configuration**, then the Function Area Settings menu appears.



Detailed information is described on the following pages.

Stop Input and Reset Input

As described on page 4-5, the MicroSmart can be started and stopped using a stop input or reset input, which can be designated from the Function Area Settings menu. When the designated stop or reset input is turned on, the MicroSmart stops operation. For the system statuses in the stop and reset modes, see page 4-6.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Run/Stop Control**.

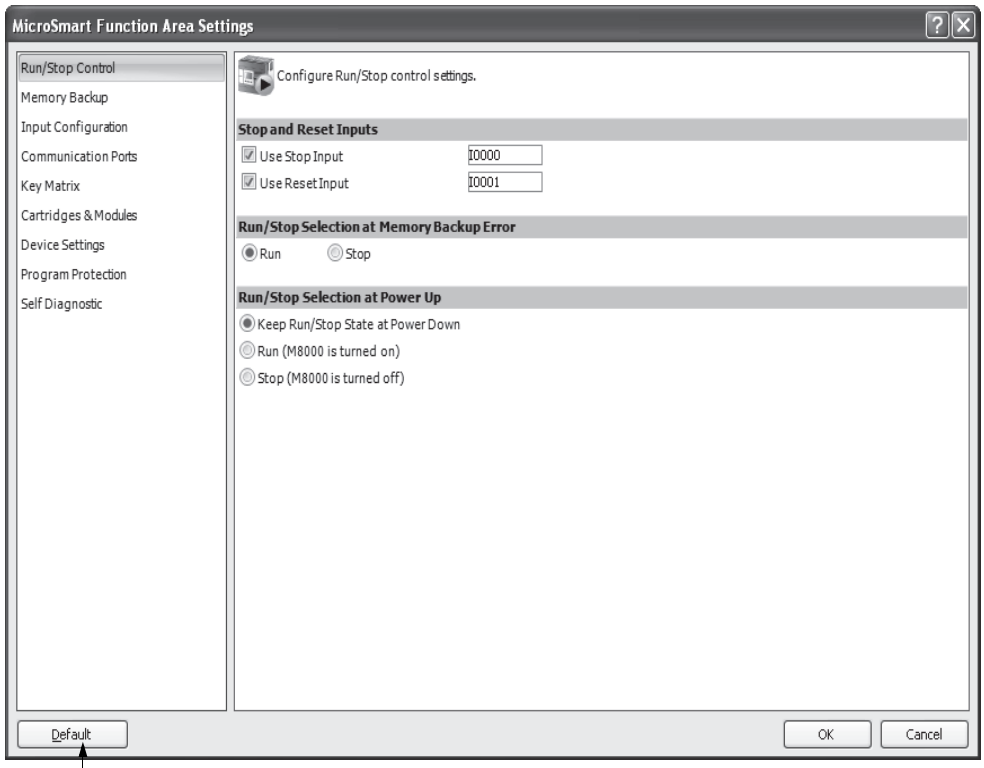
The Function Area Settings dialog box for Run/Stop Control appears.

2. Click the check box under the Stop and Reset Inputs.

Stop Input: Click the check box on the left of Use Stop Input and type a desired input number available on the CPU module in the Stop Input field.

Reset Input: Click the check box on the left of Use Reset Input and type a desired reset number available on the CPU module in the Reset Input field.

This example designates input I0 as a stop input and input I1 as a reset input.



Resets all Function Area Settings values to defaults.

Default: No stop and reset inputs are designated.

3. Click the **OK** button.

Run/Stop Selection at Memory Backup Error

Start control special internal relay M8000 maintains its status when the CPU is powered down. After the CPU has been off for a period longer than the battery backup duration, the data designated to be maintained during power failure is broken. The Run/Stop Selection at Memory Backup Error dialog box is used to select whether to start or stop the CPU when attempting to restart operation after the “keep” data in the CPU RAM has been lost.

When memory backup error occurs, Run/Stop Selection at Memory Backup Error is preferred than Run/Stop Selection at Power Up.

When a built-in lithium battery is fully charged, data of internal relays, shift registers, counters, and data registers stored in the RAM are maintained for approximately 30 days.

Since this setting relates to the user program, the user program must be downloaded to the MicroSmart after changing this setting.

Programming WindLDR

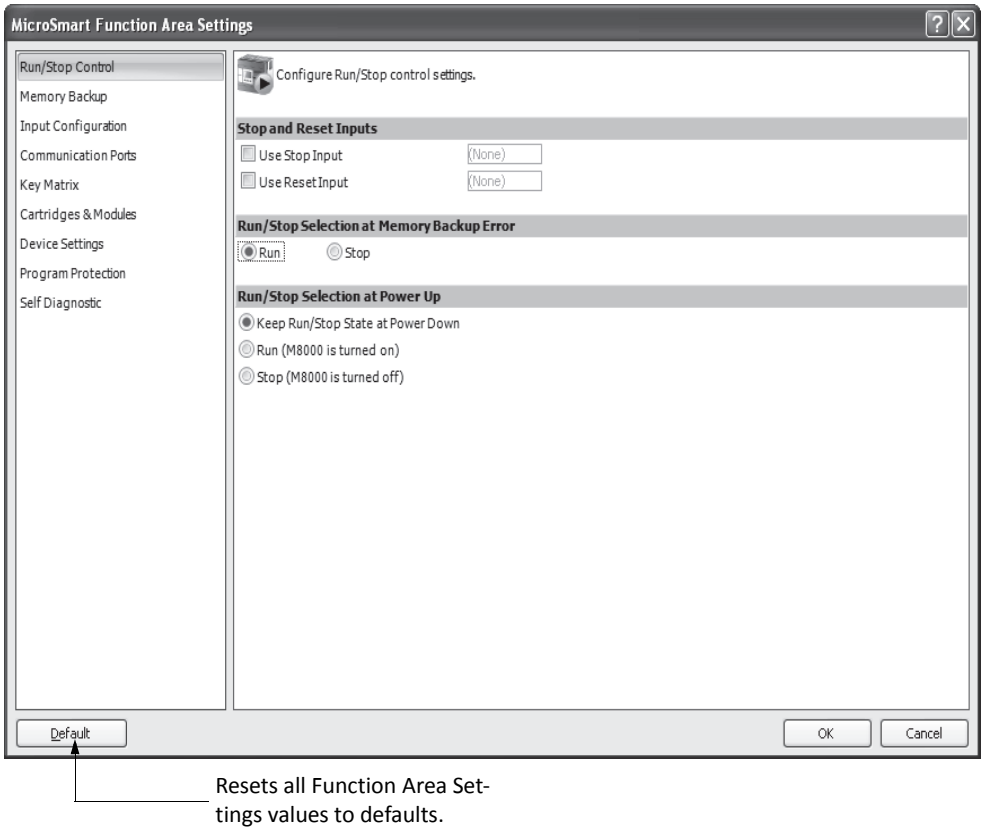
1. From the WindLDR menu bar, select **Configuration** > **Run/Stop Control**.

The Function Area Settings dialog box for Run/Stop Control appears.

2. Click the Run or Stop button.

Run (Default): Click the button on the left to start the CPU at memory backup error.

Stop: Click the button on the right to stop the CPU when attempting to start at memory backup error.
When the CPU does not start because of the Stop selection, the CPU can not be started alone, then the CPU can still be started by sending a start command from WindLDR to turn on start control special internal relay M8000.
For start/stop operation, see page 4-5.



Resets all Function Area Settings values to defaults.

3. Click the **OK** button.

Run/Stop Selection at Power Up

Start control special internal relay M8000 maintains its status when the CPU module is powered down. When powered up, the CPU module is started or stopped according to the M8000 status. The Run/Stop Selection at Power Up is used to select whether to start or stop the CPU module regardless of the M8000 status when the CPU is powered up.

When a memory cartridge is installed on a CPU module, the CPU module is started or stopped according to the M8000 status of the CPU module. The CPU module can always be started regardless of the M8000 status by using Run/Stop Selection at Power Up. WindLDR software is not needed to start the CPU module.

Stop and Reset inputs have priority over start control special internal relay M8000. When the memory backup error occurs, the CPU module is started or stopped according to Run/Stop Selection at Memory Backup Error regardless of Run/Stop Selection at Power Up. For start/stop operation, see page 4-5.

Since this settings relate to the user program, the user program must be downloaded to the MicroSmart after changing this settings.

The Run/Stop Selection at Power Up can be used with the CPU module system program version 220 or higher.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Run/Stop Control**.

The Function Area Settings dialog box for Run/Stop Control appears.

2. Click the button under Run/Stop Selection at Power Up.

Keep Run/Stop State at Power Down (Default)

Click this button to keep the run/stop status at power down when the CPU module is powered up.

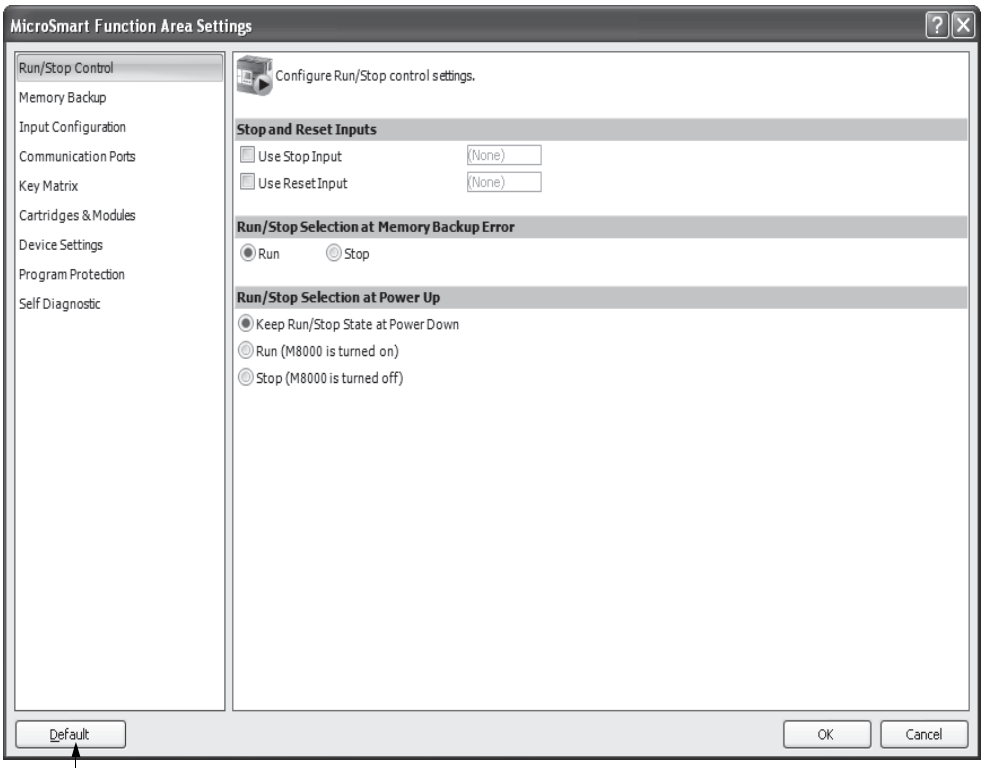
Run (M8000 is turned on):

Click this button to always start the CPU module when the CPU module is powered up.

Stop (M8000 is turned off):

Click this button to always stop the CPU module when the CPU module is powered up.

This example designates Keep Run/Stop Status at Power Down.



Resets all Function Area Settings values to defaults.

3. Click the **OK** button.

Keep Designation for Internal Relays, Shift Registers, Counters, and Data Registers

The statuses of internal relays and shift register bits are usually cleared at startup. It is also possible to designate all or a block of consecutive internal relays or shift register bits as “keep” types. Counter current values and data register values are usually maintained at powerup. It is also possible to designate all or a block of consecutive counters and data registers as “clear” types.

When the CPU is stopped, these statuses and values are maintained. When the CPU is reset by turning on a designated reset input, these statues and values are cleared despite the settings in the Configure Keep/Clear Settings dialog box shown below. The keep/clear settings in this dialog box have effect when restarting the CPU.

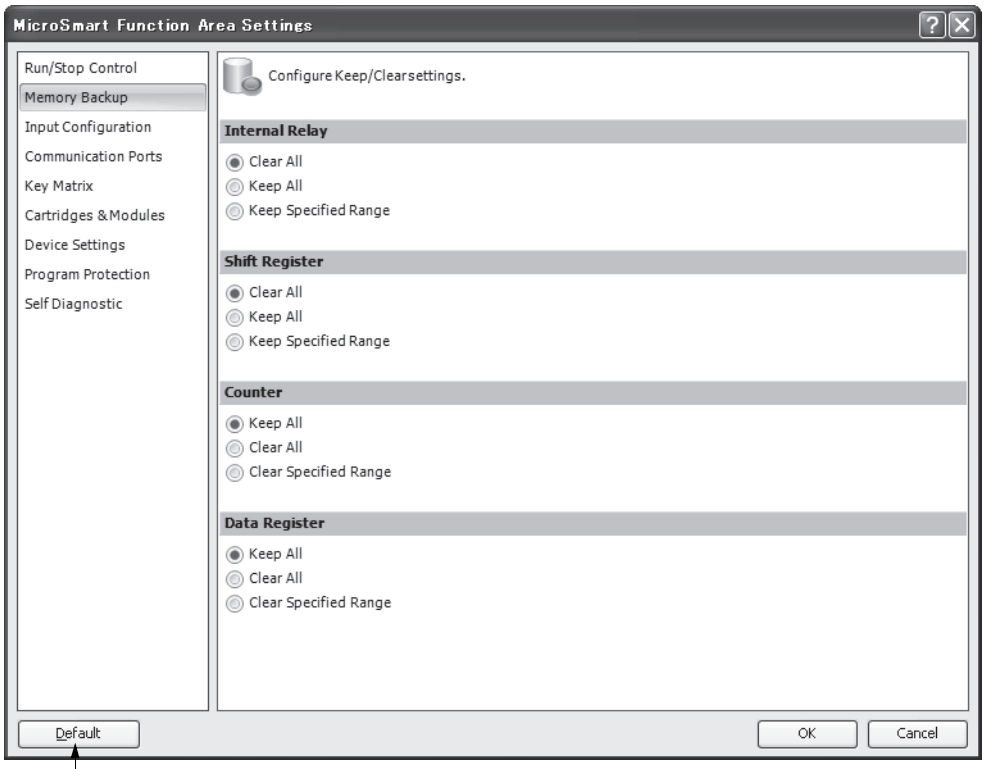
Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Memory Backup**.

The Function Area Settings dialog box for Configure Keep/Clear Settings appears.

2. Click the buttons under Internal Relay, Shift Register, Counter, and Data Register to clear all, keep all, or keep/clear specified range as required.



Resets all Function Area Settings values to defaults.

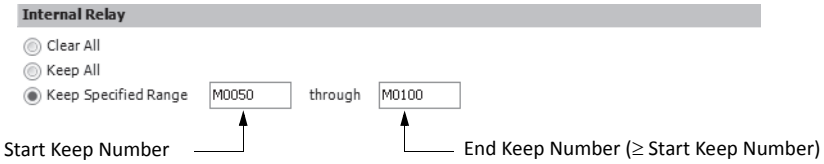
Internal Relay 'Keep' Designation

Clear All: All internal relay statuses are cleared at startup (default).

Keep All: All internal relay statuses are maintained at startup.

Keep Specified Range: A specified range of internal relays are maintained at startup. Enter the start "keep" number in the left field and the end "keep" number in the right field. The start "keep" number must be smaller than or equal to the end "keep" number.

Valid internal relay numbers are M0 through M2557. Special internal relays cannot be designated.



When a range of M50 through M100 is designated as shown in the example above, M50 through M100 are keep types, M0 through M47 and M101 through M2557 are clear types.

Shift Register 'Keep' Designation

Clear All: All shift register bit statuses are cleared at startup (default).

Keep All: All shift register bit statuses are maintained at startup.

Keep Specified Range: A specified range of shift register bits are maintained at startup. Enter the start "keep" number in the left field and the end "keep" number in the right field. The start "keep" number must be smaller than or equal to the end "keep" number.

Valid shift register bit numbers are R0 through R255.

When a range of R17 through R32 is designated, R17 through R32 are keep types, R0 through R16 and R33 through R255 are clear types.

Counter 'Clear' Designation

Keep All: All counter current values are maintained at startup (default).

Clear All: All counter current values are cleared at startup.

Clear Specified Range: A specified range of counter current values are cleared at startup. Enter the start "clear" number in the left field and the end "clear" number in the right field. The start "clear" number must be smaller than or equal to the end "clear" number.

Valid counter numbers are C0 through C255.

When a range of C0 through C10 is designated, C0 through C10 are clear types, and C11 through C255 are keep types.

Data Register 'Clear' Designation

Keep All: All data register values are maintained at startup (default).

Clear All: All data register values are cleared at startup.

Clear Specified Range: A specified range of data register values are cleared at startup. Enter the start "clear" number in the left field and the end "clear" number in the right field. The start "clear" number must be smaller than or equal to the end "clear" number.

Valid data register numbers are D0 through D1999. Special data registers and expansion data registers cannot be designated. All expansion data registers are keep types.

On slim type CPU modules, extra data registers D10000 through D49999 can be enabled in the Function Area Settings. All extra data registers are keep types.

When a range of D100 through D1999 is designated, D0 through D99 are keep types, and D100 through D1999 are clear types.

High-speed Counter

This section describes the high-speed counter function to count many pulse inputs within one scan. Using the built-in 16-bit high-speed counter, the all-in-one type CPU module counts up to 65,535 high-speed pulses. Using the built-in 32-bit high-speed counter, the slim type CPU module counts up 4,294,967,295 pulses.

The high-speed counter counts input pulses from a rotary encoder or proximity switch without regard to the scan time, compares the current value with a preset value, and turns on the output when the current value reaches the preset value. This function can be used for simple motor control or to measure lengths of objects.

The all-in-one type CPU modules and slim type CPU modules have different high-speed counter configurations.

CPU Module	**All-in One Type CPU Module**		
High-speed Counter No.	**HSC1**		**HSC2, HSC3, HSC4**
Operation Mode	Single-phase	Two-phase	Single-phase
Counting Mode	Adding counter	1-edge count	Adding counter
Maximum Counting Frequency	50 kHz		5 kHz
Counting Range	0 to 65,535 (16 bits)		
Current Value Comparison	Preset value	Overflow Underflow	Preset value
Comparison Action	Comparison output		
Reset Input	With		Without
Reset Special Internal Relay	With		
Current Value after Reset	0	Reset value	0

CPU Module	**Slim Type CPU Module**		
High-speed Counter No.	**HSC1, HSC4**		**HSC2, HSC3**
Operation Mode	Single-phase	Two-phase	Single-phase
Counting Mode	Adding counter Dual-pulse reversible Up/down selection reversible	1-edge count 2-edge count 4-edge count	Adding counter
Maximum Counting Frequency	100 kHz	1-edge count: 100 kHz 2-edge count: 50 kHz 4-edge count: 25 kHz	100 kHz
Counting Range	0 to 4,294,967,295 (32 bits)		
Current Value Comparison	Preset value 1 Preset value 2 Overflow Underflow		Preset value
Comparison Action	Comparison output Interrupt program		
Reset Input	With		Without
Reset Special Internal Relay	With		
Current Value after Reset	Reset value		0

High-speed counters are programmed in the Function Area Settings in WindLDR and allocated to input terminals I0 through I5 (all-in-one type CPU module) or I7 (slim type CPU module) in four groups. When high-speed counters are used, input terminals in the same group cannot be used for ordinary inputs, catch inputs, or interrupt inputs.

High-speed Counters on All-in-One Type CPU Modules

All-in-one type CPU modules have four 16-bit high-speed counters; HSC1 through HSC4, which can count up to 65,535. HSC1 can be used as a single-phase or two-phase 50-kHz high-speed counter. HSC2 through HSC4 are single-phase 5-kHz high-speed counters. All high-speed counter functions are selected using the Function Area Settings in WindLDR.

High-speed Counter Operation Modes and Input Terminals (All-in-One Type CPU Modules)

High-speed counters HSC1 through HSC4 are allocated input terminals as listed in the following table.

High-speed Counter No.	HSC1			HSC2	HSC3	HSC4
Input Terminal (Note 1)	I0	I1	I2	I3	I4	I5
Single-phase High-speed Counter	(Note 2)	Pulse Input	Reset Input (Note 3)	Pulse Input	Pulse Input	Pulse Input
Two-phase High-speed Counter	Phase A	Phase B	Reset Input (Phase Z) (Note 3)	—	—	—

Note 1: When the voltage difference between the input terminal and the COM terminal is 24V DC, the input turns on. Both positive and negative input voltages are accepted.
Note 2: Input I0 can be used as an ordinary input terminal.
Note 3: When a reset input is not used, input I2 can be used as an ordinary input terminal.

Single-phase High-speed Counters HSC1 through HSC4 (All-in-One Type CPU Modules)

HSC1 can be used as a single-phase high-speed counter as well as HSC2 through HSC4. The four single-phase high-speed counters count input pulses to the input terminal allocated to each high-speed counter. When the preset value is reached, a designated comparison output turns on, and the current value is reset to 0 to count subsequent input pulses.

Five special internal relays and two special data registers are assigned to control and monitor each single-phase high-speed counter operation. The current value is stored in a special data register (current value) and is updated every scan. The value stored in another special data register (preset value) is used as a preset value. When a reset input special internal relay is turned on, the current value is reset to 0.

The single-phase high-speed counter is enabled while a gate input special internal relay is on and is disabled while the gate input is off. When the current value reaches the preset value, a special internal relay (comparison ON status) turns on in the next scan. At this point, the current value is reset to 0, and the value stored in a preset value special data register takes effect for the subsequent counting cycle. When a comparison output reset special internal relay is turned on, the designated comparison output is turned off.

In addition, only the single-phase high-speed counter HSC1 has reset input I2 and reset status special internal relay M8130. When reset input I2 is turned on to reset the current value to 0, reset status special internal relay M8130 turns on in the next scan. When reset input special internal relay M8032 is turned on, M8130 does not turn on. See page 5-9.

Special Internal Relays for Single-phase High-speed Counters (All-in-One Type CPU Modules)

Description	High-speed Counter No.				ON	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Comparison Output Reset	M8030	M8034	M8040	M8044	Turns off comparison output	R/W
Gate Input	M8031	M8035	M8041	M8045	Enables counting	R/W
Reset Input	M8032	M8036	M8042	M8046	Resets the current value	R/W
Reset Status	M8130	—	—	—	Current value reset by I2	Read only
Comparison ON Status	M8131	M8133	M8134	M8136	Preset value reached	Read only

Note: Special internal relays M8130, M8131, M8133, M8134, and M8136 go on for only one scan.

Special Data Registers for Single-phase High-speed Counters (All-in-One Type CPU Modules)

Description	High-speed Counter No.				Updated	Read/Write
	HSC1	HSC2	HSC3	HSC4		
High-speed Counter Current Value	D8045	D8047	D8049	D8051	Every scan	Read only
High-speed Counter Preset Value	D8046	D8048	D8050	D8052	—	R/W

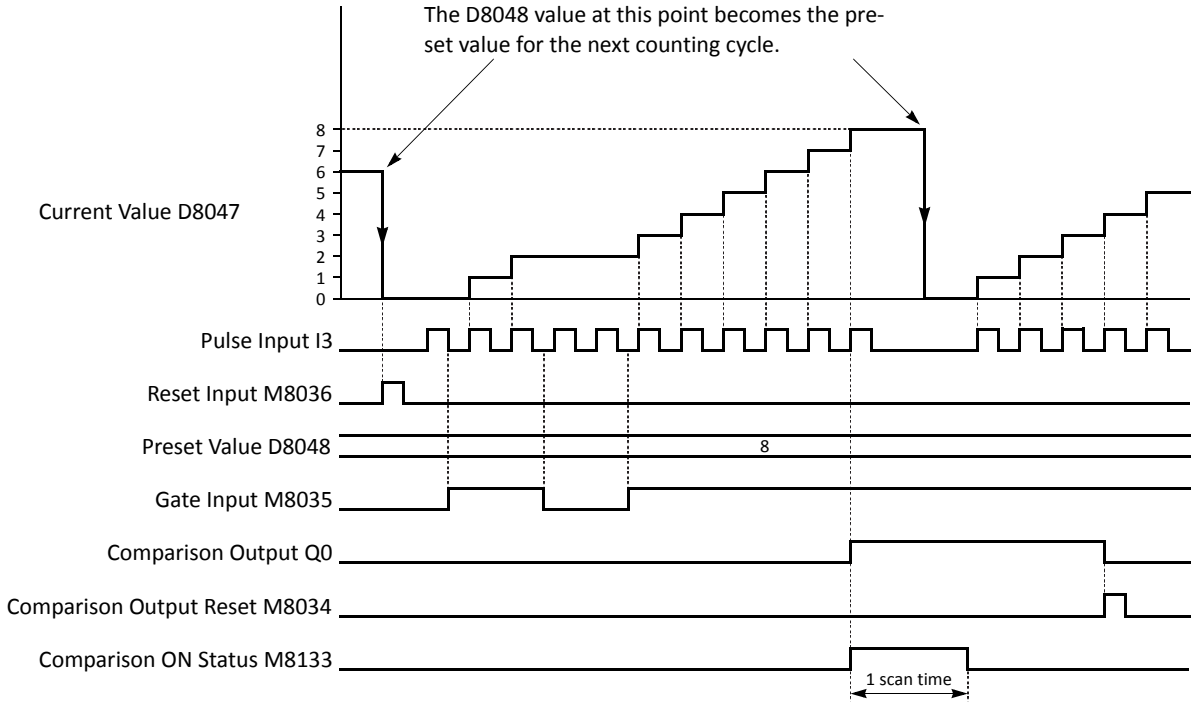
Single-phase High-speed Counter Functions (All-in-One Type CPU Modules)

Counting Mode	Adding counter
Maximum Counting Frequency	HSC1: 50 kHz HSC2 through HSC4: 5 kHz
Counting Range	0 to 65535 (16 bits)
Gate Control	Enable/disable counting
Current Value Reset	Current value is reset to 0 when the current value reaches the preset value or when reset input I2 (HSC1 only) or a reset input special internal relay is turned on.
Status Relays	Special internal relays for indicating high-speed counter statuses.
Comparison Output	Any output number available on the CPU module can be designated as a comparison output which turns on when the current value reaches the preset value. Output numbers on expansion output or mixed I/O modules cannot be designated as a comparison output.

Single-phase High-speed Counter Timing Chart

Example: Single--phase high-speed counter HSC2

Preset value is 8. Q0 is designated as a comparison output.



- When reset input M8036 is turned on, the D8047 current value is cleared to 0, then the D8048 preset value takes effect for the next counting cycle.
- While gate input M8035 is on, single-phase high-speed counter HSC2 counts pulse inputs to input I3.
- The D8047 current value is updated every scan.
- When the D8047 current value reaches the D8048 preset value, comparison ON status M8133 goes on for one scan. At the same time, comparison output Q0 turns on and remains on until comparison output reset M8034 is turned on.
- When the D8047 current value reaches the D8048 preset value, the D8048 preset value at that point takes effect for the next counting cycle.

Two-phase High-speed Counter HSC1 (All-in-One Type CPU Modules)

Two-phase high-speed counter HSC1 operates in the rotary encoder mode, and counts up or down input pulses to input terminals I0 (phase A) and I1 (phase B). When the current value overflows 65535 or underflows 0, a designated comparison output turns on. Any output terminal available on the CPU module can be designated as a comparison output. When input I2 (reset input) is turned on, the current value is reset to a predetermined reset value, and the two-phase high-speed counter counts subsequent input pulses starting at the reset value.

Six special internal relays and two special data registers are assigned to control and monitor the two-phase high-speed counter operation. The current value is stored in data register D8045 (current value) and is updated every scan. The value stored in D8046 (reset value) is used as a reset value. When a high-speed counter reset input (I2 or M8032) is turned on, the current value in D8045 is reset to the value stored in D8046.

The two-phase high-speed counter is enabled while gate input special internal relay M8031 is on and is disabled while M8031 is off. When current value overflow or underflow occurs while counting up or down, special internal relay M8131 or M8132 turns on in the next scan, respectively. At this point, the D8045 current value is reset to the D8046 reset value for the subsequent counting cycle. When comparison output reset special internal relay M8030 is turned on, the designated comparison output is turned off. When reset input I2 is turned on to reset the current value, reset status special internal relay M8130 turns on in the next scan. When reset input special internal relay M8032 is turned on, M8130 does not turn on. See page 5-11.

Special Internal Relays for Two-phase High-speed Counter (All-in-One Type CPU Modules)

Description	High-speed Counter No.				ON	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Comparison Output Reset	M8030	—	—	—	Turns off comparison output	R/W
Gate Input	M8031	—	—	—	Enables counting	R/W
Reset Input	M8032	—	—	—	Resets the current value	R/W
Reset Status	M8130	—	—	—	Current value reset by I2	Read only
Current Value Overflow	M8131	—	—	—	Overflow occurred	Read only
Current Value Underflow	M8132	—	—	—	Underflow occurred	Read only

Note: Special internal relays M8130 through M8132 go on for only one scan.

Special Data Registers for Two-phase High-speed Counter (All-in-One Type CPU Modules)

Description	High-speed Counter No.				Updated	Read/Write
	HSC1	HSC2	HSC3	HSC4		
High-speed Counter Current Value	D8045	—	—	—	Every scan	Read only
High-speed Counter Reset Value	D8046	—	—	—	—	R/W

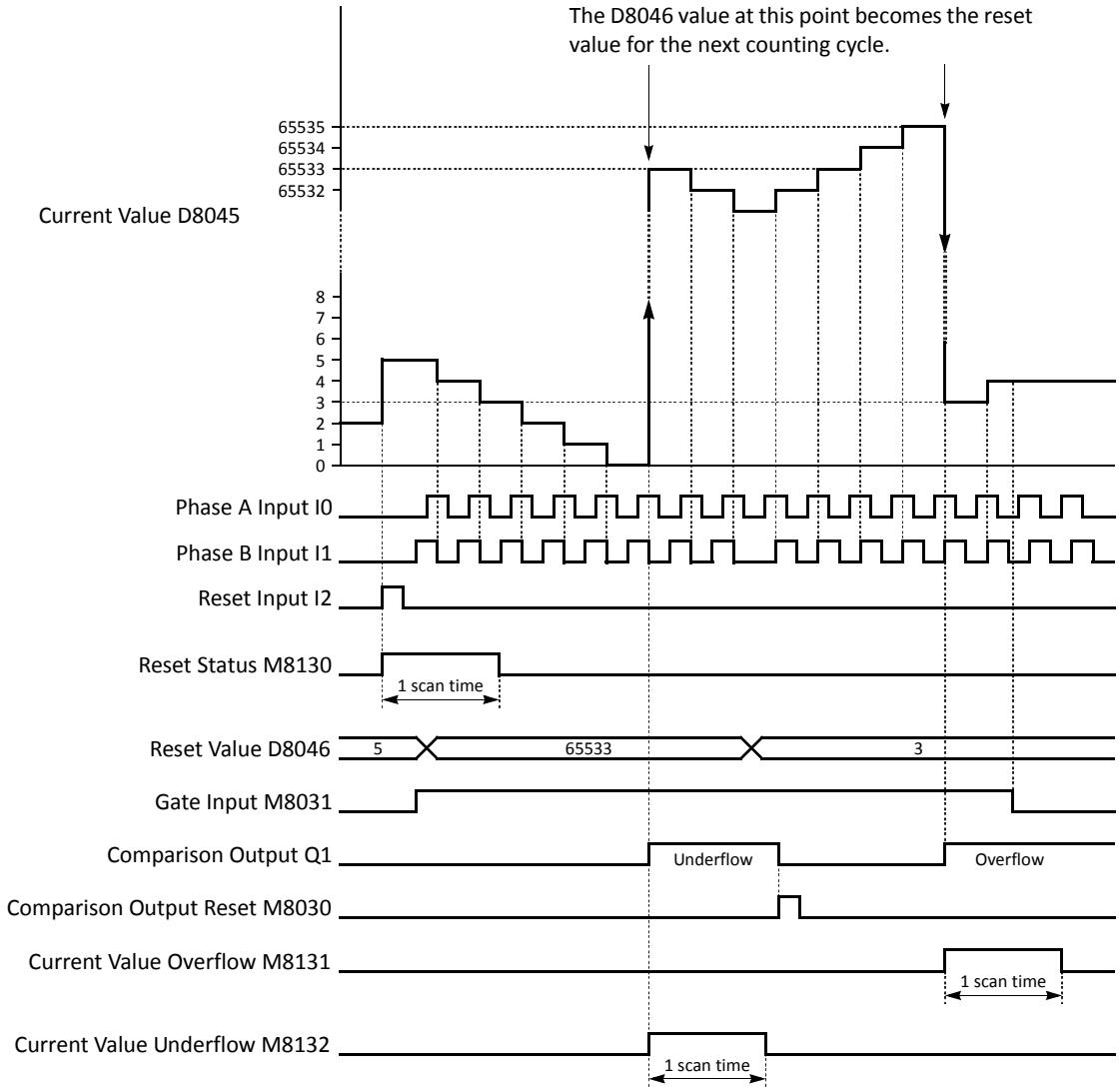
Two-phase High-speed Counter Functions (All-in-One Type CPU Modules)

Counting Mode	1-edge count (phases A, B, Z)
Maximum Counting Frequency	50 kHz
Counting Range	0 to 65535 (16 bits)
Gate Control	Enable/disable counting
Current Value Reset	Current value is reset to a given value when the current value overflows 65535 or underflows 0, or when reset input I2 or reset input special internal relay M8032 is turned on.
Control/Status Relays	Special internal relays are provided to control and monitor the high-speed counter operation.
Comparison Output	Any output number available on the CPU module can be designated as a comparison output which turns on when current value overflow or underflow occurs. Output numbers on expansion output or mixed I/O modules cannot be designated as a comparison output.

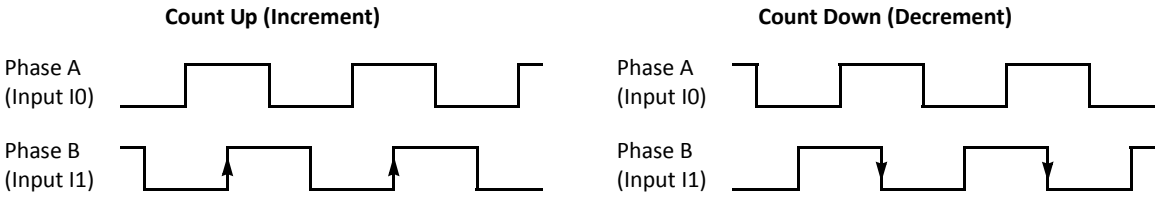
Two-phase High-speed Counter Timing Chart

Example: Two--phase high-speed counter HSC1

Reset input I2 is used. Q1 is designated as a comparison output.



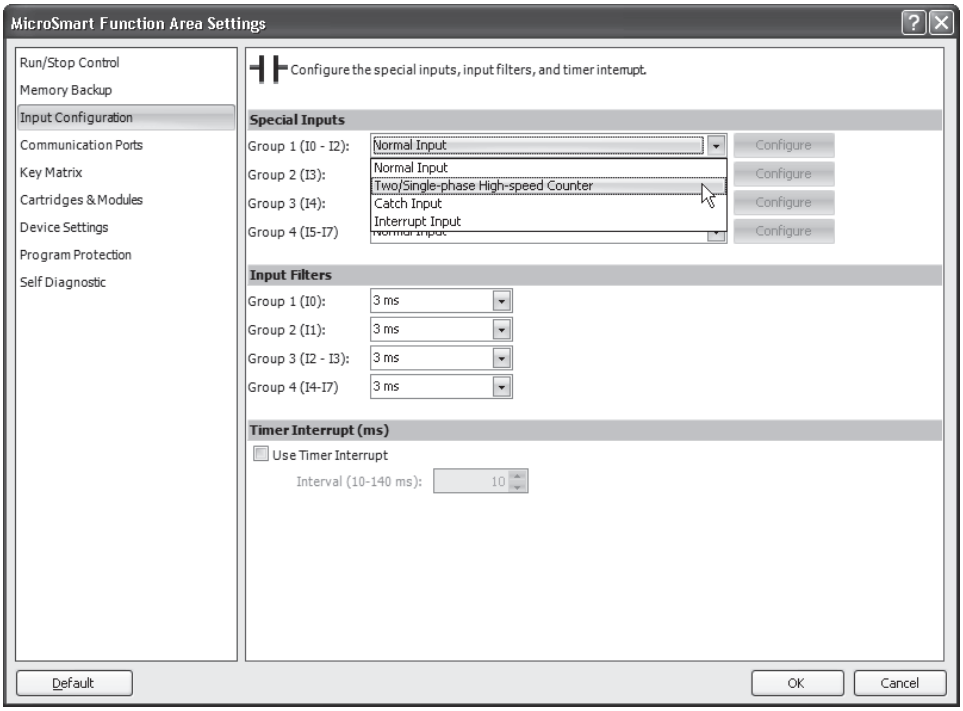
- When reset input I2 is turned on, the D8046 reset value is set to the D8045 current value, then reset status M8130 turns on for one scan. If reset input M8032 is turned on, reset status M8130 does not turn on.
- While gate input M8031 is on, the two-phase high-speed counter counts up or down depending on the phase difference between phase A (input I0) and phase B (input I1).



Programming WindLDR (All-in-One Type CPU Modules)

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

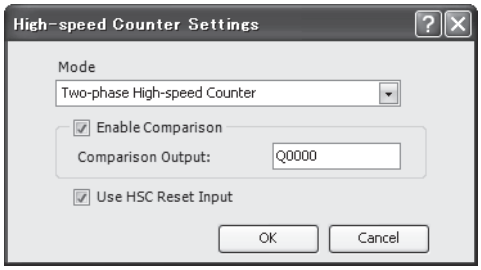
The Function Area Settings dialog box for Input Configuration appears.



2. When using high-speed counter HSC1, select **Two/Single-phase High-speed Counter** in the Group 1 pull-down list box.

When using high-speed counters HSC2 through HSC4, select **Single-phase High-speed Counter** in the Groups 2 through 4 pull-down list boxes.

The High-speed Counter Settings dialog box appears.



Mode

Select **Two-phase High-speed Counter** or **Single-phase High-speed Counter** for HSC1. Only Single-phase High-speed Counter is available for HSC2 through HSC4.

CPU Module	Comparison Output
FC5A-C10R2/C/D	Q0 to Q3
FC5A-C16R2/C/D	Q0 to Q6
FC5A-C24R2/C/D	Q0 to Q7, Q10 to Q11

Enable Comparison

Click the check box to enable the high-speed counter comparison output, and specify an output number available on the CPU module in the **Comparison Output** field. When the preset value is reached (single-phase high-speed counter) or when current value overflow or underflow occurs (two-phase high-speed counter), the specified comparison output is turned on and remains on until a comparison output reset special internal relay (M8030, M8034, M8040, or M8044) is turned on.

Use HSC Reset Input

Click the check box to enable high-speed counter reset input I2 for HSC1 only. When input I2 is turned on, the current value in D8045 is reset depending on the high-speed counter mode.

Single-phase	The current value is reset to 0. The value stored in D8046 (high-speed counter preset value) at this point takes effect for the subsequent counting cycle.
Two-phase	The current value is reset to the value stored in D8046 (high-speed counter reset value). The two-phase high-speed counter counts subsequent input pulses starting at the reset value.

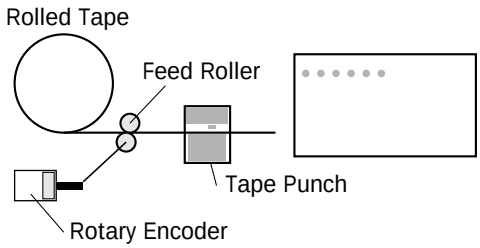
Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Example: Two-phase High-speed Counter on All-in-One Type CPU Module

This example demonstrates a program for two-phase high-speed counter HSC1 to punch holes in a paper tape at regular intervals.

Description of Operation

A rotary encoder is linked to the tape feed roller directly, and the output pulses from the rotary encoder are counted by the two-phase high-speed counter in the MicroSmart CPU module. When the high-speed counter counts 2,700 pulses, the comparison output is turned on. When the comparison output is turned on, the high-speed counter continues another cycle of counting. The comparison output remains on for 0.5 second to punch holes in the tape, and is turned off before the high-speed counter counts 2,700 pulses again.

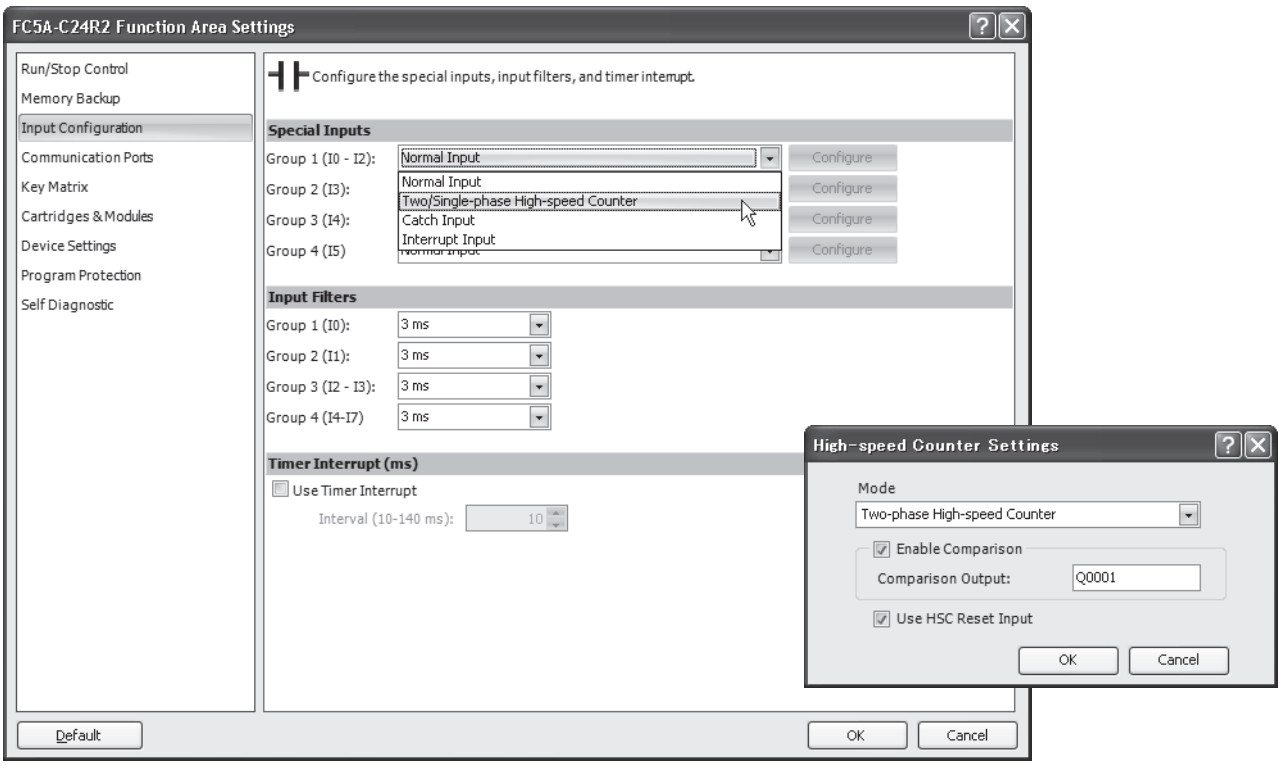


Program Parameters

PLC Selection	FC5A-C24R2
Group 1 (I0 - I2)	Two/Single-phase High-speed Counter
High-speed Counter Settings	Two-phase High-speed Counter
Enable Comparison	Yes
Comparison Output	Q1
Use HSC Reset Input (I2)	No
HSC Reset Value (D8046)	To cause current value overflow every 2700 pulses, store 62836 to D8046 (65535 – 2700 + 1 = 62836)
Timer Preset Value	0.5 sec (needed for punching) programmed in TIM instruction

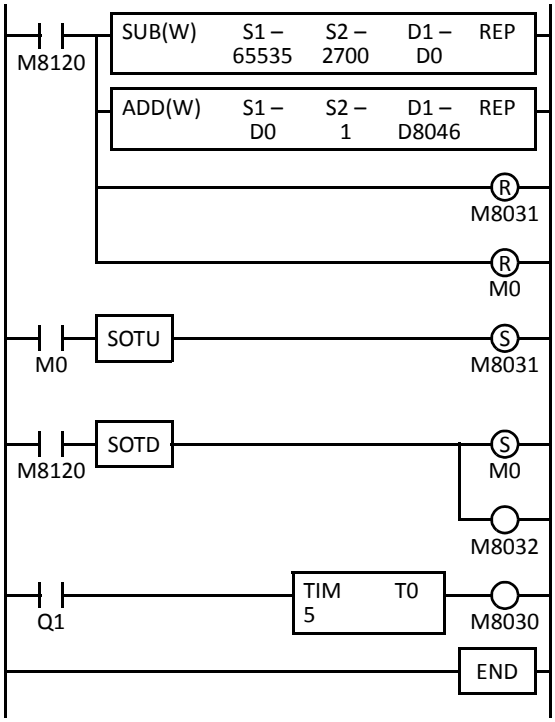
Note: This example does not use the phase Z signal (input I2).

Programming WindLDR



Ladder Diagram

When the MicroSmart starts operation, reset value 62836 is stored to reset value special data register D8046. Gate input special internal relay M8031 is turned on at the end of the third scan to start the high-speed counter to count input pulses.



M8120 is the initialize pulse special internal relay.

1st scan

SUB and ADD instructions are used to store a reset value of 62836 (65535 – 2700 + 1) to D8046 (reset value).

M8031 (gate input) is turned off.

M0 is turned off.

3rd scan

At the rising edge of M0, M8031 (gate input) is turned on. After the END processing of the third scan, HSC1 starts counting.

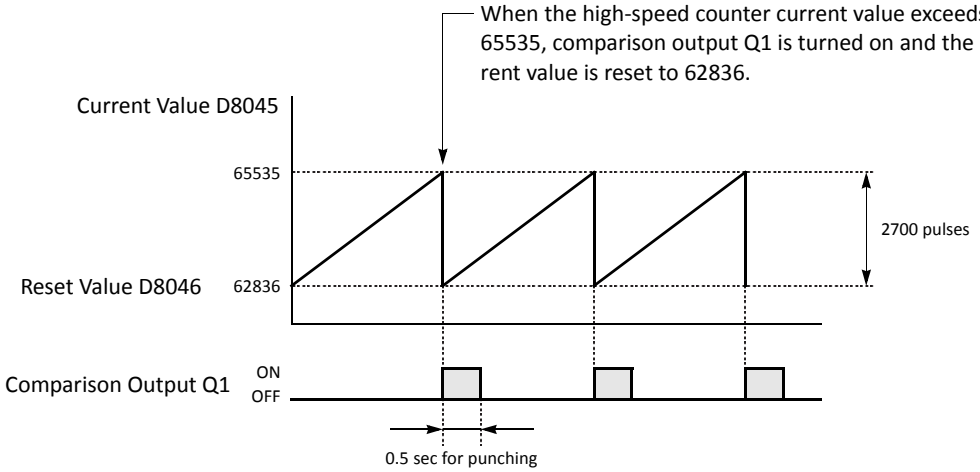
2nd scan

At the falling edge of M8120 (initialize pulse), M0 is turned on. M8032 (reset input) is turned on to initialize HSC1 in the END processing of the second scan.

When HSC1 overflows 65535, output Q1 (comparison output) is turned on to start timer T0. HSC1 starts to repeat counting.

When the timer times out 0.5 sec, M8030 (comparison output reset) is turned on to turn off output Q1.

Timing Chart



High-speed Counters on Slim Type CPU Modules

Slim type CPU modules have four 32-bit high-speed counters, HSC1 through HSC4, which can count up to 4,294,967,295 pulses. HSC1 and HSC4 can be used as a single-phase or two-phase high-speed counter. HSC2 and HSC3 are single-phase high-speed counters. All high-speed counter functions are selected using the Function Area Settings in WindLDR.

High-speed Counter Operation Modes and Input Terminals (Slim Type CPU Modules)

HSC No.	HSC1			HSC2	HSC3	HSC4		
Input Terminal (Note 1)	I0	I1	I2	I3	I4	I5	I6	I7
Single-phase High-speed Counter								
Adding Counter	(Note 2)	Pulse Input	Reset Input (Note 3)	Pulse Input	Pulse Input	Reset Input (Note 3)	(Note 2)	Pulse Input
Dual-pulse Reversible Counter	Down Pulse	Up Pulse	Reset Input (Note 3)	—	—	Reset Input (Note 3)	Down Pulse	Up Pulse
Up/down Selection Reversible Counter	U/D Selection	Pulse Input	Reset Input (Note 3)	—	—	Reset Input (Note 3)	U/D Selection	Pulse Input
Two-phase High-speed Counter								
1-edge Count 2-edge Count 4-edge Count	Phase A	Phase B	Reset Input (Phase Z) (Note 3)	—	—	Reset Input (Phase Z) (Note 3)	Phase A	Phase B

Note 1: When the voltage difference between the input terminal and the COM terminal is 24V DC, the input turns on. Both positive and negative input voltages are accepted.
Note 2: In the single-phase high-speed counter, inputs I0 and I6 are used for dual-pulse reversible counters and up/down selection reversible counters. When adding counter is selected, inputs I0 and I6 can be used as ordinary input terminals.
Note 3: When a reset input is not used, inputs I2 and I5 can be used as an ordinary input terminal.

Single-phase High-speed Counters HSC1 through HSC4 (Slim Type CPU Modules)

Single-phase counters include three modes; adding counter, dual-pulse reversible counter, and up/down selection reversible counter. All high-speed counters HSC1 through HSC4 can be used as adding counters. HSC1 and HSC4 can also be used as a dual-pulse reversible counter and an up/down selection reversible counter.

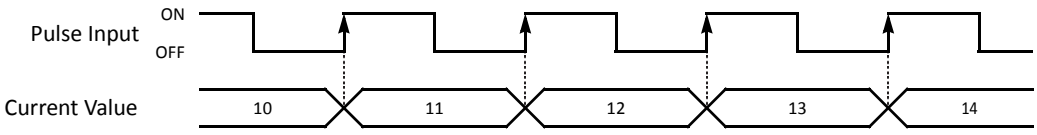
Adding Counter

The four adding counters count input pulses to the input terminal allocated to each high-speed counter.

HSC1 and HSC4 can designate two preset values: preset value 1 and preset value 2. When the current value reaches preset value 1, a designated comparison output turns on or program execution jumps to a designated tag. At this point, the current value can be designated to keep counting subsequent input pulses or to be reset to the reset value and restart another counting cycle. When “Keep Current Value” is designated, the current value continues to increase up to preset value 2, then another comparison output can be turned on or program execution jumps to a designated tag. Similarly, when “Keep Current Value” is designated for preset value 2, the current value continues to increase up to 4,294,967,295. At this point, another comparison output can be turned on or program execution jumps to a designated tag, and the current value is reset to the reset value.

HSC2 and HSC3 can designate one preset value. When the preset value is reached, a designated comparison output turns on or program execution jumps to a designated tag, and the current value is reset to 0 to start another counting cycle.

- **Single-phase Adding Counter Operation Chart**



When the pulse input turns on, the current value increments.

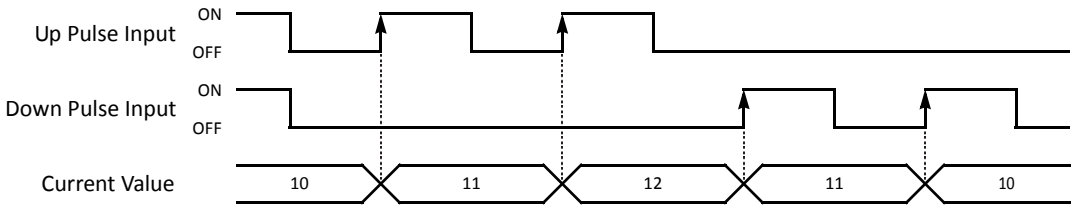
Dual-pulse Reversible Counter

HSC1 and HSC4 can also be used as dual-pulse reversible counters to increment or decrement the current value when receiving input pulses to the up pulse input terminal or the down pulse input terminal, respectively.

Current value comparison and comparison actions are similar to the HSC1 and HSC4 adding counters. In addition, the dual pulse reversible counters have another comparison of the current value to 0. When the current value decreases down to 0, another comparison output can be turned on or program execution jumps to a designated tag, and the current value is reset to the reset value.

When the current value decrements and reaches preset value 1 or 2, the comparison action occurs similarly, turning on the comparison output or jumping to a designated tag.

- **Single-phase Dual-pulse Reversible Counter Operation Chart**



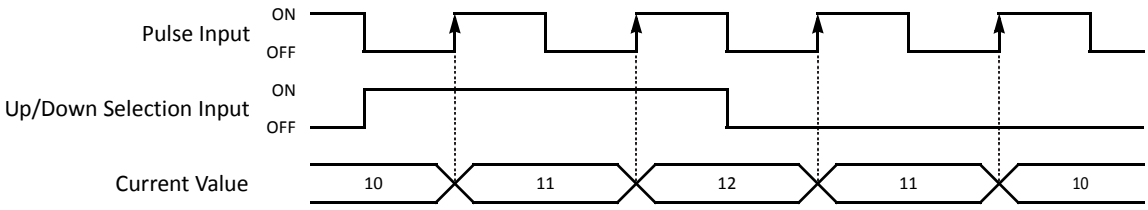
When the up pulse input turns on, the current value increments.
When the down pulse input turns on, the current value decrements.

Up/down Selection Reversible Counter

HSC1 and HSC4 can also be used as up/down selection reversible counters to increment or decrement the current value when receiving input pulses to the pulse input terminal depending on the up/down selection input status.

Current value comparison and comparison actions are the same as the HSC1 and HSC4 dual-pulse reversible counters.

- **Single-phase Up/down Selection Reversible Counter Operation Chart**



When the pulse input turns on while the up/down selection input is on, the current value increments.
When the pulse input turns on while the up/down selection input is off, the current value decrements.

Eight special internal relays and eight special data registers are assigned to control and monitor each single-phase high-speed counter operation. The current value is stored in two special data registers (current value) and is updated every scan. The value stored in another two special data registers (preset value) is used as a preset value. When a reset input special internal relay is turned on, the current value is reset to the reset value (HSC1 and HSC4) or 0 (HSC2 and HSC3). HSC1 and HSC4 can set two preset values.

The single-phase high-speed counter is enabled while a gate input special internal relay is on and is disabled while the gate input is off. When the current value reaches the preset value, a special internal relay (comparison ON status) turns on in the next scan. At this point, the current value is reset to the reset value (HSC1 and HSC4) or 0 (HSC2 and HSC3), and the value stored in preset value special data registers takes effect for the subsequent counting cycle. If HSC1 or HSC4 is set to keep the current value when the current value reaches the first preset value, HSC1 or HSC4 continues counting until the current value reaches the second preset value. When a comparison output reset special internal relay is turned on, the designated comparison output is turned off.

In addition, only the single-phase high-speed counter HSC1 or HSC4 has reset input I2 or I5 and reset status special internal relay M8130 or M8135. When reset input I2 or I5 is turned on to reset the current value, reset status special internal relay M8130 or M8135 turns on in the next scan. When reset input special internal relay M8032 or M8046 is turned on, M8130 or M8135 does not turn on. See page 5-18.

Special Internal Relays for Single-phase High-speed Counters (Slim Type CPU Modules)

Description	High-speed Counter No.				ON	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Comparison Output Reset	M8030	M8034	M8040	M8044	Turns off comparison output	R/W
Gate Input	M8031	M8035	M8041	M8045	Enables counting	R/W
Reset Input	M8032	M8036	M8042	M8046	Resets the current value	R/W
Reset Status	M8130	—	—	M8135	Current value reset by I2 or I5	Read only
Comparison 1 ON Status	M8131	M8133	M8134	M8136	Preset value 1 reached	Read only
Comparison 2 ON Status	M8132	—	—	M8137	Preset value 2 reached	Read only
Current Value Overflow	M8161	—	—	M8163	Overflow occurred	Read only
Current Value Underflow	M8162	—	—	M8164	Underflow occurred	Read only

Note: Special internal relays M8130 through M8137 and M8161 through M8164 go on for only one scan.

Special Data Registers for Single-phase High-speed Counters (Slim Type CPU Modules)

Description	High-speed Counter No.				Updated	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Current Value (High Word)	D8210	D8218	D8222	D8226	Every scan	Read only
Current Value (Low Word)	D8211	D8219	D8223	D8227	Every scan	Read only
Preset Value 1 (High Word)	D8212	D8220	D8224	D8228	—	R/W
Preset Value 1 (Low Word)	D8213	D8221	D8225	D8229	—	R/W
Preset Value 2 (High Word)	D8214	—	—	D8230	—	R/W
Preset Value 2 (Low Word)	D8215	—	—	D8231	—	R/W
Reset Value (High Word)	D8216	—	—	D8232	—	R/W
Reset Value (Low Word)	D8217	—	—	D8233	—	R/W

Note: When using the current value, preset value 1, preset value 2, and reset value in advanced instructions, select the data type of double word (D).

Single-phase High-speed Counter Functions (Slim Type CPU Modules)

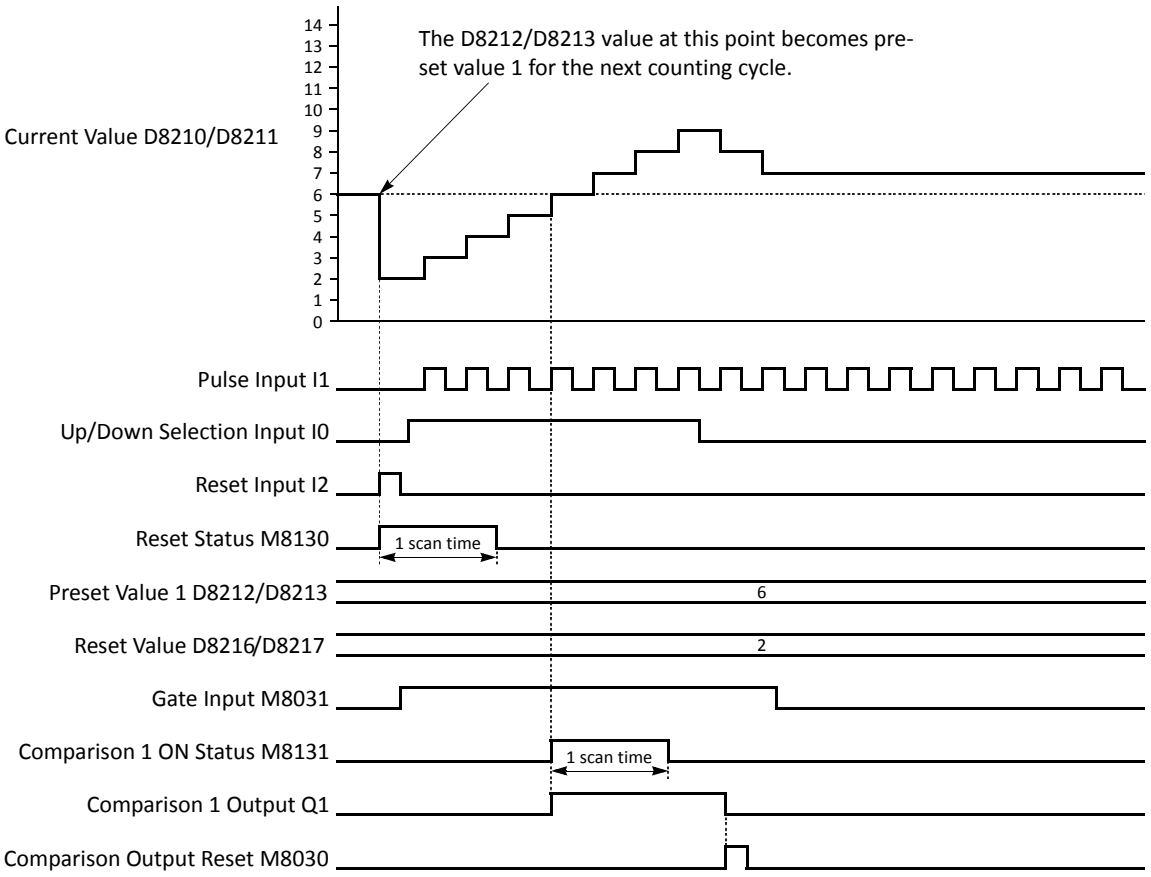
Counting Mode	HSC1 to HSC4	Adding counter
	HSC1 HSC4	Dual-pulse reversible counter Up/down selection reversible counter
Maximum Counting Frequency		100 kHz
Counting Range		0 to 4,294,967,295 (32 bits)
Gate Control		Enable/disable counting
Current Value Reset	HSC1 HSC4	Current value is reset to the reset value when reset input I2 (HSC1) or I5 (HSC4) is turned on or when a reset input special internal relay M8032 (HSC1) or M8046 (HSC4) is turned on. In addition, when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true, the current value can be reset to the reset value. The current value comparison is designated in the Function Area Settings.
	HSC2 HSC3	Current value is reset to 0 when a reset input special internal relay M8036 (HSC2) or M8042 (HSC3) is turned on. In addition, when the current value reaches the preset value, the current value is reset to 0.
Current Value Keep	HSC1 HSC4	When current value comparison for preset value 1 or preset value 2 is true, the current value can also be kept to count subsequent input pulses, without resetting the current value to the reset value.
Status Relays		Special internal relays for indicating high-speed counter statuses.

Comparison Action	Comparison Output	A comparison output turns on when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true. Any output number available on the CPU module can be designated as a comparison output. Output numbers on expansion output or mixed I/O modules cannot be designated as a comparison output.
	Interrupt Program	Program execution jumps to a tag when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true.

Single-phase High-speed Counter Timing Chart

Example: Single--phase high-speed counter HSC1

Operation mode: Up/down selection reversible counter
Preset value 1 is 6.
Q1 is designated as the comparison 1 output.
The current value is maintained when preset value 1 is reached.



- When reset input I2 is turned on, the D8210/D8211 current value is reset to the D8216/D8217 reset value, then the D8212/D8213 preset value 1 takes effect for the next counting cycle.
- While gate input M8031 is on, up/down selection reversible counter HSC1 counts pulse inputs to input I1. While up/down selection input I0 is on, the current value increments. While up/down selection input I0 is off, the current value decrements.
- The current value is updated every scan.
- When the current value reaches the preset value, comparison 1 ON status M8131 goes on for one scan. At the same time, comparison 1 output Q1 turns on and remains on until comparison output reset M8030 is turned on.
- After the current value has reached the preset value, the current value is maintained and the high-speed couner continues to count input pulses as long as the gate input is on.

Two-phase High-speed Counters HSC1 and HSC4 (Slim Type CPU Modules)

Two-phase high-speed counters HSC1 and HSC4 operates in the rotary encoder mode, and counts up or down input pulses to input terminals I0 or I6 (phase A) and I1 or I7 (phase B), respectively.

HSC1 and HSC4 can designate two preset values: preset value 1 and preset value 2. When the current value reaches preset value 1, a designated comparison output turns on or program execution jumps to a designated tag. At this point, the current value can be designated to keep counting subsequent input pulses or to be reset to the reset value and restart another counting cycle. When “Keep Current Value” is designated, the current value continues to increase up to preset value 2, then another comparison output can be turned on or program execution jumps to a designated tag. Similarly, when “Keep Current Value” is designated for preset value 2, the current value continues to increase up to 4,294,967,295. At this point, another comparison output can be turned on or program execution jumps to a designated tag, and the current value is reset to the reset value.

In addition, the two-phase high-speed counters have another comparison of the current value to 0. When the current value decreases down to 0, another comparison output can be turned on or program execution jumps to a designated tag, and the current value is reset to the reset value.

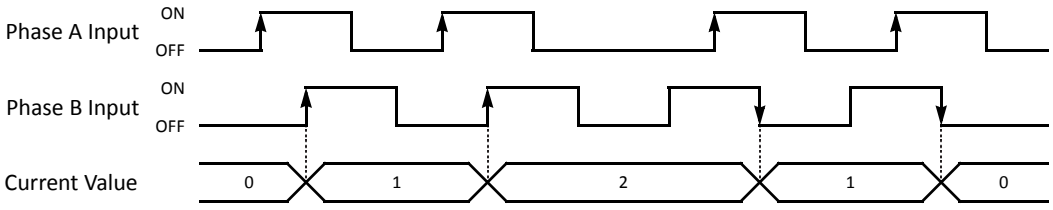
When the current value decrements and reaches preset value 1 or 2, the comparison action occurs similarly, turning on the comparison output or jumping to a designated tag.

The two-phase high-speed counters have three counting modes: 1-edge count, 2-edge count, and 4-edge count.

1-edge Count

The current value increments or decrements at the rising or falling edge of the phase B input after the phase A input has turned on.

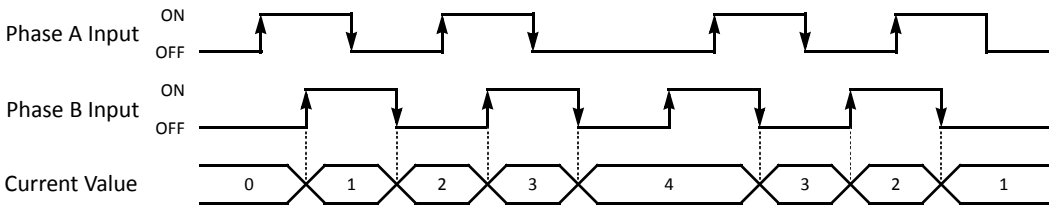
- **1-edge Count Operation Chart**



2-edge Count

The current value increments or decrements at the rising or falling edge of the phase B input after the phase A input has turned on or off.

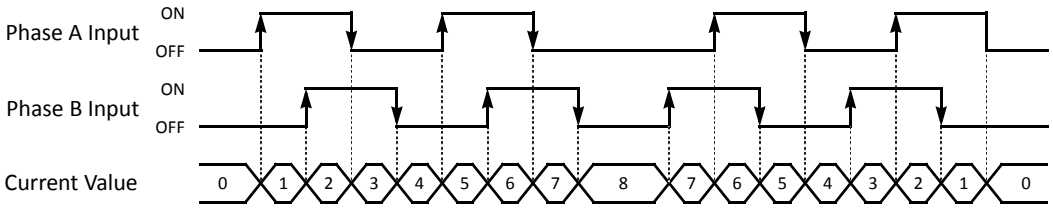
- **2-edge Count Operation Chart**



4-edge Count

The current value increments or decrements at the rising or falling edges of the phase A and B inputs.

- **4-edge Count Operation Chart**



Eight special internal relays and eight special data registers are assigned to control and monitor each two-phase high-speed counter operation. The current value is stored in two special data registers (current value) and is updated every scan. The value stored in another two special data registers (preset value) is used as a preset value. When a reset input special internal relay is turned on, the current value is reset to the reset value. HSC1 and HSC4 can set two preset values.

The two-phase high-speed counter is enabled while a gate input special internal relay is on and is disabled while the gate input is off. When the current value reaches the preset value, a special internal relay (comparison ON status) turns on in the next scan. At this point, the current value is reset to the reset value, and the value stored in preset value special data registers takes effect for the subsequent counting cycle. If HSC1 or HSC4 is set to keep the current value when the current value reaches the first preset value, HSC1 or HSC4 continues counting until the current value reaches the second preset value. When a comparison output reset special internal relay is turned on, the designated comparison output is turned off.

In addition, HSC1 or HSC4 has reset input I2 or I5 and reset status special internal relay M8130 or M8135. When reset input I2 or I5 is turned on to reset the current value, reset status special internal relay M8130 or M8135 turns on in the next scan. When reset input special internal relay M8032 or M8046 is turned on, M8130 or M8135 does not turn on. See page 5-22.

Special Internal Relays for Two-phase High-speed Counters (Slim Type CPU Modules)

Description	High-speed Counter No.				ON	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Comparison Output Reset	M8030	—	—	M8044	Turns off comparison output	R/W
Gate Input	M8031	—	—	M8045	Enables counting	R/W
Reset Input	M8032	—	—	M8046	Resets the current value	R/W
Reset Status	M8130	—	—	M8135	Current value reset by I2 or I5	Read only
Comparison 1 ON Status	M8131	—	—	M8136	Preset value 1 reached	Read only
Comparison 2 ON Status	M8132	—	—	M8137	Preset value 2 reached	Read only
Current Value Overflow	M8161	—	—	M8163	Overflow occurred	Read only
Current Value Underflow	M8162	—	—	M8164	Underflow occurred	Read only

Note: Special internal relays M8130 to M8132, M8135 to M8137, and M8161 to M8164 go on for only one scan.

Special Data Registers for Two-phase High-speed Counters (Slim Type CPU Modules)

Description	High-speed Counter No.				Updated	Read/Write
	HSC1	HSC2	HSC3	HSC4		
Current Value (High Word)	D8210	—	—	D8226	Every scan	Read only
Current Value (Low Word)	D8211	—	—	D8227	Every scan	Read only
Preset Value 1 (High Word)	D8212	—	—	D8228	—	R/W
Preset Value 1 (Low Word)	D8213	—	—	D8229	—	R/W
Preset Value 2 (High Word)	D8214	—	—	D8230	—	R/W
Preset Value 2 (Low Word)	D8215	—	—	D8231	—	R/W
Reset Value (High Word)	D8216	—	—	D8232	—	R/W
Reset Value (Low Word)	D8217	—	—	D8233	—	R/W

Note: When using the current value, preset value 1, preset value 2, and reset value in advanced instructions, select the data type of double word (D).

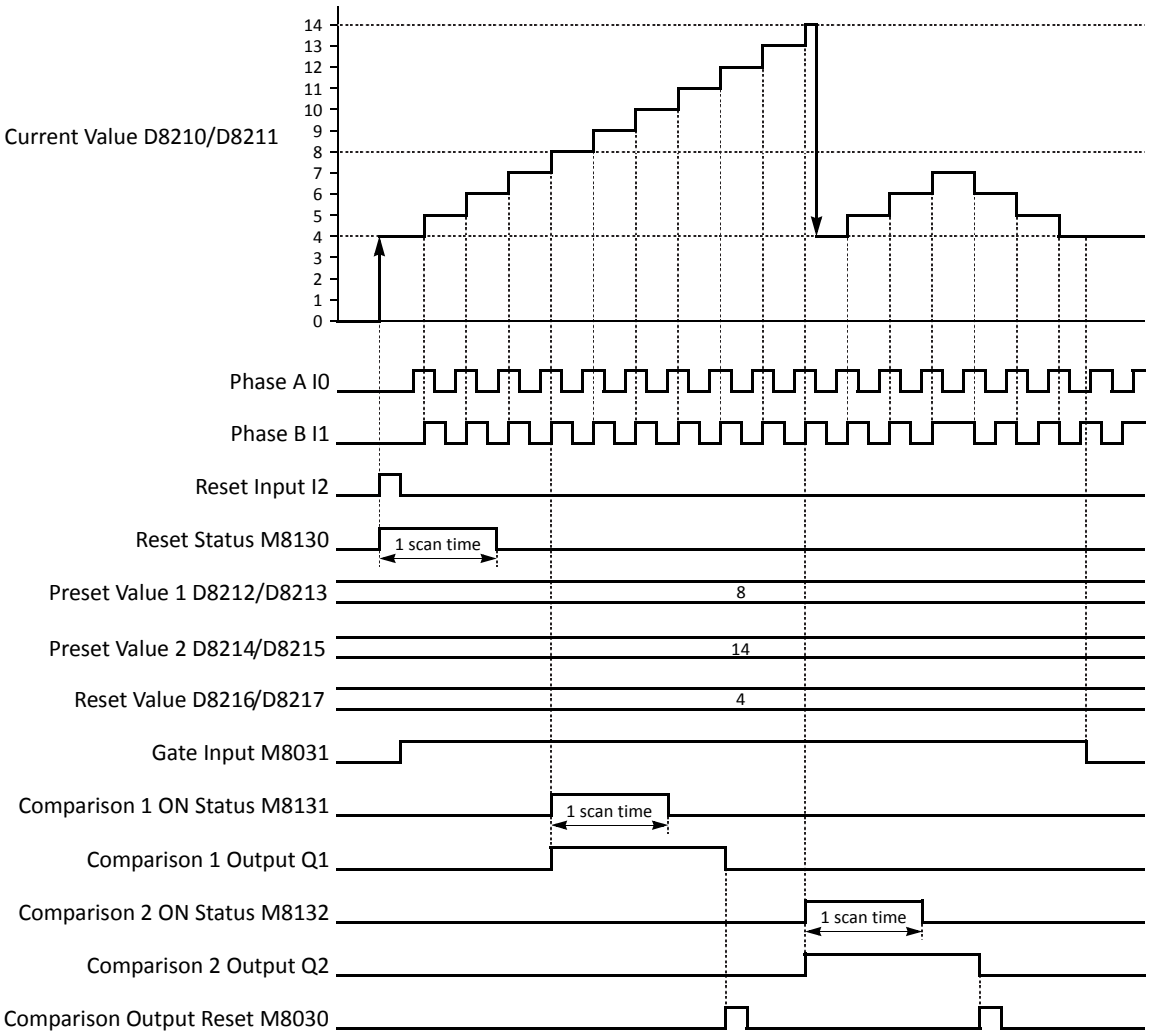
Two-phase High-speed Counter Functions (Slim Type CPU Modules)

Counting Mode and Maximum Counting Frequency		1-edge count: 100 kHz 2-edge count: 50 kHz 4-edge count: 25 kHz
Counting Range		0 to 4,294,967,295 (32 bits)
Gate Control		Enable/disable counting
Current Value Reset		Current value is reset to the reset value when reset input I2 (HSC1) or I5 (HSC4) is turned on or when a reset input special internal relay M8032 (HSC1) or M8046 (HSC4) is turned on. In addition, when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true, the current value can be reset to the reset value. The current value comparison is designated in the Function Area Settings.
Current Value Keep		When current value comparison for preset value 1 or preset value 2 is true, the current value can also be kept to count subsequent input pulses, without resetting the current value to the reset value.
Status Relays		Special internal relays for indicating high-speed counter statuses.
Comparison Action	Comparison Output	A comparison output turns on when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true. Any output number available on the CPU module can be designated as a comparison output. Output numbers on expansion output or mixed I/O modules cannot be designated as a comparison output.
	Interrupt Program	Program execution jumps to a tag when any of current value comparison (preset value 1, preset value 2, overflow, or underflow) is true.

Two-phase High-speed Counter Timing Chart

Example: Two--phase high-speed counter HSC1

1-edge count, preset value 1 is 8.
I2 is designated as the reset input.
Q1 is designated as the comparison 1 output.
The current value is maintained when preset value 1 is reached.
Q2 is designated as the comparison 2 output.
The current value is not maintained when preset value 2 is reached.
Overflow and underflow actions are not used.



- When reset input I2 is turned on, the D8210/D8211 current value is reset to the D8216/D8217 reset value, then the D8212/D8213 preset value 1 and D8214/D8215 preset value 2 take effect for the next counting cycle.
- While gate input M8031 is on, two-phase HSC1 counts pulse inputs to phase B input I1 because of the 1-edge count mode. While phase A input I0 is leading phase B input I1, the current value increments. While phase A input I0 is trailing phase B input I1, the current value decrements.
- The current value is updated every scan.
- When the current value reaches the preset value 1, comparison 1 ON status M8131 goes on for one scan. At the same time, comparison 1 output Q1 turns on and remains on until comparison output reset M8030 is turned on. The current value is maintained and the high-speed couner continues to count input pulses.
- When the current value reaches the preset value 2, comparison 2 ON status M8132 goes on for one scan. At the same time, comparison 2 output Q2 turns on and remains on until comparison output reset M8030 is turned on. The current value is reset to the reset value and the high-speed couner continues to count input pulses.

Clearing High-speed Counter Current Value

The high-speed counter current value is reset to the reset value (two-phase high-speed counter) or to zero (single-phase high-speed counters) in five ways:

- when the CPU is powered up,
- when a user program is downloaded to the CPU,
- when reset input I2 (HSC1) or I5 (HSC4 on slim type CPU only) is turned on,
- when current value overflow or underflow occurs (two-phase) or when the preset value is reached (single-phase when Keep Current Value is not selected), or
- when the reset input (*not* the high-speed counter reset input) designated in the Function Area Settings is turned on.

Precautions for Downloading High-speed Counter Program

When downloading a user program containing a high-speed counter, turn off the gate input before downloading the user program.

If a user program containing a high-speed counter is downloaded while the gate input is on, the high-speed counter is disabled. Then, to enable counting, stop and restart the MicroSmart. Or, turn off the gate input, and 3 scans later turn on the gate input again. For ladder programs to delay the gate input 3 scans, see pages 5-27 and 5-29.

Preset Values 1 and 2

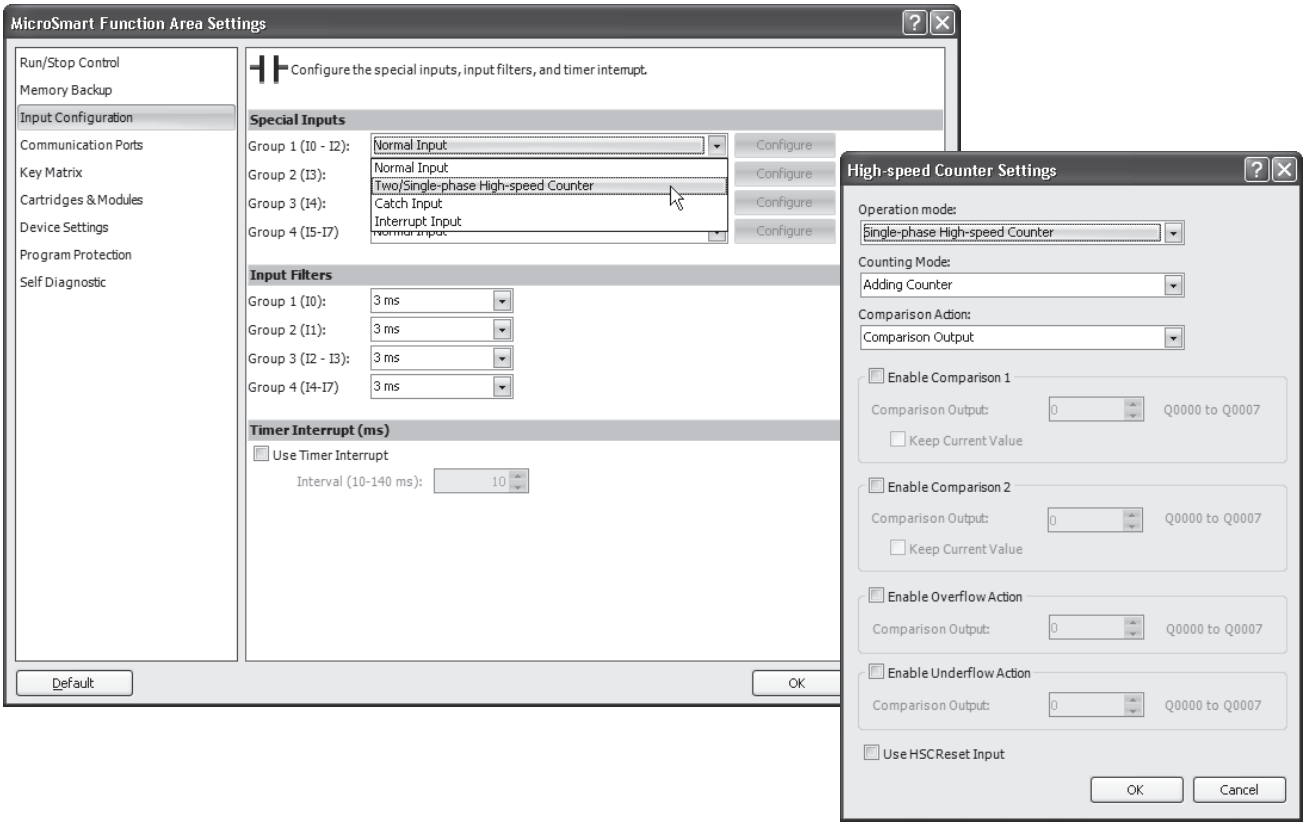
Preset values 1 and 2 take effect in the END processing at the end of the second scan after starting the CPU module. Use initialize pulse special internal relay M8120 to store preset values to appropriate data registers.

If preset value 1 or 2 has been changed during high-speed counter operation, the new preset value takes effect when the current value reaches the previous preset value. To change preset values easily, store new preset values in an interrupt program and call the new preset values when the current value reaches the previous preset value.

Programming WindLDR (Slim Type CPU Modules)

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.



2. When using high-speed counter HSC1 or HSC4, select **Two/Single-phase High-speed Counter** in the Group 1 or 4 pull-down list box.

When using high-speed counters HSC2 or HSC3, select **Single-phase High-speed Counter** in the Group 2 or 3 pull-down list box.

The High-speed Counter Settings dialog box appears.

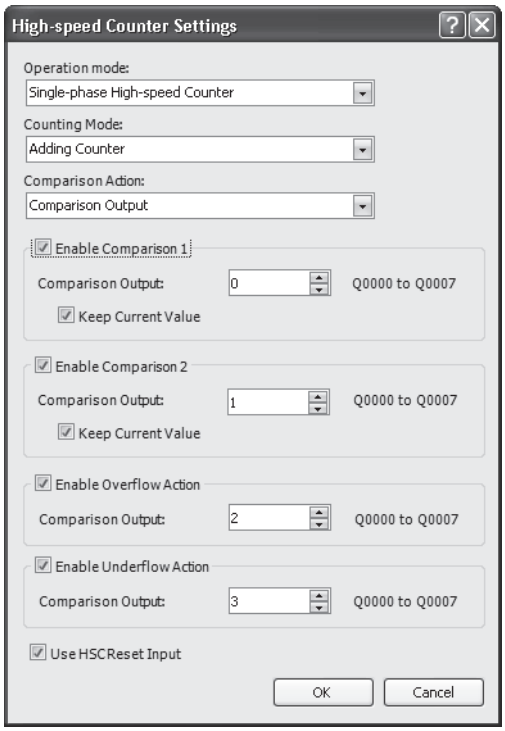
3. In the High-speed Counter Settings dialog box, select the following options.

High-speed Counter No.	**HSC1, HSC4**		**HSC2, HSC3**
Operation Mode	Single-phase	Two-phase	Single-phase
Counting Mode	Adding counter Dual-pulse reversible Up/down selection reversible	1-edge count 2-edge count 4-edge count	Adding counter
Comparison Action	Comparison output Interrupt program		Comparison output Interrupt program
Current Value Comparison	Preset value 1 Preset value 2 Overflow Underflow		Preset value

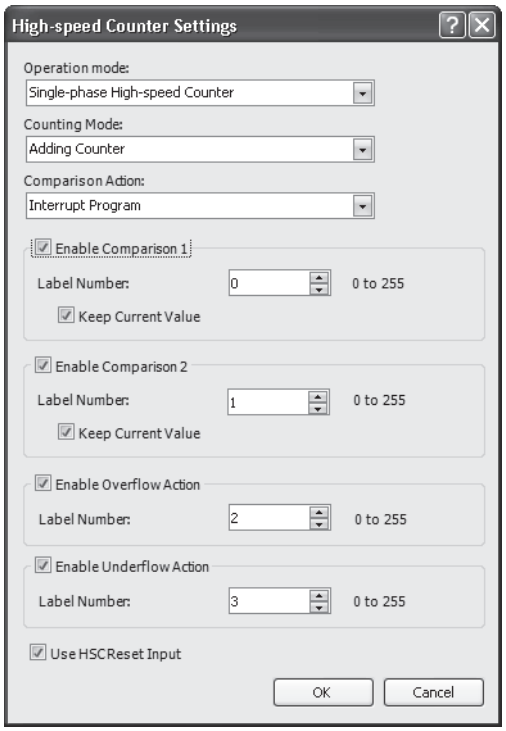
Comparison Action

For the HSC1 through HSC4, comparison action can be selected from comparison output or interrupt program. Depending on the selection in the Comparison Action field, different options for the comparison action are shown.

Comparison Action: Comparison Output



Comparison Action: Interrupt Program



4. Select comparison output number or label number for each enabled comparison.

Comparison Output

When comparison output is selected for the comparison action, specify an output number available on the CPU module in the **Comparison Output** field. When the preset value is reached (single-phase and two-phase high-speed counters) or current value overflow or underflow occurs (two-phase high-speed counter), the specified comparison output is turned on and remains on until a comparison output reset special internal relay (M8030, M8034, M8040, or M8044) is turned on.

Label Number

When interrupt program is selected for the comparison action, specify a label number to jump to. When the preset value is reached (single-phase and two-phase high-speed counters) or current value overflow or underflow occurs (two-phase high-speed counter), program execution jumps to the specified label number in the subroutine program.

5. Select to keep current value or not.

For the HSC1 and HSC4, the current value can be kept when reaching preset value 1 and preset value 2 to enable another comparison. To keep the current value, check the box. When this box is not checked, the current value in D8210/D8211 or D8226/D8227 is reset to the reset value to start another counting cycle.

6. Select to use the HSC reset input or not.

Click the check box to enable high-speed counter reset input I2 for HSC1 or I5 for HSC4 only. When input I2 or I5 is turned on, the current value is reset to the reset value to start another counting cycle.

HSC1	The current value is reset to the value stored in D8216/D8217 (high-speed counter reset value). High-speed counter HSC1 counts subsequent input pulses starting at the reset value.
HSC4	The current value is reset to the value stored in D8232/D8233 (high-speed counter reset value). High-speed counter HSC4 counts subsequent input pulses starting at the reset value.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

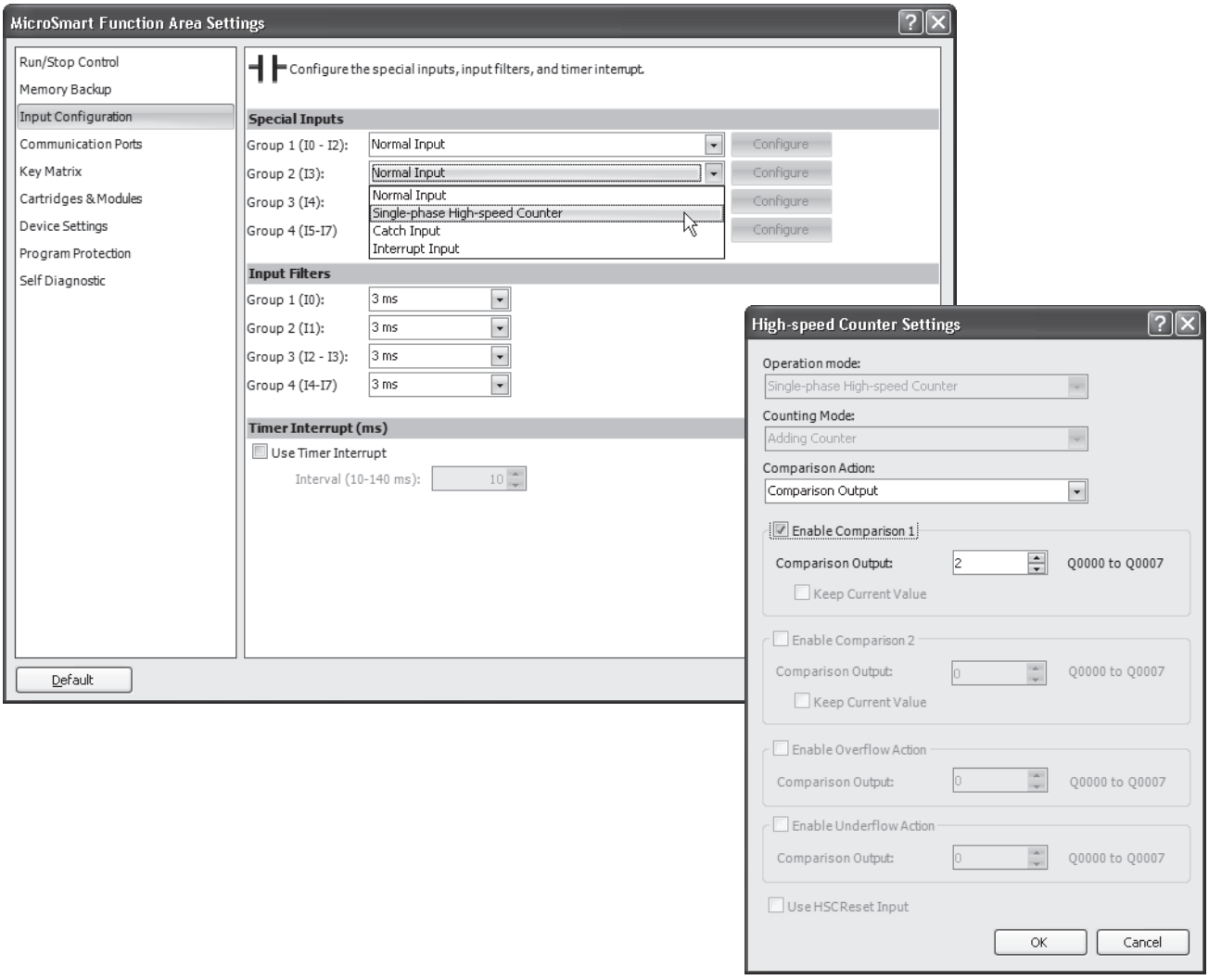
Example: Single-phase High-speed Counter (Slim Type CPU Module)

This example demonstrates a program for single-phase high-speed counter HSC2 to count input pulses and turn on output Q2 every 1000 pulses.

Program Parameters

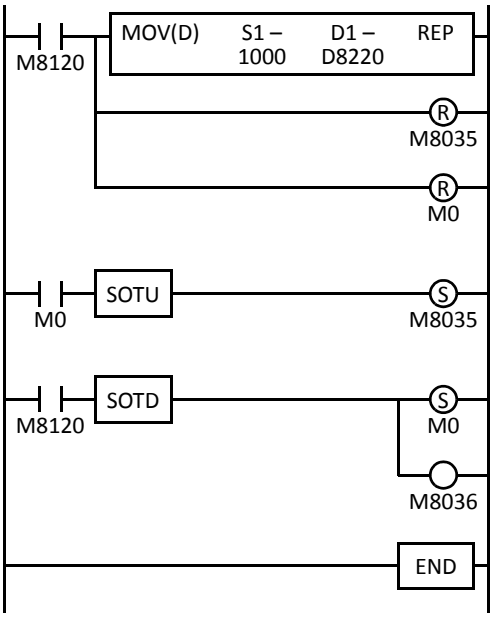
PLC Selection		FC5A-D32
Function Area Settings	Group 2 (I3)	Single-phase High-speed Counter
	Enable Comparison 1	Yes
	Comparison Output	Q2
	Enable Comparison 2	No
	Enable Overflow Action	No
	Enable Underflow Action	No
Special Data Registers	HSC Preset Value 1 High Word (D8220)	0
	HSC Preset Value 1 Low Word (D8221)	1000

Programming WindLDR



Ladder Diagram

When the MicroSmart starts operation, preset value 1000 is stored to preset value special data registers D8220 and D8221. Gate input special internal relay M8035 is turned on at the end of the third scan to start the high-speed counter to count input pulses.



M8120 is the initialize pulse special internal relay.

1st scan

MOV instruction stores a preset value of 1000 to D8220/D8221 (preset value).

M8035 (gate input) is turned off.

M0 is turned off.

3rd scan

At the rising edge of M0, M8035 (gate input) is turned on. After the END processing of the third scan, HSC2 starts counting.

2nd scan

At the falling edge of M8120 (initialize pulse), M0 is turned on.

M8036 (reset input) is also turned on to initialize HSC2 in the END processing of the second scan.

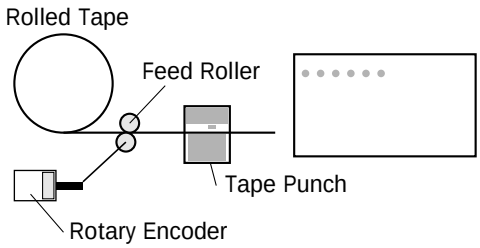
When HSC2 current value reaches 1000, output Q2 (comparison output) is turned on, and HSC2 starts to repeat counting from zero.

Example: Two-phase High-speed Counter (Slim Type CPU Module)

This example demonstrates a program for two-phase high-speed counter HSC1 to punch holes in a paper tape at regular intervals.

Description of Operation

A rotary encoder is linked to the tape feed roller directly, and the output pulses from the rotary encoder are counted by the two-phase high-speed counter in the MicroSmart CPU module. When the high-speed counter counts 2,700 pulses, the comparison output is turned on. When the comparison output is turned on, the high-speed counter continues another cycle of counting. The comparison output remains on for 0.5 second to punch holes in the tape, and is turned off before the high-speed counter counts 2,700 pulses again.

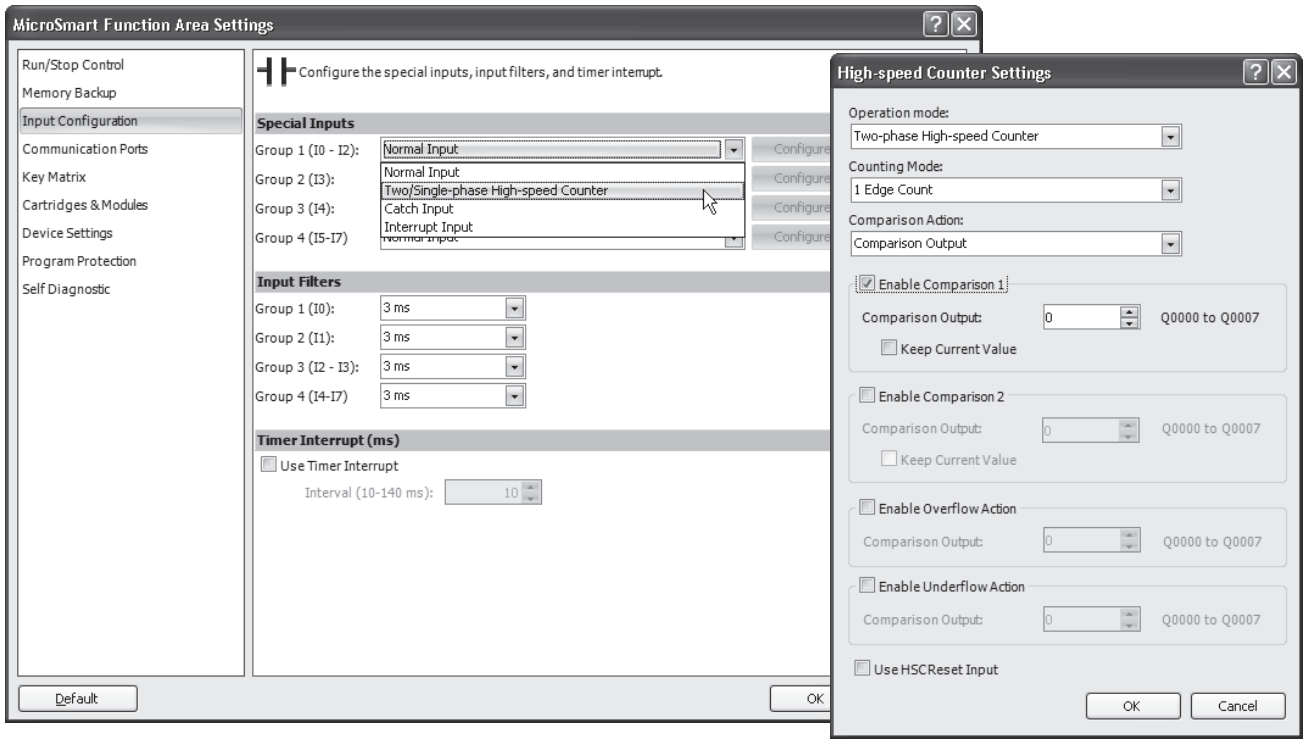


Program Parameters

PLC Selection		FC5A-D32
Function Area Settings	Group 1 (I0-I2)	Two/Single-phase High-speed Counter
	Enable Comparison 1	Yes
	Comparison Output	Q1
	Keep Current Value	No
	Enable Comparison 2	No
	Enable Overflow Action	No
	Enable Underflow Action	No
Special Data Registers	HSC Preset Value 1 High Word (D8212)	0
	HSC Preset Value 1 Low Word (D8213)	2700
	HSC Reset Value High Word (D8216)	0
	HSC Reset Value Low Word (D8217)	0

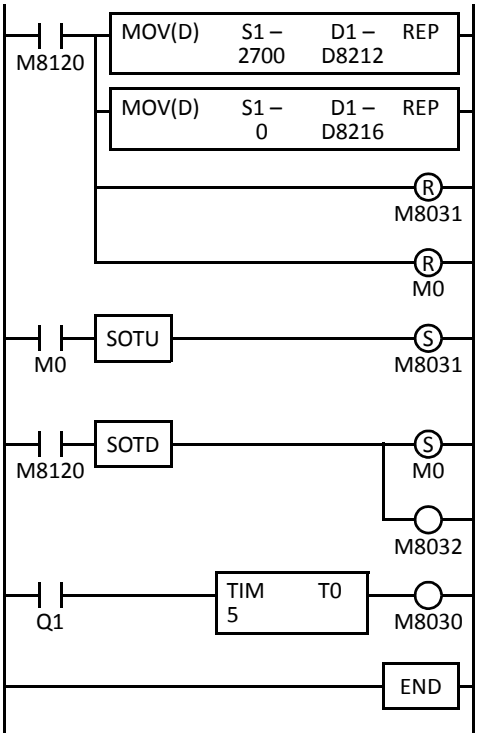
Note: This example does not use the phase Z signal (input I2).

Programming WindLDR



Ladder Diagram

When the MicroSmart starts operation, preset value 2700 is stored to preset value special data registers D8212 and D8213. Gate input special internal relay M8031 is turned on at the end of the third scan to start the high-speed counter to count input pulses.



M8120 is the initialize pulse special internal relay.

1st scan

MOV instruction stores a preset value of 2700 to D8212/D8213 (preset value 1).

MOV instruction stores a reset value of 0 to D8216/D8217 (reset value).

M8031 (gate input) is turned off.

M0 is turned off.

3rd scan

At the rising edge of M0, M8031 (gate input) is turned on. After the END processing of the third scan, HSC1 starts counting.

2nd scan

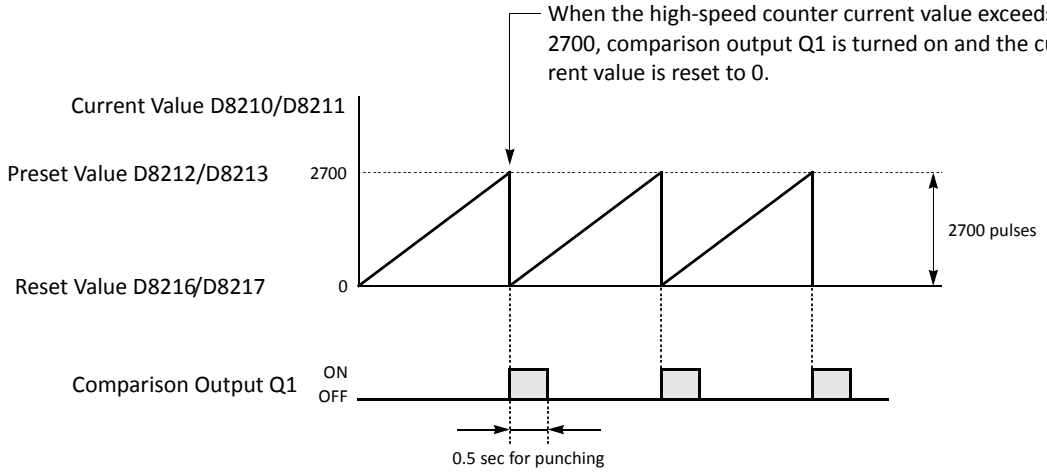
At the falling edge of M8120 (initialize pulse), M0 is turned on.

M8032 (reset input) is also turned on to initialize HSC1 in the END processing of the second scan.

When HSC1 current value reaches 2700, output Q1 (comparison output) is turned on to start timer T0. HSC1 starts to repeat counting.

When the timer times out 0.5 sec, M8030 (comparison output reset) is turned on to turn off output Q1.

Timing Chart



Frequency Measurement

The pulse frequency of input signals to input terminals I1, I3, I4, and I5 (all-in-one) or I7 (slim) can be counted using the high-speed counter function. The high-speed counter counts input pulses within a given period, calculates input pulse frequency, and stores the result to a special data register.

The all-in-one type CPU modules and slim type CPU modules have different frequency measurement configurations.

Frequency Measurement Devices for All-in-One Type CPU Modules

Description	High-speed Counter No.			
	HSC1	HSC2	HSC3	HSC4
Input Terminal	I1	I3	I4	I5
Gate Input	M8031	M8035	M8041	M8045
Frequency Measurement Value	D8060	D8062	D8064	D8066
Frequency Measurement Range	4 Hz to 50 kHz	4 Hz to 5 kHz		
Measurement Error	4 Hz to 4 kHz: ±10% maximum 4 kHz and above: ±0.1% maximum			
Calculation Period	Below 4 kHz: 1 sec maximum 4 kHz and above: 250 ms maximum			

Frequency Measurement Devices for Slim Type CPU Modules

Description		High-speed Counter No.			
		HSC1	HSC2	HSC3	HSC4
Input Terminal		I1	I3	I4	I7
Gate Input		M8031	M8035	M8041	M8045
Frequency Measurement Value	**High Word**	D8060	D8062	D8064	D8066
	Low Word	D8061	D8063	D8065	D8067
Frequency Measurement Range		4 Hz to 100 kHz			
Measurement Error		4 Hz to 4 kHz: ±10% maximum 4 kHz and above: ±0.1% maximum			
Calculation Period		Below 4 kHz: 1 sec maximum 4 kHz and above: 250 ms maximum			

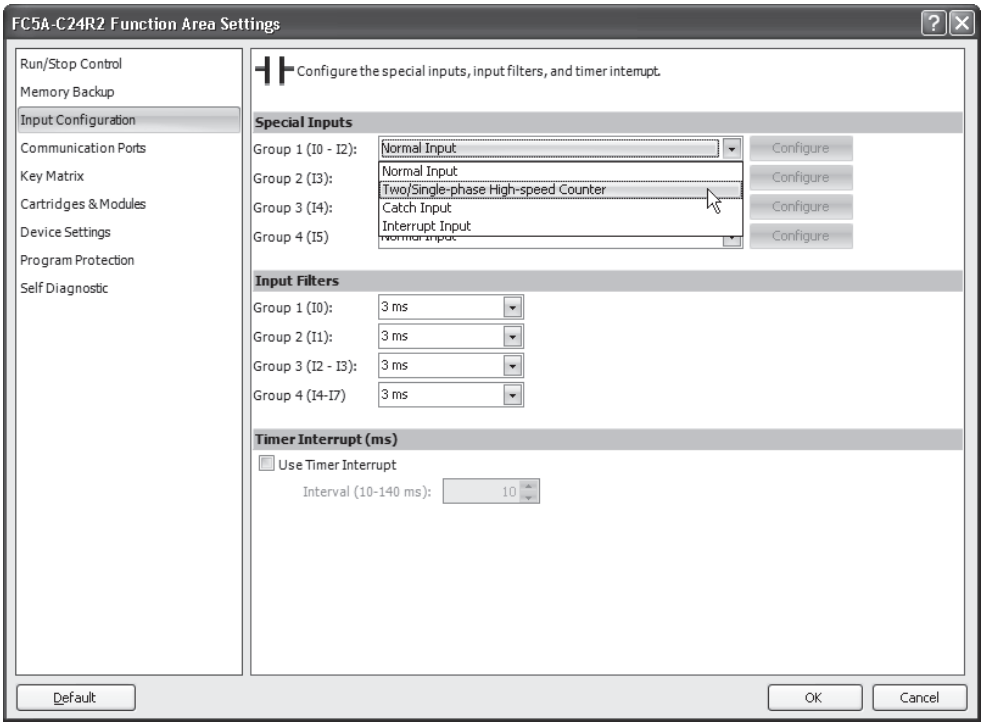
Precautions for Using Frequency Measurement Function

- High-speed counters cannot be used for the group in which frequency measurement is used.
- While the gate input is on, the input pulse frequency is measured. To restart frequency measurement, turn off and on the gate input, or stop and run the CPU module.
- Before downloading a user program to the CPU module, turn off the gate input. If a user program is downloaded while the gate input is on, frequency measurement stops.
- Before the measured results are stored in the special data registers, it takes a maximum of calculation period plus one scan time. Using the FRQRF (frequency measurement refresh) instruction in the ladder diagram, the latest value of the frequency measurement can be read out within 250 ms regardless of the input frequency. For the FRQRF instruction, see page 11-12 (Advanced Vol.).
- For wiring the frequency measurement input signals, use a twisted-pair shielded cable.

Programming WindLDR (All-in-One Type CPU Modules)

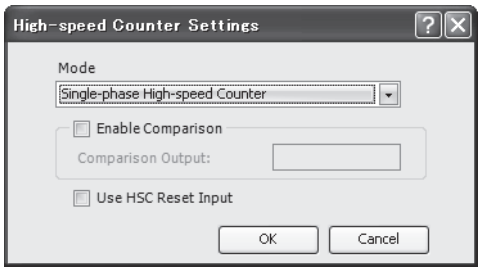
1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.



2. When using frequency measurement, select **Single-phase High-speed Counter** in the Groups 1 through 4 pull-down list boxes.

Do not make other changes.



Catch Input

The catch input function is used to receive short pulses from sensor outputs regardless of the scan time. Input pulses shorter than one scan time can be received. Four inputs I2 through I5 can be designated to catch a rising or falling edge of short input pulses, and the catch input statuses are stored to special internal relays M8154 through M8157, respectively. The Function Area Settings dialog box is used to designate inputs I2 through I5 as a catch input.

Normal input signals to input terminals are read when the END instruction is executed at the end of a scan.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Catch Input Specifications

Minimum Turn ON Pulse Width	All-in-one type: 40 µs	Slim type: 5 µs (I3, I4), 40 µs (I2, I5)
Minimum Turn OFF Pulse Width	All-in-one type: 150 µs	Slim type: 5 µs (I3, I4), 150 µs (I2, I5)

Note: Input filter settings have no effect on the catch inputs. For the input filter function, see page 5-42.

Catch Input Terminals and Special Internal Relays for Catch Inputs

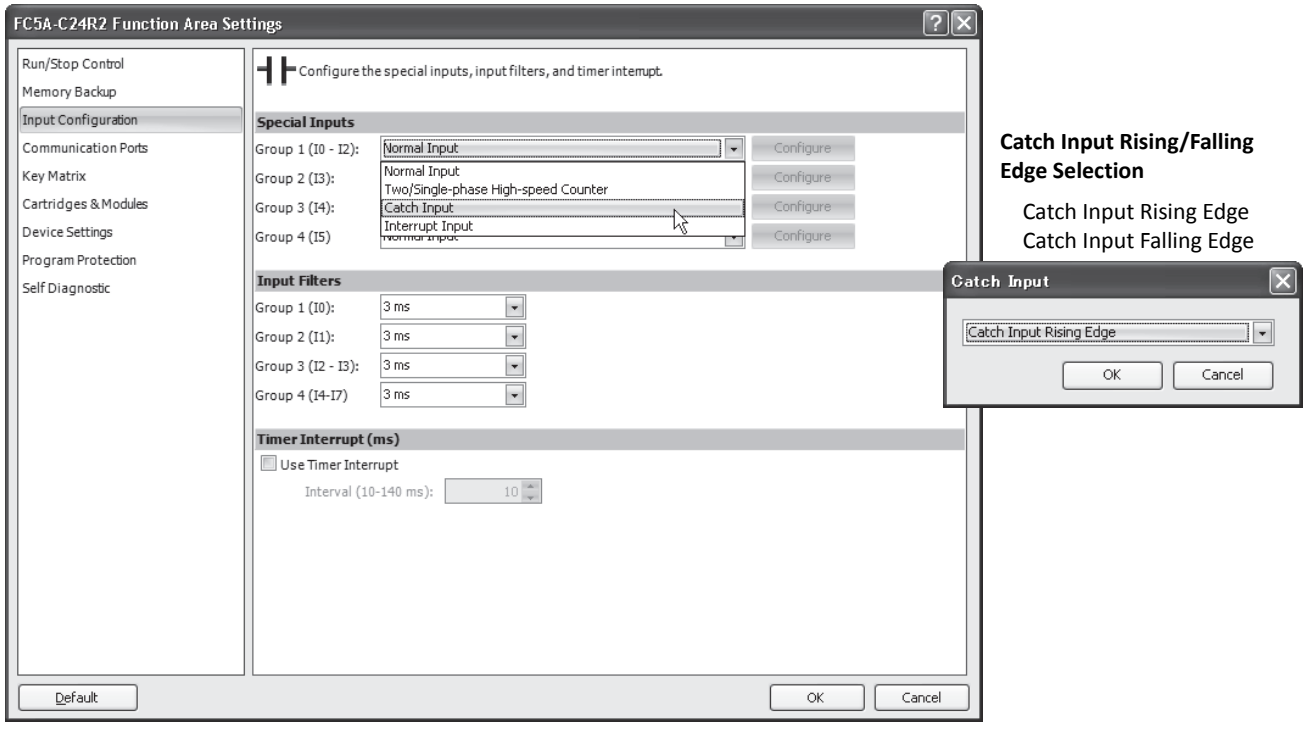
Group	Catch Input No.	Special Internal Relay for Catch Input
Group 1	I2	M8154
Group 2	I3	M8155
Group 3	I4	M8156
Group 4	I5	M8157

Note: For wiring the catch input signals, use a twisted-pair shielded cable.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.

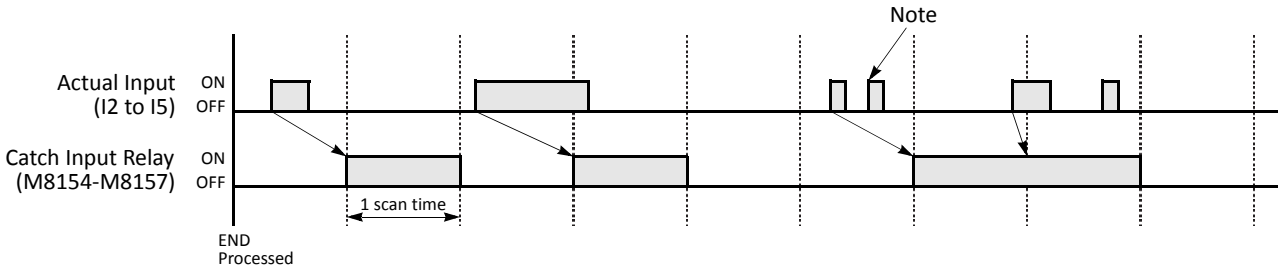


Catch Input Rising/Falling Edge Selection

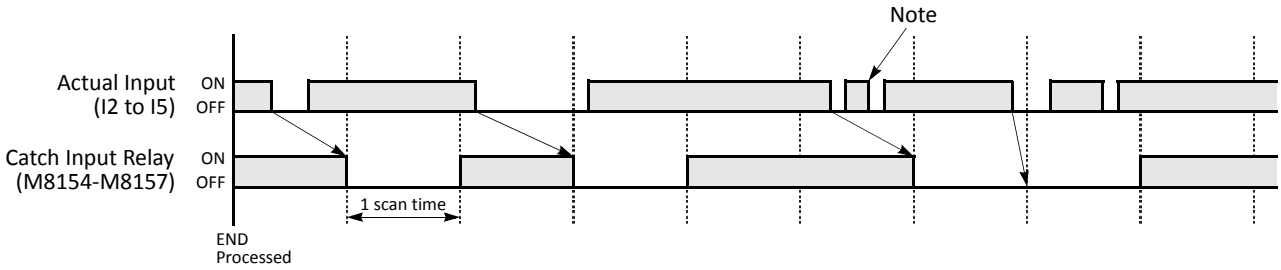
Catch Input Rising Edge
Catch Input Falling Edge

2. Select **Catch Input** in the Groups 1 through 4 pull-down list boxes. The Catch Input dialog box appears.
3. Select **Catch Input Rising Edge** or **Catch Input Falling Edge** in the pull-down list.

Catching Rising Edge of Input Pulse



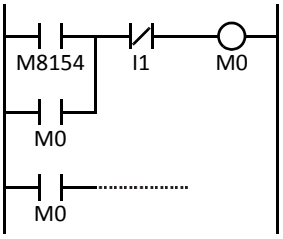
Catching Falling Edge of Input Pulse



Note: When two or more pulses enter within one scan, subsequent pulses are ignored.

Example: Maintaining Catch Input

When a catch input is received, the catch input relay assigned to a catch input is turned on for only one scan. This example demonstrates a program to maintain a catch input status for more than one scan.



Input I2 is designated as a catch input using the Function Area Settings.

When input I2 is turned on, special internal relay M8154 is turned on, and M0 is maintained in the self-holding circuit.

When NC input I1 is turned off, the self-holding circuit is unlatched, and M0 is turned off.

M0 is used as an input condition for the subsequent program instructions.

Interrupt Input

All MicroSmart CPU modules have an interrupt input function. When a quick response to an external input is required, such as positioning control, the interrupt input can call a subroutine to execute an interrupt program.

Four inputs I2 through I5 can be designated to execute interrupt at a rising and/or falling edge of input pulses. When an interrupt is initiated by inputs I2 through I5, program execution immediately jumps to a predetermined label number stored in special data registers D8032 through D8035, respectively. The Function Area Settings dialog box is used to designate inputs I2 through I5 as an interrupt input, normal input, high-speed counter input, or catch input.

Normal input signals to input terminals are read when the END instruction is executed at the end of a scan.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

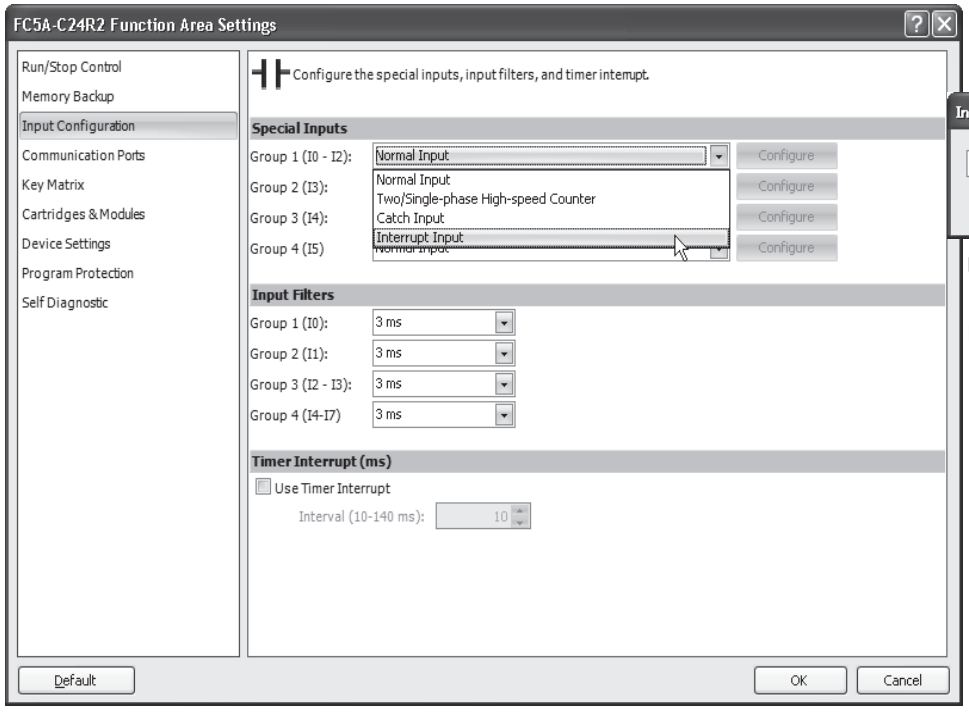
Interrupt Input Terminals, Special Data Registers, and Special Internal Relays for Interrupt Inputs

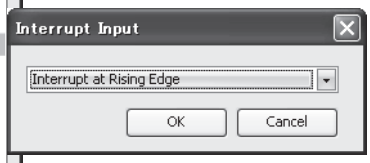
Group	Interrupt Input No.	Interrupt Input Jump Destination Label No.	Interrupt Input Status
Group 1	I2	D8032	M8140
Group 2	I3	D8033	M8141
Group 3	I4	D8034	M8142
Group 4	I5	D8035	M8143

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.





Interrupt Input Rising/Falling Edge Selection

Interrupt at Rising Edge
Interrupt occurs when the interrupt input turns on.

Interrupt at Falling Edge
Interrupt occurs when the interrupt input turns off.

Interrupt at Both Edges
Interrupt occurs when the interrupt input turns on or off.

2. Select **Interrupt Input** in the Groups 1 through 4 pull-down list boxes. the Interrupt Input dialog box appears.

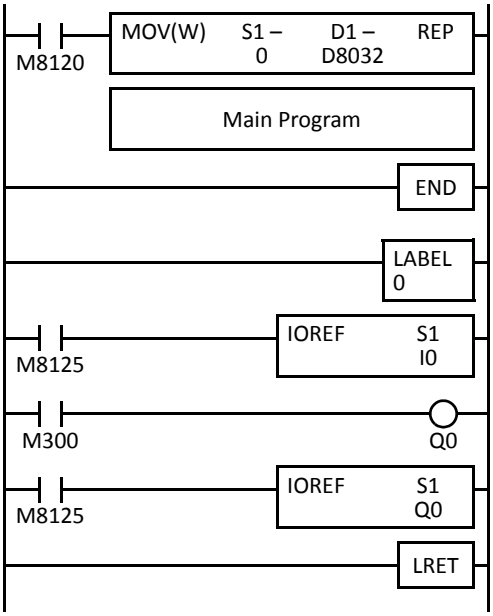
3. Select an interrupt edge in the pull-down list for each group.

Disable and Enable Interrupts

The interrupt inputs I2 through I5 and timer interrupt are normally enabled while the CPU is running, and can also be individually disabled using the DI instruction or enabled using the EI instruction. When interrupt inputs I2 through I5 are enabled, special internal relay M8140 through M8143 are turned on, respectively. See page 11-7 (Advanced Vol.).

Example: Interrupt Input

The following example demonstrates a program of using the interrupt input function, with input I2 designated as an interrupt input. When the interrupt input is turned on, the input I0 status is immediately transferred to output Q0 using the IOREF (I/O refresh) instruction before the END instruction is executed. For the IOREF instruction, see page 11-9 (Advanced Vol.).



M8120 is the initialize pulse special internal relay.

D8032 stores 0 to designate jump destination label 0 for interrupt input I2.

The interrupt program is separated from the main program by the END instruction.

When input I2 is on, program execution jumps to label 0.

M8125 is the in-operation output special internal relay.

IOREF immediately reads input I0 status to internal relay M300.

M300 turns on or off the output Q0 internal memory.

Another IOREF immediately writes the output Q0 internal memory status to actual output Q0.

Program execution returns to the main program.

Insert LRET at the end of the subroutine to return to the main program.

Notes for Using Interrupt Inputs and Timer Interrupt:

- When using an interrupt input or timer interrupt, separate the interrupt program from the main program using the END instruction at the end of the main program.
- When an interrupt program calls another subroutine, a maximum of 3 subroutine calls can be nested. If more than 3 calls are nested, a user program execution error occurs, turning on special internal relay M8004 and the ERR LED.
- When using an interrupt input or timer interrupt, include the label number of the interrupt program to be executed when an interrupt occurs. The label numbers stored in data registers D8032 through D8036 specify the interrupt programs for interrupt inputs I2 through I5 and timer interrupt, respectively.
- When more than one interrupt input is turned on at the same time, interrupt program execution is given priority to inputs I2, I3, I4, and I5, in that order. If an interrupt is initiated while another interrupt program is executed, the subsequent interrupt program is executed after the prior interrupt is completed. Multiple interrupt programs cannot be executed simultaneously.
- Make sure that the execution time of the interrupt program is shorter than interrupt intervals sufficiently.
- Interrupt programs cannot use the following instructions: SOTU, SOTD, TML, TIM, TMH, TMS, CNT, CDP, CUD, SFR, SFRN, WKTIM, WKTBL, DISP, DGRD, TXD1/2, RXD1/2, DI, EI, XYFS, CVXTY, CVYTX, PULS1/2/3, PWM1/2/3, RAMP1/2, ZRN1/2/3, PID, DTML, DTIM, DTMH, DTMS, TTIM, RUNA, and STPA.
- For wiring the interrupt input signals, use a twisted-pair shielded cable.

Timer Interrupt

In addition to the interrupt input as described in the preceding section, all CPU modules have a timer interrupt function. When a repetitive operation is required, the timer interrupt can be used to call a subroutine repeatedly at predetermined intervals of 10 through 140 ms.

The Function Area Settings dialog box is used to enable the timer interrupt and to specify the interval, from 10 to 140 ms, to execute the timer interrupt. When the timer interrupt is enabled, the program execution jumps to the jump destination label number stored in special data register D8036 repeatedly while the CPU is running. When the interrupt program is completed, the program execution returns to the main program at the address where the interrupt occurred.

Since these settings relate to the user program, the user program must be downloaded to the CPU module after changing any of these settings.

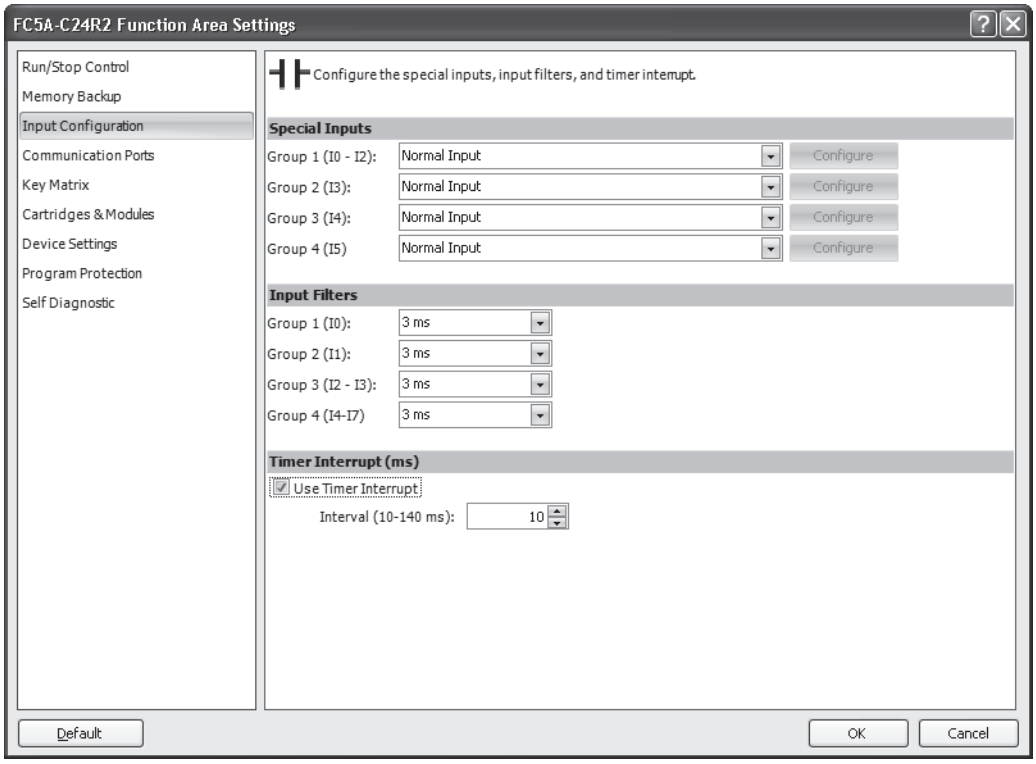
Special Data Register and Special Internal Relay for Timer Interrupt

Interrupt	Special Data Register for Timer Interrupt Jump Destination Label No.	Special Internal Relay for Timer Interrupt Status
Timer Interrupt	D8036	M8144

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.



2. Under the Timer Interrupt, click the check box to use the timer interrupt function.

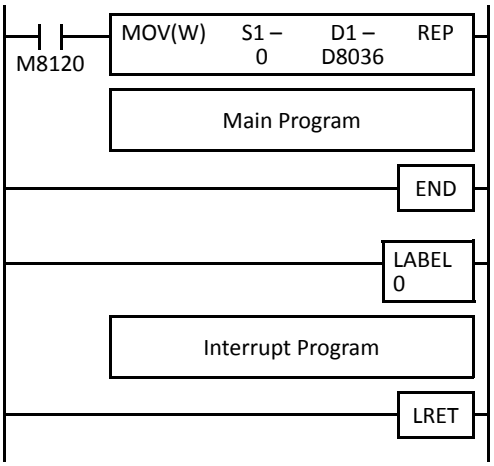
3. Select an interval to execute the timer interrupt, from 10 to 140 ms.

Disable and Enable Interrupts

The timer interrupt and interrupt inputs I2 through I5 are normally enabled while the CPU is running, and can also be individually disabled using the DI instruction or enabled using the EI instruction. When timer interrupt is enabled, M8144 is turned on. When disabled, M8144 is turned off. See page 11-7 (Advanced Vol.).

Example: Timer Interrupt

The following example demonstrates a program of using the timer interrupt function. The Function Area Settings must also be completed to use the timer interrupt function as described on the preceding page.



M8120 is the initialize pulse special internal relay.

D8036 stores 0 to designate jump destination label 0 for timer interrupt.

The interrupt program is separated from the main program by the END instruction.

While the CPU is running, program execution jumps to label 0 repeatedly at intervals selected in the Function Area Settings.

Each time the interrupt program is completed, program execution returns to the main program at the address where timer interrupt occurred.

Insert LRET at the end of the subroutine to return to the main program.

Notes for Using Timer Interrupt and Interrupt Inputs:

- When using a timer interrupt or interrupt input, separate the interrupt program from the main program using the END instruction at the end of the main program.
- When an interrupt program calls another subroutine, a maximum of 3 subroutine calls can be nested. If more than 3 calls are nested, a user program execution error occurs, turning on special internal relay M8004 and the ERR LED.
- When using a timer interrupt or interrupt input, include the label number of the interrupt program to be executed when an interrupt occurs. The label numbers stored in data registers D8032 through D8036 specify the interrupt programs for interrupt inputs I2 through I5 and timer interrupt, respectively.
- If an interrupt is initiated while another interrupt program is executed, the subsequent interrupt program is executed after the prior interrupt is completed. Multiple interrupt programs cannot be executed simultaneously.
- Make sure that the execution time of the interrupt program is shorter than interrupt intervals sufficiently.
- Interrupt programs cannot use the following instructions: SOTU, SOTD, TML, TIM, TMH, TMS, CNT, CDP, CUD, SFR, SFRN, WKTIM, WKTBL, DISP, DGRD, TXD1/2, RXD1/2, DI, EI, XYFS, CVXTY, CVYTX, PULS1/2/3, PWM1/2/3, RAMP1/2, ZRN1/2/3, PID, DTML, DTIM, DTMH, DTMS, TTIM, RUNA, and STPA.

Key Matrix Input

The key matrix input can be programmed using the Function Area Settings in WindLDR to form a matrix with 1 to 16 input points and 2 to 16 output points to multiply input capability. A key matrix with 8 inputs and 4 outputs would equal 32 inputs, for example. The maximum, 16 inputs and 16 outputs, would result in 256 input points. A maximum of 5 sets of key matrix inputs can be programmed for one user program, therefore a maximum of 1280 inputs can be read to the FC5A MicroSmart CPU module.

The input information is stored in consecutive internal relays as many as the quantity of input points multiplied by the quantity of output points, starting at the first internal relay number programmed in the Function Area Settings.

The key matrix input function is available on upgraded CPU modules with system program version 210 or higher.

When using the key matrix input function, DC inputs and transistor outputs must be used.

Since these settings relate to the user program, the user program must be downloaded to the CPU module after changing any of these settings.

⚠ Caution

- To read key matrix inputs, use transistor outputs of either CPU module or transistor output module. If relay outputs are connected to configure the key matrix, the CPU module cannot read the inputs.

Applicable Modules for Inputs and Outputs

To configure a key matrix, use DC inputs and transistor outputs. Applicable CPU and I/O modules are listed in the table below.

Module	For Inputs		For Outputs	
FC5A MicroSmart CPU Modules	FC5A-C24R2 FC5A-D16RK1 FC5A-D32K3 FC5A-D12K1E	FC5A-C24R2C FC5A-D16RS1 FC5A-D32S3 FC5A-D12S1E	FC5A-D16RK1 FC5A-D32K3 FC5A-D12K1E	FC5A-D16RS1 FC5A-D32S3 FC5A-D12S1E
I/O Modules	FC4A-N08B1 FC4A-N16B3 FC4A-M08BR1	FC4A-N16B1 FC4A-N32B3 FC4A-M24BR2	FC4A-T08K1 FC4A-T16K3 FC4A-T32K3	FC4A-T08S1 FC4A-T16S3 FC4A-T32S3

Valid Device Ranges

A maximum of 1280 points (16 inputs × 16 outputs × 5 key matrices) can be read using the key matrix input function. The valid device range depends on the CPU module.

CPU Module	Inputs	Outputs	Internal Relays
FC5A-C10R2, FC5A-C10R2C, FC5A-C10R2D	—	—	—
FC5A-C16R2, FC5A-C16R2C, FC5A-C16R2D	—	—	—
FC5A-C24R2D	—	—	—
FC5A-C24R2, FC5A-C24R2C	I0 - I15, I30 - I107	Q30 - Q107	M0 - M2557
FC5A-D16RK1, FC5A-D16RS1	I0 - I7, I30 - I627	Q0 - Q1, Q30 - Q627	
FC5A-D32K3, FC5A-D32S3	I0 - I17, I30 - I627	Q0 - Q17, Q30 - Q627	
FC5A-D12K1E, FC5A-D12S1E	I0 - I7, I30 - I627	Q0 - Q3, Q30 - Q627	

A maximum of 16 inputs and 16 outputs can be designated. Use inputs or outputs of a CPU module or I/O module separately. Do not straddle a CPU module and an I/O module to designate input or output devices for a key matrix. For example, when the FC5A-D32K3 CPU module is used and input I10 is designated as the first input number, then 16 cannot be designated as the quantity of inputs. When input I10 is designated as the first input number, a maximum of 8 inputs can be used, I10 through I17.

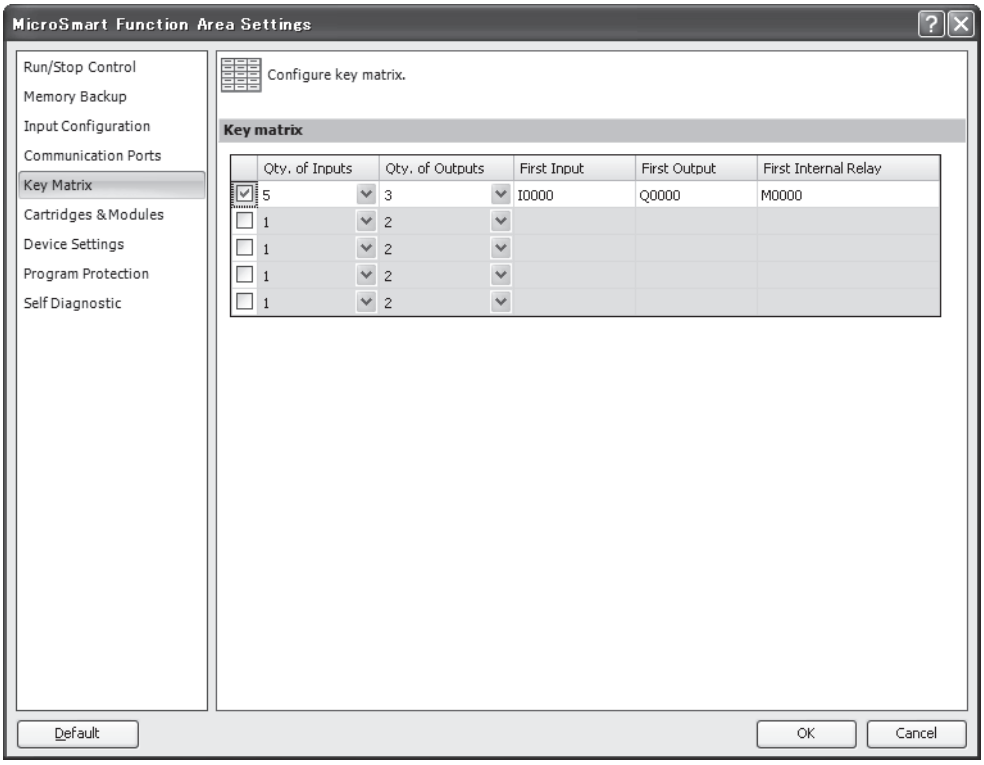
Key matrix input information is stored to internal relays starting with the designated internal relay number. Internal relays as many as input points × output points must be reserved for the key matrix.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Key Matrix**.

The Function Area Settings dialog box for Key Matrix appears.

A maximum of five key matrices can be programmed.



2. Click the check box on the left and enter required data in the fields shown below.

Field	Description
First Input	Enter the first input number used for the key matrix.
Qty of Inputs	Enter the quantity of input points used for the key matrix. Valid range: 1 to 16
First Output	Enter the first output number used for the key matrix.
Qty of Outputs	Enter the quantity of output points used for the key matrix. Valid range: 2 to 16
First Internal Relay	Enter the first internal relay number used for storing key matrix input information. Internal relays as many as input points × output points must be reserved.

3. Click the **OK** button.

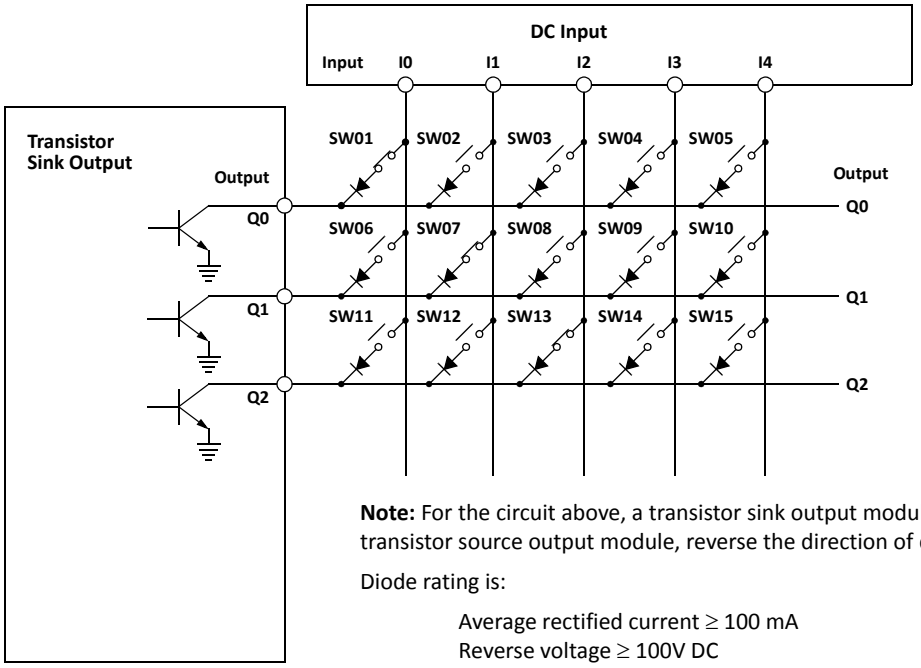
4. Download the user program to the CPU module.

Key Matrix Dialog Box

The screen display shown above is an example to configure a key matrix of 5 input points and 3 output points, starting with input I0 and output Q0. The key matrix information is stored to 15 internal relays starting with M0.

Key Matrix Circuit

The key matrix structure includes sequentially-numbered input points along the top and sequentially-numbered output points along the side. The I/O connecting blocks include a diode and a switch. The following diagram illustrates an example of key matrix circuit consisting of 5 inputs and 3 outputs.



Note: For the circuit above, a transistor sink output module must be used. When using a transistor source output module, reverse the direction of diodes.

Diode rating is:

Average rectified current ≥ 100 mA
Reverse voltage ≥ 100V DC

Internal Relay Allocation

The example of a key matrix configuration shown on page 5-39 stores input information to 15 internal relays starting with internal relay M0. The switches are assigned to internal relays as shown below:

Outputs	Inputs				
	I0	**I1**	**I2**	**I3**	**I4**
Q0	M0 (SW01)	M1 (SW02)	M2 (SW03)	M3 (SW04)	M4 (SW05)
Q1	M5 (SW06)	M6 (SW07)	M7 (SW08)	M10 (SW09)	M11 (SW10)
Q2	M12 (SW11)	M13 (SW12)	M14 (SW13)	M15 (SW14)	M16 (SW15)

Maximum Input Read Time

The maximum period of time required to read input signals in the key matrix circuit is called the maximum input read time, which can be calculated using the following formula. When the input ON duration is shorter than the maximum input read time, the input may not be read.

$$\text{Maximum Input Read Time} = \text{Output Points} \times \left(\left[\frac{\text{I/O Delay Time}}{\text{Scan Time}} + 1 \right] + 1 \right) \times \text{Scan Time}$$

- The scan time can be confirmed using special data register D8023 (scan time current value in ms).
- The I/O delay time depends on the modules used for inputs of the key matrix. The I/O delay time for CPU modules and I/O modules are listed in the table below.
- The value of [X] in the above formula represents the maximum integer value less than or equal to X. For example, [0.23] represents 0, and [2.5] represents 2.

	CPU Module		I/O Module	
Module Used for Key Matrix Inputs	FC5A-C24R2 FC5A-D16RK1 FC5A-D32K3 FC5A-D12K1E	FC5A-C24R2C FC5A-D16RS1 FC5A-D32S3 FC5A-D12S1E	FC4A-N08B1 FC4A-N16B3 FC4A-M08BR1	FC4A-N16B1 FC4A-N32B3 FC4A-M24BR2
I/O Delay Time	Approx. 5 ms + Input filter value (Note 1)		Approx. 10 ms (Note 2)	

Note 1: The input filter can be selected using WindLDR. From the WindLDR menu bar, select **Configuration** > **Input Configuration** > **Input Filters**. Different input filter values can be selected for inputs I0 through I7 in four groups. When the inputs used for the key matrix contain different input filter values, the largest input filter value takes effect for the I/O delay time.

Note 2: When using expansion interface modules (FC5A-EXM2 or FC5A-EXM1M and FC5A-EXM1S) for key matrix inputs or outputs, the I/O delay time is approximately 22 ms.

Example: Calculating Maximum Input Read Time

This example calculates the maximum input read time for a key matrix consisting of 4 inputs and 16 outputs to read 64 points of input signals.

Conditions	**MicroSmart System Setup**		FC5A-D16RK1 + FC4A-T16K3
	Function Area Settings	**Key Matrix Input**	I4 to I7 (4 inputs)
		Key Matrix Output	Q30 to Q47 (16 outputs)
		Input Filter (Group 4)	3 ms
	Scan Time		10 ms (D8023 value)
	I/O Delay Time		5 ms + Input filter value (3 ms) = 8 ms
Calculation Formula			$\text{Output Points} \times \left(\left[\frac{\text{I/O Delay Time}}{\text{Scan Time}} + 1 \right] + 1 \right) \times \text{Scan Time}$ $= 16 \times \left(\left[\frac{8\ \text{ms}}{10\ \text{ms}} + 1 \right] + 1 \right) \times 10\ \text{ms}$ $= 16 \times ([1.8] + 1) \times 10\ \text{ms}$ $= 16 \times (1 + 1) \times 10\ \text{ms}$
Maximum Input Read Time			320 ms

Input Filter

The input filter function is used to reject input noises. The catch input function described in the preceding section is used to read short input pulses to special internal relays. On the contrary, the input filter rejects short input pulses when the MicroSmart is used with input signals containing noises.

Different input filter values can be selected for inputs I0 through I7 in four groups using the Function Area Settings. Selectable input filter values to pass input signals are 0 ms, and 3 through 15 ms in 1-ms increments. Default value is 3 ms for all inputs I0 through I7. Inputs I10 and above on 16- and 24-I/O all-in-one type CPU modules and 32-I/O slim type CPU modules are provided with a fixed filter of 3 ms. Inputs I30 and above on all expansion input modules have a fixed filter of 4 ms. The input filter rejects inputs shorter than the selected input filter value minus 2 ms.

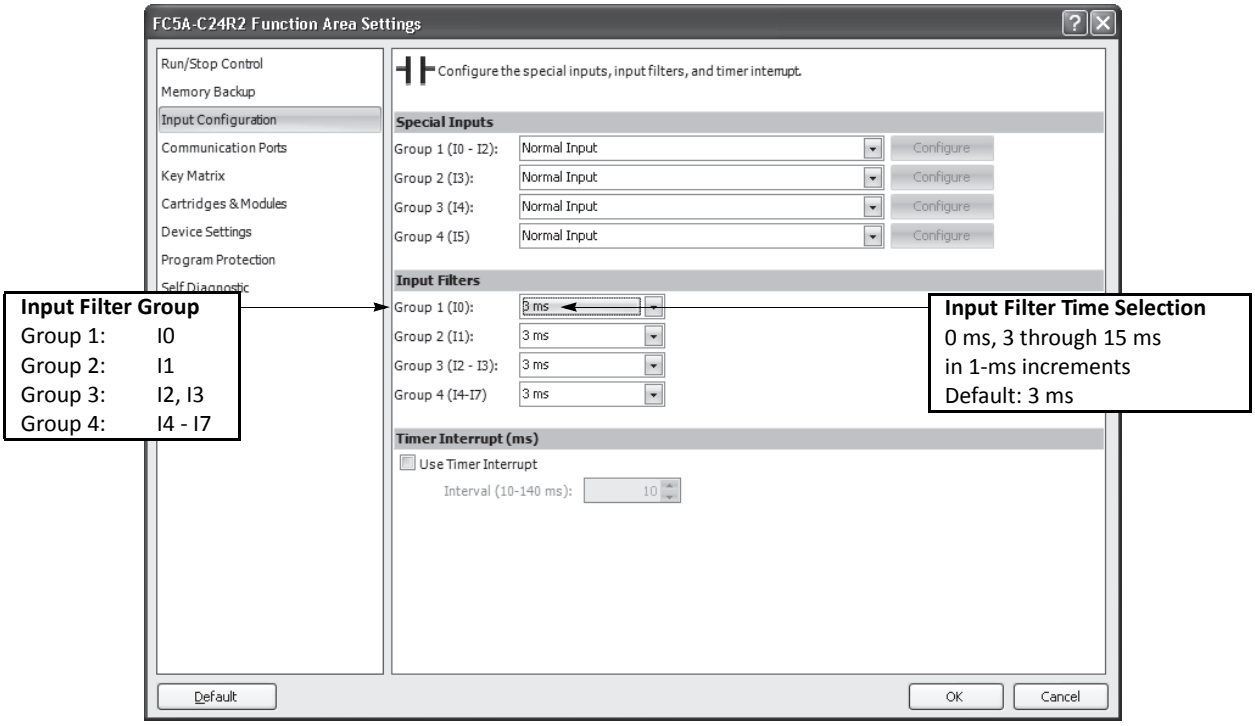
Normal inputs require a pulse width of the filter value plus one scan time to receive input signals. When using the input filter function, select **Normal Input** under Special Inputs on the Input Configuration dialog box in the Function Area Settings.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Input Configuration**.

The Function Area Settings dialog box for Input Configuration appears.



2. Select an input filter value for each group of inputs.

Input Filter Values and Input Operation

Depending on the selected values, the input filter has three response areas to reject or pass input signals.

Reject area:	Input signals do not pass the filter (selected filter value minus 2 ms).
Indefinite area:	Input signals may be rejected or passed.
Pass area:	Input signals pass the filter (selected filter value).

Example: Input Filter 8 ms

To reject input pulses of 6 ms or less, select input filter value of 8 ms. Then input pulses of 8 ms plus one scan time are accepted correctly at the END processing.

		6 ms	8 ms + 1 scan
Input	Rejected	Indefinite	Accepted

Communication Refresh for Port 3 through Port 7

The expansion communication buffers for port 3 through port 7 are refreshed in the END processing. Communication refresh option for port 3 through port 7 can be used to refresh the buffers every 10 ms during the scan. When the buffers are refreshed, the send data in the buffers are sent out and the receive data in the buffer are processed immediately.

COMRF instructions can also be programmed to refresh the communication buffers for port 3 through port 7 in any place in the ladder program where you want to refresh the buffers. When “Every 10 ms” under “Communication Refresh for Port 3 through Port 7” is selected in the Function Area Settings dialog box, COMRF instructions programmed in the ladder program have no effects. For COMRF instruction, see page 11-13 (Advanced Vol.).

Regardless of the communication refresh option for port 3 through port 7, the expansion communication buffers for port 3 through port 7 are always refreshed in the END processing.

Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing this setting.

Communication Refresh for Port 3 through port 7 can be used with the CPU module system program version 220 or higher.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Comm. Ports**.

The Function Area Settings dialog box for Communication Ports appears.

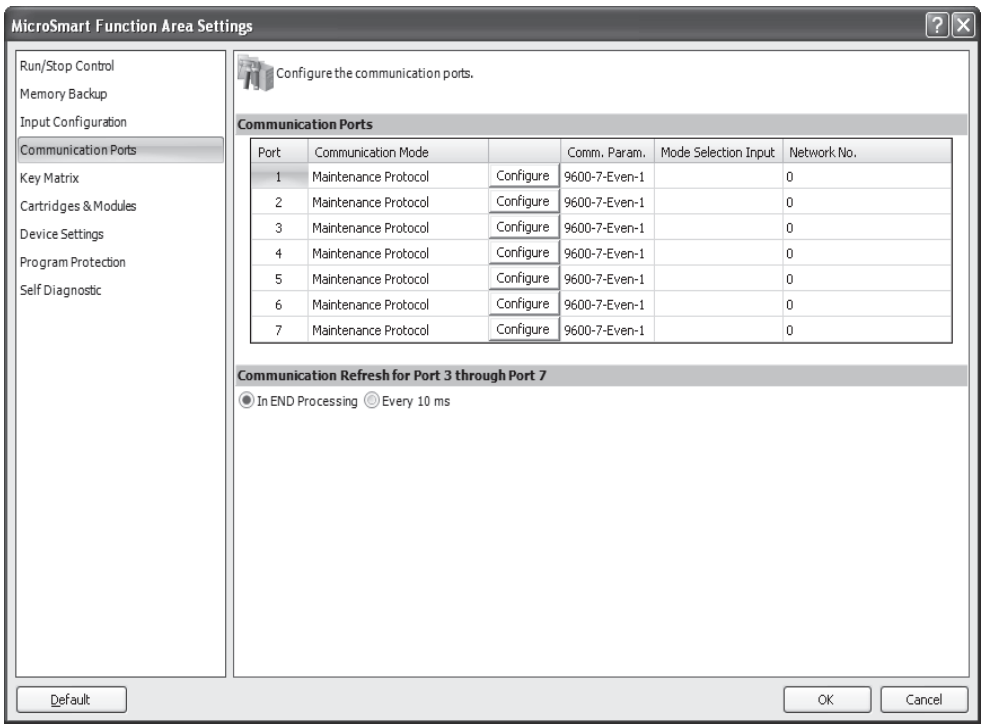
2. Click the In END Processing or Every 10 ms button.

   In END Processing (Default):

   Click this button to refresh the expansion communication buffers for port 3 through port 7 in the END processing.

   Every 10 ms:

   Click this button to refresh the expansion communication buffers for port 3 through port 7 every 10 ms during the scan.



3. Click the **OK** button.

User Program Protection

The user program in the MicroSmart CPU module can be protected from reading, writing, or both using the Function Area Settings in WindLDR.

Upgraded CPU modules with system program version 210 or higher have an option for read protection without a password, making it possible to inhibit reading completely.

Warning

- Before proceeding with the following steps, make sure to note the protect code, which is needed to disable the user program protection. If the user program in the MicroSmart CPU module is write- or read/write-protected, the user program cannot be changed without the protect code.

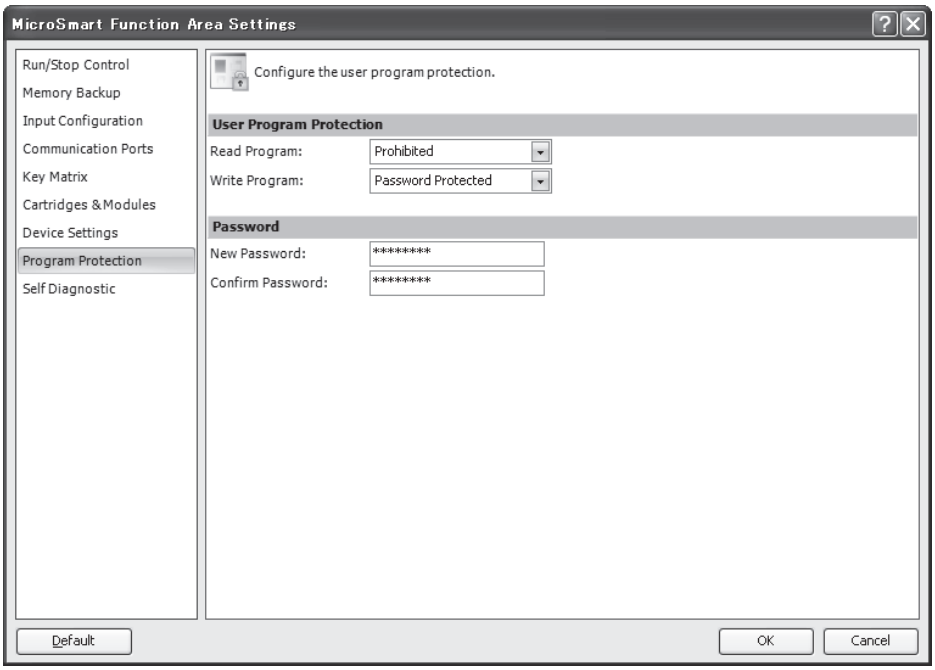
Caution

- If the user program is read-protected without using a password, the read protection cannot be temporarily disabled using the password, thus the user program cannot be read out by any means. To disable the read protection, download another user program without user program protection.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Program Protection**.

The Function Area Settings dialog box for Program Protection appears.



2. Under **User Program Protection**, select required protect modes for **Read Program** and **Write Program** in the pull-down list.

Unprotected:	The user program in the CPU module can be read and written without a password.
Password Protected:	Prevents unauthorized copying or inadvertent replacement of the user program. The protection can be temporarily disabled using a predetermined password.
Prohibited:	Prevents copying of the user program completely. This option is available for read protection only and can not be temporarily disabled using a password. To select this option, use a CPU module with system program ver. 210 or higher and WindLDR ver 5.31 or higher

3. After selecting a required protect mode, enter a password of 1 through 8 ASCII characters from the key board in the **New Password** field, and enter the same password in the **Confirm Password** field.

4. Click the **OK** button and download the user program to the MicroSmart after changing any of these settings.

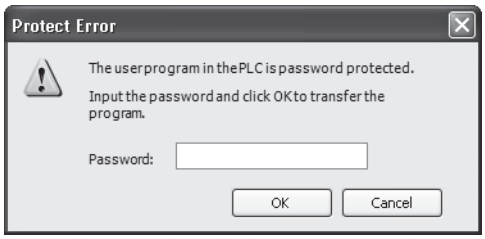
Disabling Protection

When the user program is password-protected against read and/or write, the protection can be temporarily disabled using WindLDR.

If the user program is read-prohibited, the read protection cannot be disabled, thus the user program cannot be read out by any means. To disable the read protection, download another user program without user program protection.

1. From the WindLDR menu bar, select **Online** > **Download or Upload**.

When the user program in the CPU module is read and/or write protected, the Protect Error dialog box appears. When program verification or online edit is attempted, the Protect Error dialog box appears.



2. Enter the password and click the **OK** button.

The user program protection is disabled only temporarily. When the CPU module is powered up again, the protection designated in the user program takes effect again.

To disable or change the protection permanently, change the protection settings and download the user program.

32-bit Data Storage Setting

When the double-word, long, or float data type is selected for the source or destination device, the data is loaded from or stored to two consecutive data registers. The order of two devices can be selected from the following two settings in the Function Area Settings.

This setting can be used on CPU modules with system program version 110 or higher.

Setting	Description
From Upper Word	When a data register, timer, or counter is used as a double-word device, the high-word data is loaded from or stored to the first device selected. The low-word data is loaded from or stored to the subsequent device. This is identical with the 32-bit data storage of OpenNet Controller and FC4A MicroSmart, and is the default setting of the FC5A MicroSmart.
From Lower Word	When a data register, timer, or counter is used as a double-word device, the low-word data is loaded from or stored to the first device selected. The high-word data is loaded from or stored to the subsequent device. This is identical with the 32-bit data storage of IDEC FA Series PLCs.

Devices

When the devices listed below are used as a double-word device, two consecutive devices are processed according to the 32-bit data storage settings.

Device	Device Address
Data Register	D0 - D1999
Expansion Data Register	D2000 - D7999
Special Data Register	D8000 - D8499
Extra Data Register	D10000 - D49999
Timer	T0 - T255
Counter	C0 - C255

Instructions

The 32-bit data storage setting has the effect on the following instructions: CNTD, CDPD, CUDD, MOV, MOVN, IMOV, IMOVN, NSET, NRS, TCCST, CMP=, CMP<>, CMP<, CMP>, CMP<=, CMP>=, ICMP>=, LC=, LC<>, LC<, LC>, LC<=, LC>=, ADD, SUB, MUL, DIV, ROOT, ANDW, ORW, XORW, BCDLS, ROTL, ROTR, HTOB, BTOH, BTOA, ATOB, CVDT, AVRG, PULS, PWM, RAMP, RAD, DEG, SIN, COS, TAN, ASIN, ACOS, ATAN, LOGE, LOG10, EXP, and POW.

Data Register Allocation

The 32-bit data storage setting has the effect on data register allocation of the following functions: PULS, PWM, and RAMP instructions, frequency measurement, and high-speed counter. All of these functions can be used on the slim type CPU modules only.

Control Registers for PULS or PWM Instruction

Device Address	Description	From Upper Word	From Lower Word
S1+3	Preset Value 1 to 100,000,000 (05F5E100h)	High Word	Low Word
S1+4		Low Word	High Word
S1+5	Current Value 1 to 100,000,000 (05F5E100h) (PULS1, PULS3, PWM1, and PWM3 only)	High Word	Low Word
S1+6		Low Word	High Word

Control Registers for RAMP Instruction

Device Address	Description	From Upper Word	From Lower Word
S1+6	Preset Value 1 to 100,000,000 (05F5E100h)	High Word	Low Word
S1+7		Low Word	High Word
S1+8	Current Value 1 to 100,000,000 (05F5E100h)	High Word	Low Word
S1+9		Low Word	High Word

Special Data Registers for Frequency Measurement

Device Address	Description	From Upper Word	From Lower Word
D8060	Frequency Measurement Value I1	High Word	Low Word
D8061		Low Word	High Word
D8062	Frequency Measurement Value I3	High Word	Low Word
D8063		Low Word	High Word
D8064	Frequency Measurement Value I4	High Word	Low Word
D8065		Low Word	High Word
D8066	Frequency Measurement Value I7	High Word	Low Word
D8067		Low Word	High Word

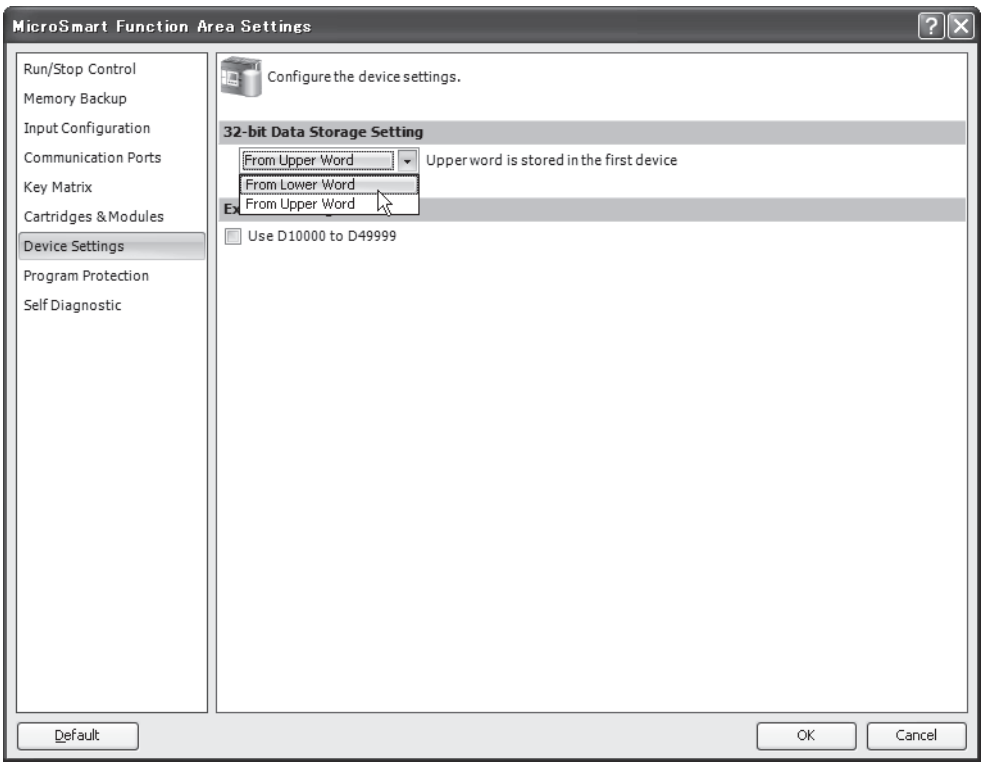
Special Data Registers for High-speed Counters

Device Address	Description	From Upper Word	From Lower Word
D8210	High-speed Counter 1 (I0-I2) Current Value	High Word	Low Word
D8211		Low Word	High Word
D8212	High-speed Counter 1 (I0-I2) Preset Value 1	High Word	Low Word
D8213		Low Word	High Word
D8214	High-speed Counter 1 (I0-I2) Preset Value 2	High Word	Low Word
D8215		Low Word	High Word
D8216	High-speed Counter 1 (I0-I2) Reset Value	High Word	Low Word
D8217		Low Word	High Word
D8218	High-speed Counter 2 (I3) Current Value	High Word	Low Word
D8219		Low Word	High Word
D8220	High-speed Counter 2 (I3) Preset Value	High Word	Low Word
D8221		Low Word	High Word
D8222	High-speed Counter 3 (I4) Current Value	High Word	Low Word
D8223		Low Word	High Word
D8224	High-speed Counter 3 (I4) Preset Value	High Word	Low Word
D8225		Low Word	High Word
D8226	High-speed Counter 4 (I5-I7) Current Value	High Word	Low Word
D8227		Low Word	High Word
D8228	High-speed Counter 4 (I5-I7) Preset Value 1	High Word	Low Word
D8229		Low Word	High Word
D8230	High-speed Counter 4 (I5-I7) Preset Value 2	High Word	Low Word
D8231		Low Word	High Word
D8232	High-speed Counter 4 (I5-I7) Reset Value	High Word	Low Word
D8233		Low Word	High Word

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Device Settings**.

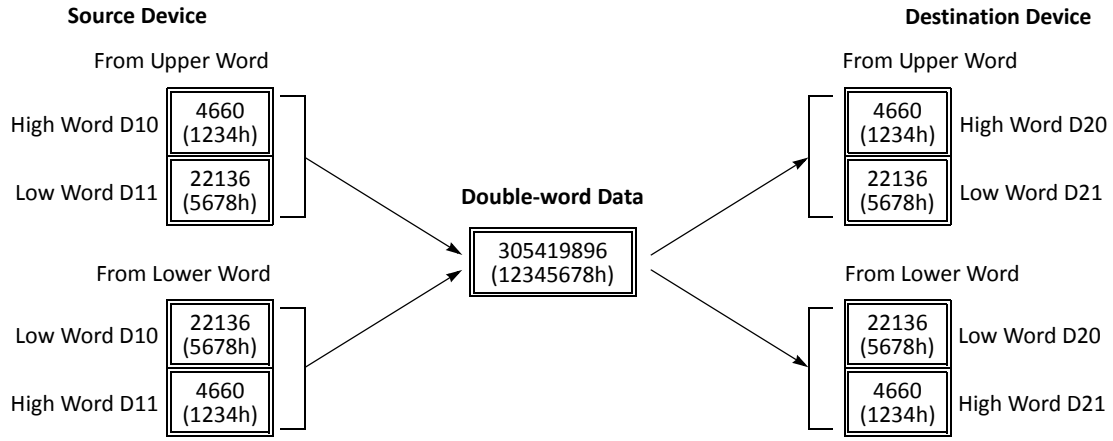
The Function Area Settings dialog box for Device Settings appears.



2. Under **32-bit Data Storage Setting**, select **From Upper Word** or **From Lower Word** in the pull-down list.

Example: 32-bit Data Storage Setting

When data register D10 is designated as a double-word source device and data register D20 is designated as a double word destination device, the data is loaded from or stored to two consecutive devices according the 32-bit data storage setting as illustrated below.



RUN LED Flashing Mode

The RUN LED flashing mode has been added to the MicroSmart CPU modules. The internal status of the MicroSmart CPU module can be seen with the flashing status of the RUN LED. The RUN LED flashes slowly or quickly according to the status of the MicroSmart as shown below.

The RUN LED flashing mode can be used with the CPU module system program version 200 or higher. This setting is always enabled in the FC5A-D12K1E and D12S1E.

RUN LED status	Description
Slow Flash (1-sec interval)	Test program has been downloaded to the MicroSmart but not been confirmed nor canceled during the online editing.
	Timer/counter preset values have been changed but not been confirmed nor canceled.
Quick Flash (100-ms interval)	During the user program in the RAM of the MicroSmart is written to the EEPROM.

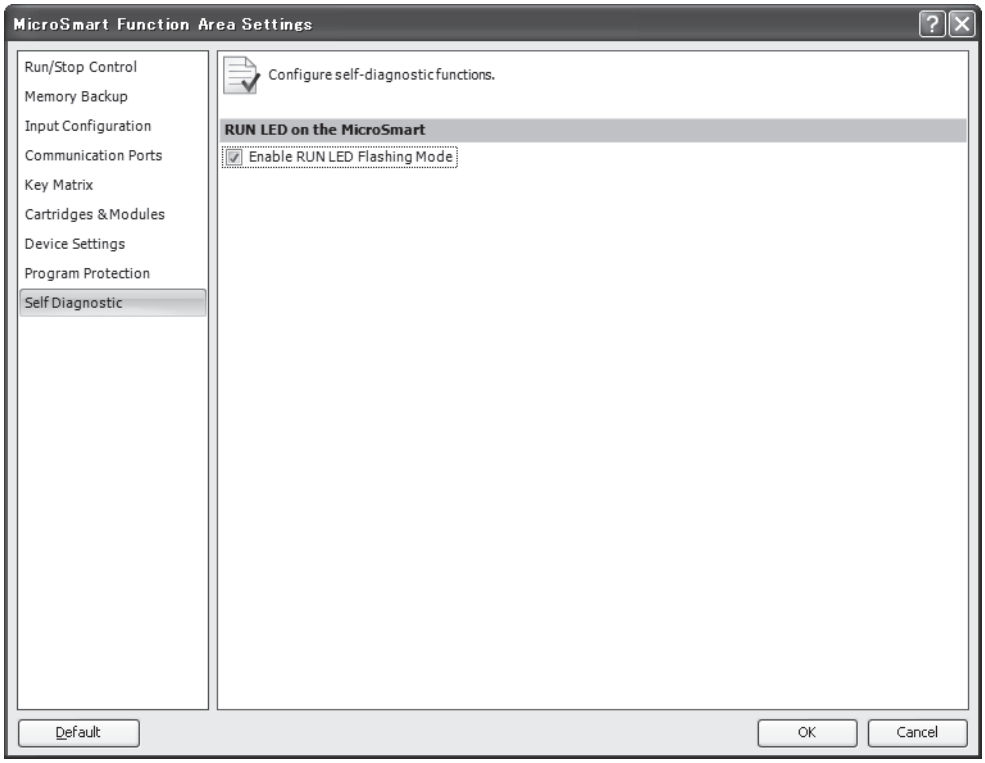
Notes:

- RUN LED flashes when inputs/outputs are forced on/off regardless of the RUN LED flashing mode setting. See page 5-72.
- While RUN LED flashes quickly, do not shut down the CPU module. Otherwise, a fatal error may occur such as user program writing error.

Programming WindLDR

1. From the WindLDR menu bar, select **Configuration** > **Self Diagnostic**.

The Function Area Settings dialog box for Self Diagnostic appears.



2. Click the check box to enable the RUN LED flashing mode.

Constant Scan Time

The scan time may vary whether basic and advanced instructions are executed or not depending on input conditions to these instructions. The scan time can be made constant by entering a required scan time preset value into special data register D8022 reserved for constant scan time. When performing accurate repetitive control, make the scan time constant using this function. The constant scan time preset value can be between 1 and 1,000 ms.

The scan time error is ±1 ms of the preset value normally. When the data link or other communication functions are used, the scan time error may be increased to several milliseconds.

When the actual scan time is longer than the scan time preset value, the scan time cannot be reduced to the constant value.

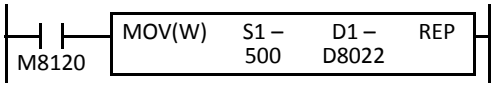
Special Data Registers for Scan Time

In addition to D8022, three more special data registers are reserved to indicate current, maximum, and minimum scan time values.

D8022	Constant Scan Time Preset Value (1 to 1,000 ms)
D8023	Scan Time Current Value (ms)
D8024	Scan Time Maximum Value (ms)
D8025	Scan Time Minimum Value (ms)

Example: Constant Scan Time

This example sets the scan time to a constant value of 500 ms.



M8120 is the initialize pulse special internal relay.

When the CPU starts operation, the MOV (move) instruction stores 500 to special data register D8022.

The scan time is set to a constant value of 500 ms.

Online Edit, Run-Time Program Download, and Test Program Download

Normally, the CPU module has to be stopped before downloading a user program. Using WindLDR 5.0 or higher, the FC5A MicroSmart CPU modules have online edit capabilities which allow to make small modifications to the user program while monitoring the CPU module operation on the WindLDR screen either in the 1:1 or 1:N computer link system.

While monitoring on the WindLDR screen, the modified user program can be downloaded in two ways: run-time program download and test program download.

When executing run-time program download, the modified user program is downloaded to the EEPROM in the CPU module and replaces the original user program permanently. When download is completed, the modified program is executed and monitored on the WindLDR screen.

The test program download replaces the user program in the RAM only and does not overwrite the EEPROM immediately. When test program download is completed, the modified program is executed while the original user program still remains in the EEPROM. Before quitting the test program download, you are asked whether to store the modified user program in the EEPEOM or discard the modified program.

Before performing the online edit, a user program has to be downloaded to the CPU module using the ordinary program download. Add or delete a part of the same user program, or make small changes to the same user program, and download the modified user program using the run-time program download or test program download while the CPU is running to confirm the changes online.

Another method of using this feature is: upload the user program from the CPU module to WindLDR, make changes, and download the modified user program while the CPU is running.

Online Edit

Before starting the online edit using WindLDR, download a user program to the CPU module or upload a user program from the CPU module using the ordinary program download or upload. If user programs do not match between WindLDR and the CPU module, the online edit cannot be used.

Online edit can not change Function Area Settings and Expansion Data Register values. Only ladder diagrams can be edited.

When TIM/CNT preset values have been changed as a result of advanced instructions or through communication, confirm or clear the changes before starting the online edit. See page 7-18.

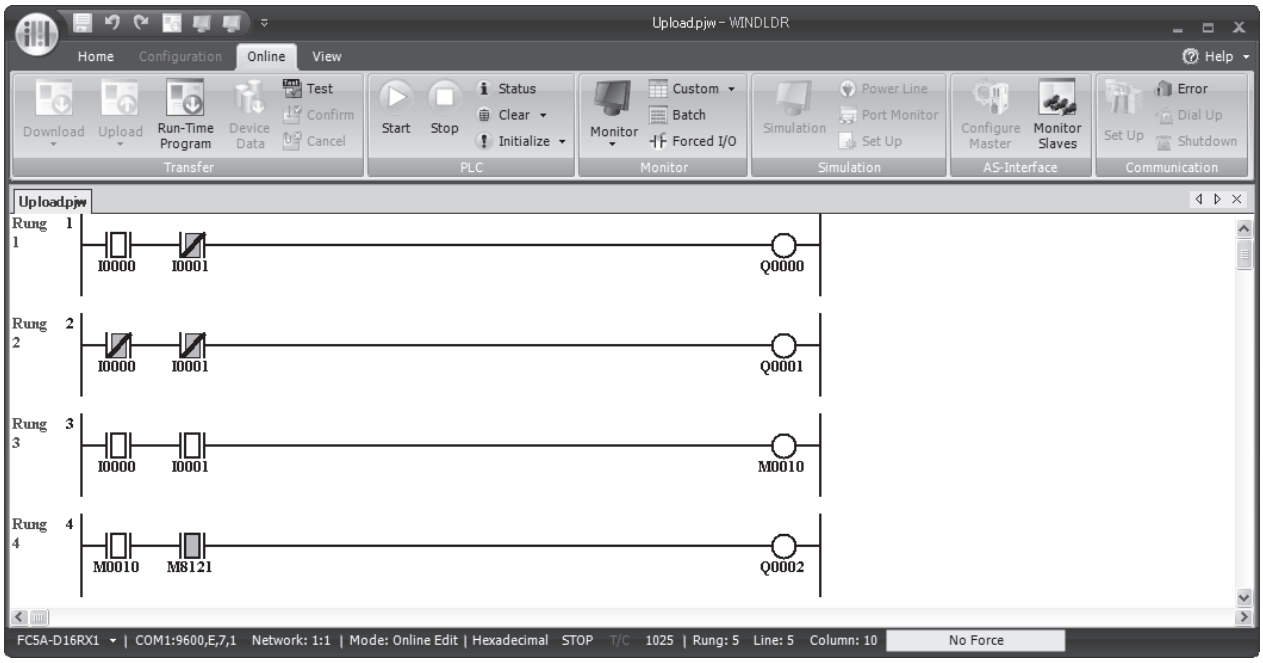
If you do not want to clear the new preset values during the run-time program download or test program download, you can import the new preset values to the user program. Access the PLC Status dialog box from the Online menu in the monitoring mode. Then click the **Confirm** button in the TIM/CNT Change Status field. (The displayed status will switch from **Changed** to **Unchanged**.) Upload the user program, which has new preset values in place of the original preset values. Make changes to the uploaded user program, then perform the run-time program download or test program download. Note that the **Confirm** button has effect on both timer and counter preset values.

Note: When "Enable D10000 to D49999" has been selected in the Function Area Settings for the slim type CPU module, the online edit cannot be used. To use the online edit, deselect the use of extra data registers D10000 to D49999. See page 6-2.

Programming WindLDR

1. From the WindLDR menu bar, select **Online** > **Monitor** > **Online Edit** while the CPU module is running.

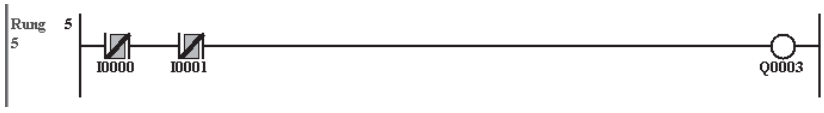
WindLDR enters Online Edit mode where the user program can be modified while monitoring the CPU module operation.



2. Edit the user program.

In this example, a rung is inserted, two NC contacts are programmed in series and connected to an output.

The added program is monitored immediately.



Run-Time Program Download

Caution

- The run-time program download may cause unexpected operation of the MicroSmart. Before starting the run-time program download, make sure of safety after understanding the function correctly.
- If many changes are made to a user program, the possibility of unexpected operation increases. Keep changes to a minimum in one modification and download the user program to make sure of safety.
- If a user program syntax error or user program writing error occurs during the run-time program download, the CPU module is stopped and all outputs are turned off, which may cause hazards depending on the application.
- Immediately when program download is completed, the new user program is executed. It takes a maximum of 60 seconds to store the downloaded program to the ROM. In this period, the scan time is extended by about 10 to 130 ms per scan.
- While executing the run-time program download, do not shut down the CPU module or disconnect the communication cable. Otherwise, a fatal error may occur such as user program writing error, which may cause hazards depending on the application.
- When executing the run-time program download, output statuses are maintained. When an OUT/OUTN instruction is deleted or an output device address has been changed, the output status is maintained after executing the run-time program download. This may cause hazards depending on the application.

Note: For FC5A-D12K1E and FC5A-D12S1E, it is possible to select whether to use a program capacity of 62,400 bytes or 127,800 bytes. If 127,800 bytes is selected, the run-time program download cannot be used.

The run-time program download function is used to download a modified user program to the EEPROM in the CPU module while the CPU is running. When program download is complete, the CPU module executes the new program in the next scan.

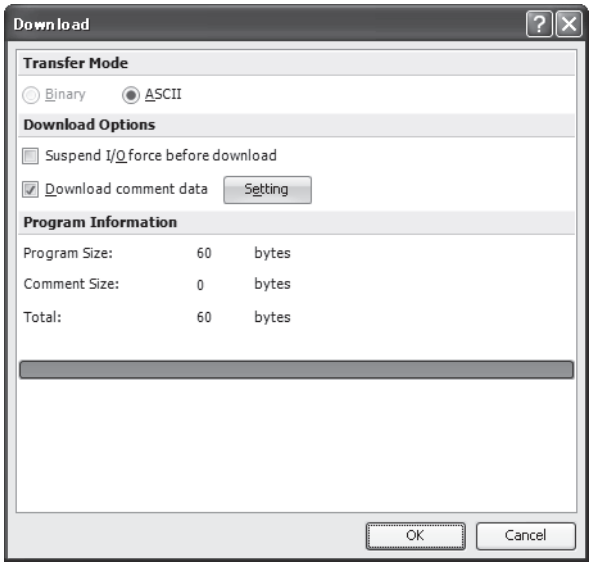
When run-time program download is completed, outputs, internal relays, shift registers, timer/counter current values, and data registers maintain the previous statuses. Timer/counter preset values are replaced by the new values.

Programming WindLDR

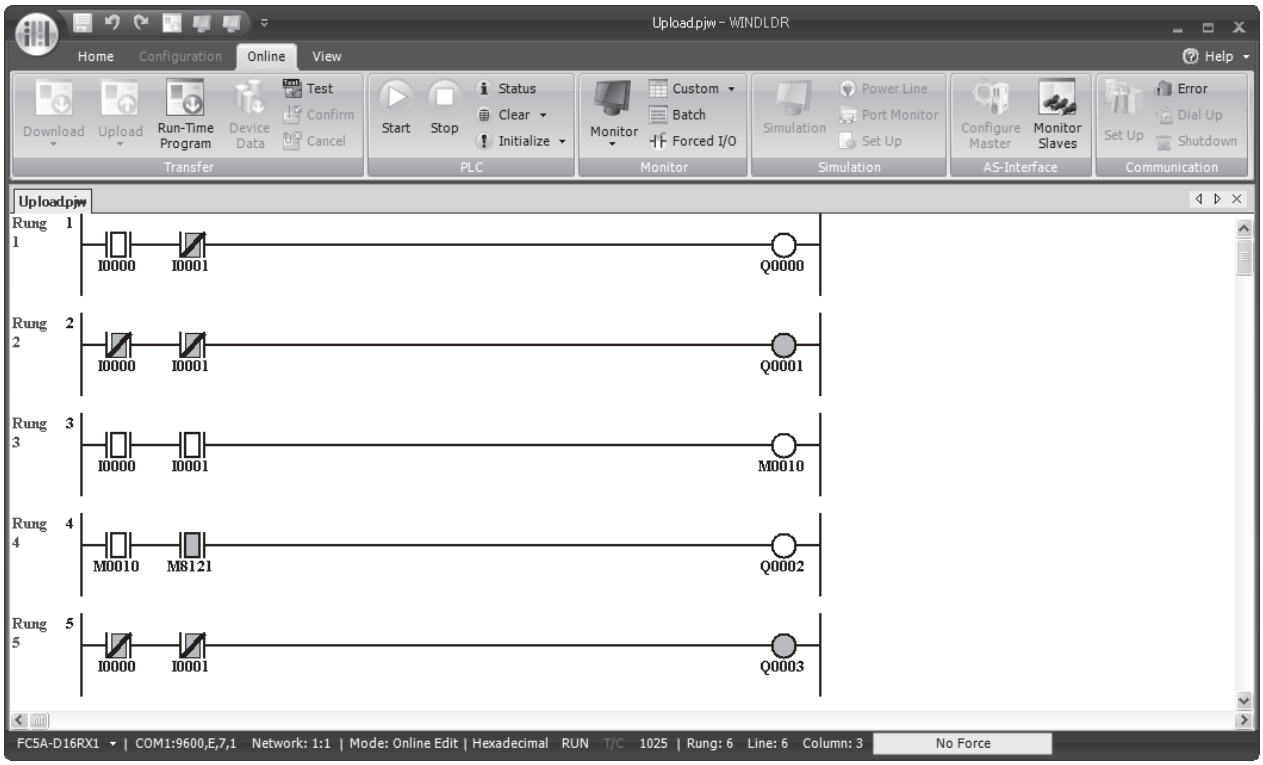
1. To execute run-time program download, select **Online** > **Run-Time Program**.

The Download Program Dialog appears.

2. Click the **OK** button to start downloading the user program to the EEPROM in the CPU module.



3. Monitor the downloaded program.



4. To quit the online edit mode, select **Online** > **Online Edit**.

Notes for Using Run-Time Program Download:

- When DISP, DGRD, AVRG, PULS, PWM, RAMP, ZRN, or PID instructions have been added or edited, the input to these instructions needs to remain off for one scan time to initialize these inputs.
- SOTU/SOTD instructions are initialized in the first scan after the run-time program download is completed.
- Function Area Settings and Expansion Data Register values cannot be changed using the online edit. To change these settings, download the user program using the ordinary program download procedure.
- When the communication buffer for TXD/RXD/ETXD/ERXD instructions still holds the instruction data, the run-time program download does not overwrite the data in the communication buffer immediately. After the communication has been completed according to the existing data in the buffer, the new data for TXD/RXD/ETXD/ERXD instructions takes effect. To clear the receive buffer for the RXD instruction, turn on the special internal relay for user communication receive instruction cancel flag, such as M8022 for port 1 or M8023 for port 2. See the example on page 5-57.
- If communication is interrupted during run-time program download, disparity between user programs in the RAM and ROM occurs. If this is the case, quit the online edit and download the user program to the CPU module using the ordinary program download procedure.

Test Program Download

Caution

- The test program download may cause unexpected operation of the MicroSmart. Before starting the test program download, make sure of safety after understanding the function correctly.
- If many changes are made to a user program, the possibility of unexpected operation increases. Keep changes to a minimum in one modification and download the user program to make sure of safety.
- If a user program syntax error or user program writing error occurs during the test program download, the CPU module is stopped and all outputs are turned off, which may cause hazards depending on the application.
- Before quitting the test program download, confirm or cancel the test program to select whether to store the modified user program to the ROM or discard the changes. Before executing the confirming procedure, the ROM stores the original user program. If the CPU module is shut down before confirming, the modified user program is lost.
- When cancelling the test program after making changes to the user program, only the original user program is restored and device values are not restored.
- While executing the test program download, do not shut down the CPU module or disconnect the communication cable. Otherwise, a fatal error may occur such as user program writing error, which may cause hazards depending on the application.
- When executing the test program download, output statuses are maintained. When an OUT/OUTN instruction is deleted or an output device address has been changed, the output status is maintained after executing the test program download. This may cause hazards depending on the application.
- When executing the Cancel Test Program, the original user program in the ROM is restored, but device values are maintained and are not restored.

The test program download replaces the user program in the RAM only and does not overwrite the ROM immediately. When test program download is completed, the modified program is executed while the original user program still remains in the ROM. Before quitting the test program download, you are asked whether to store the modified user program to the ROM or discard the modified program.

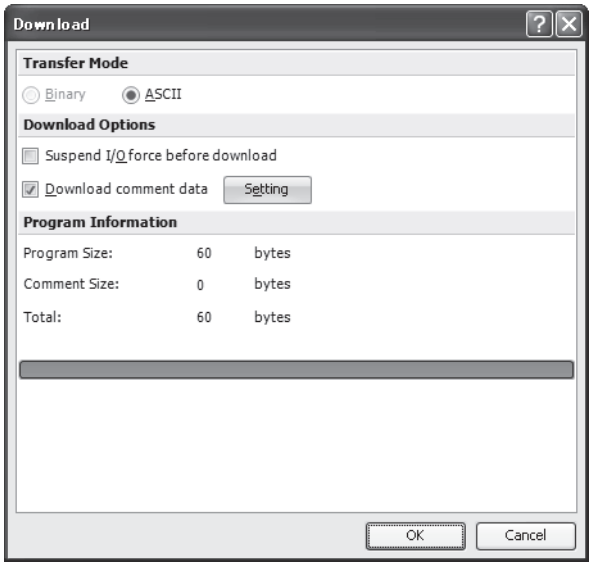
When test program download is completed, outputs, internal relays, shift registers, timer/counter current values, and data registers maintain the previous statuses. Timer/counter preset values are replaced by the new values.

Programming WindLDR

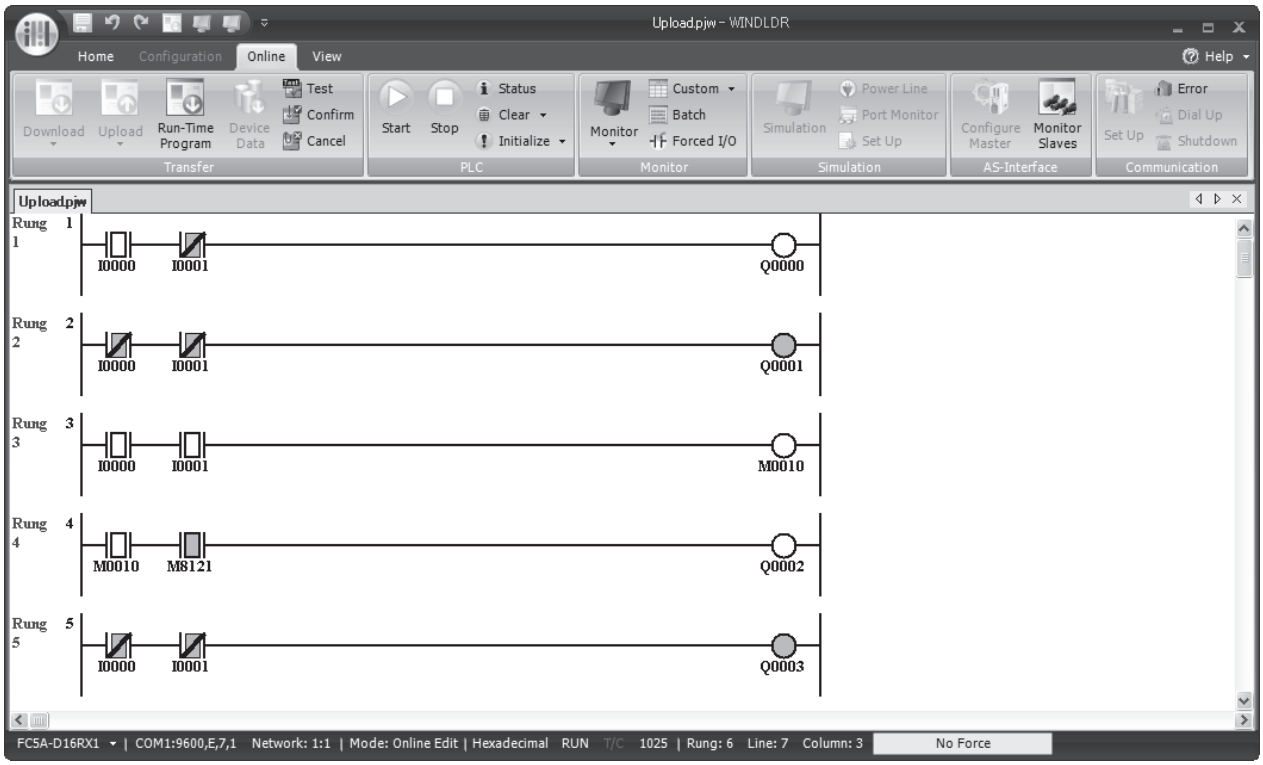
1. To execute test program download, select **Online** > **Test**.

The Download Program Dialog appears.

2. Click the **OK** button to start downloading the user program to the RAM in the CPU module.



3. Monitor the downloaded program.



Before quitting the test program download, you have to store the modified user program to the ROM or discard the modified program.

4-1. To store the downloaded program to the ROM, select **Online** > **Confirm**.
When a confirmation box appears, click **Yes** to store the downloaded program to the ROM.

The modified program is stored from the RAM to the ROM and can still be monitored.

4-2. To discard the downloaded program, select **Online** > **Cancel**.
When a confirmation box appears, click **Yes** to discard the downloaded program

The original user program stored in the ROM is restored and loaded to the RAM.

Note: If an output status is changed because of the test program download, the output status is maintained after discarding the downloaded program. In the above example, output Q3 is turned on after executing the test program download, and remains on after discarding the downloaded program. This may cause hazards depending on the application.

5. To quit the online edit mode, select **Online** > **Monitor** > **Online Edit**.

Note: To quite the online edit mode after executing the test program download, execute either Confirm, Cancel, or Run-Time Program Download, otherwise the online edit mode cannot be quit.

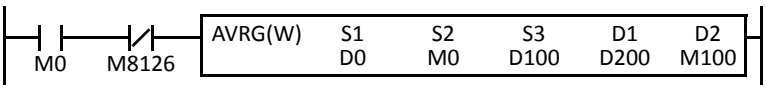
Notes for Using Test Program Download:

- Immediately when test program download is complete, the new user program is executed.
- When executing the Confirm Test Program, it takes a maximum of 60 seconds to store the downloaded program to the ROM. In this period, the scan time is extended by about 10 to 130 ms per scan.
- When the Download Test Program (to RAM) or Cancel Test Program is completed, special internal relay M8126 turns on for one scan time.
- When DISP, DGRD, AVRG, PULS, PWM, RAMP, ZRN, or PID instructions have been added or edited, the input to these instructions needs to remain off for one scan time to initialize these inputs.
- SOTU/SOTD instructions are initialized in the first scan after the Download Test Program (to RAM) or Cancel Test Program is completed.
- Function Area Settings and Expansion Data Register values cannot be changed using the online edit. To change these settings, download the user program using the ordinary program download procedure.
- When the communication buffer for TXD/RXD/ETXD/ERXD instructions still holds the instruction data, the Download Test Program (to RAM) or Cancel Test Program operation does not overwrite the data in the communication buffer immediately. After the communication has been completed according to the existing data in the buffer, the new data for TXD/RXD/ETXD/ERXD instructions takes effect. To clear the receive buffer for the RXD instruction, turn on the special internal relay for user communication receive instruction cancel flag, such as M8022 for port 1 or M8023 for port 2. See the example on page 5-57.
- If communication is interrupted during test program download, disparity between user programs in the RAM and ROM occurs. If this is the case, quit the online edit and download the user program to the CPU module using the ordinary program download procedure.

M8126 Run-Time Program Download Completion (ON for 1 scan)

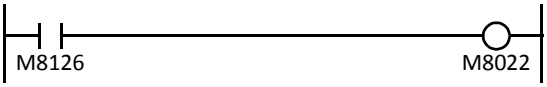
After the run-time program download has been completed, special internal relay M8126 turns on for one scan time when the CPU starts to run. During the test program download, M8126 also turns on for one scan time when the Download Test Program (to RAM) or Cancel Test Program is completed. This special internal relay is useful for initializing instructions.

Example: Initialize the AVRG instruction after Run-Time Program Download



Even if M0 is on, the AVRG instruction is initialized when the run-time program download is completed.

Example: Cancel all RXD instructions after Run-Time Program Download



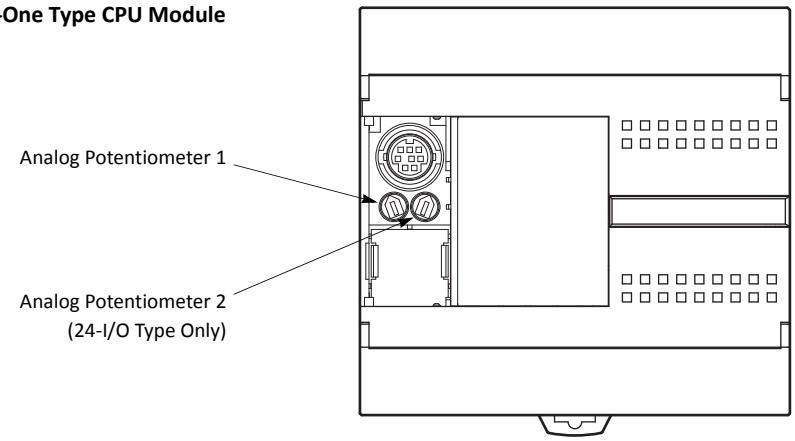
When the run-time program download is completed, special internal relay M8022 (user communication receive instruction cancel flag for port 1) is turned on to cancel all RXD1 instructions.

Analog Potentiometers

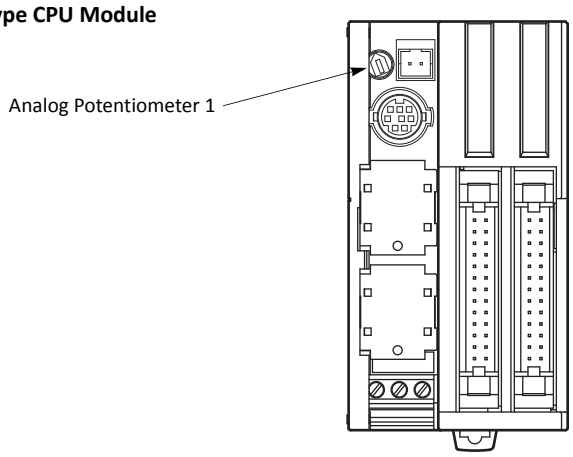
The all-in-one 10- and 16-I/O type CPU modules and every slim type CPU module have one analog potentiometer. Only the 24-I/O type CPU module has two analog potentiometers. The values (0 through 255) set with analog potentiometers 1 and 2 are stored to data registers D8057 and D8058, respectively, and updated in every scan.

The analog potentiometer can be used to change the preset value for a timer or counter.

All-in-One Type CPU Module



Slim Type CPU Module

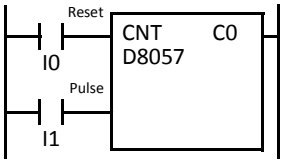


Special Data Registers for Analog Potentiometers

CPU Module	Analog Potentiometer 1	Analog Potentiometer 2
FC5A-C24R2 and FC5A-C24R2C	D8057	D8058
Other CPU Modules	D8057	—

Example: Changing Counter Preset Value Using Analog Potentiometer

This example demonstrates a program to change a counter preset value using analog potentiometer 1.



Analog potentiometer 1 value is stored to data register D8057, which is used as a preset value for counter C0.

The preset value is changed between 0 and 255 using the potentiometer.

Analog Voltage Input

Every slim type CPU module has an analog voltage input connector. When an analog voltage of 0 through 10V DC is applied to the analog voltage input connector, the signal is converted to a digital value of 0 through 255 and stored to special data register D8058. The data is updated in every scan.

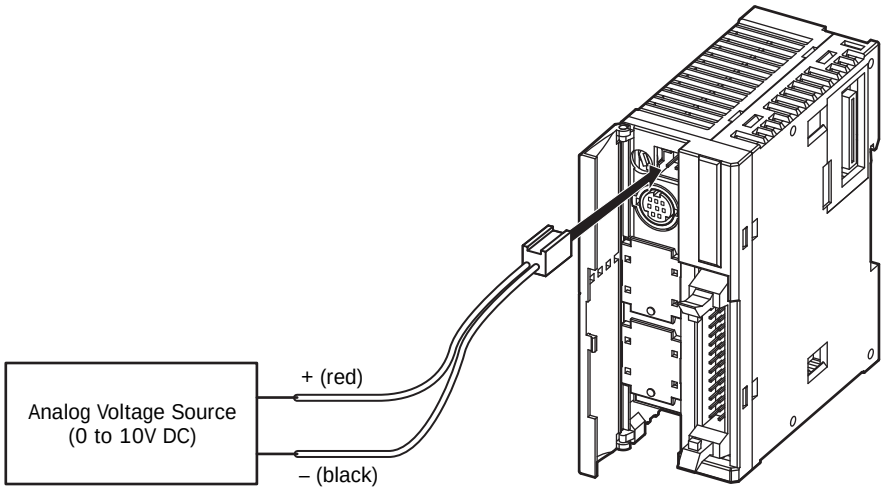
Special Data Register for Analog Voltage Input

CPU Module	Analog Voltage Input Data
Slim Type CPU Modules	D8058

To connect an external analog source, use the attached cable.

The cable is also available optionally.

Cable Name	Type No.
Analog Voltage Input Cable (1m/3.28 ft. long)	FC4A-PMAC2P (package quantity 2)



Caution

- Do not apply a voltage exceeding 10V DC to the analog voltage input, otherwise the CPU module may be damaged.

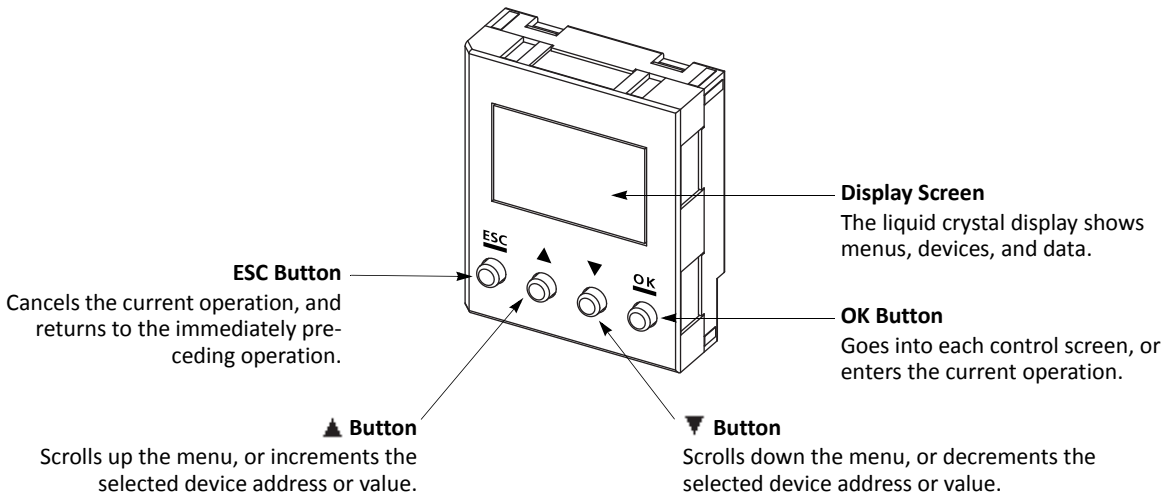
HMI Module

This section describes the functions and operation of the optional HMI module (FC4A-PH1). The HMI module can be installed on any all-in-one type CPU module, and also on the HMI base module mounted next to any slim type CPU module. The HMI module makes it possible to manipulate the RAM data in the CPU module without using the Online menu options in WindLDR. For details about the specifications of the HMI module, see page 2-80.

HMI module functions include:

- Displaying timer/counter current values and changing timer/counter preset values
- Displaying and changing data register values
- Setting and resetting bit device statuses, such as inputs, outputs, internal relays, and shift register bits
- Displaying and clearing error data
- Starting and stopping the PLC
- Displaying and changing calendar/clock data (only when using the clock cartridge)
- Confirming changed timer/counter preset values

Parts Description



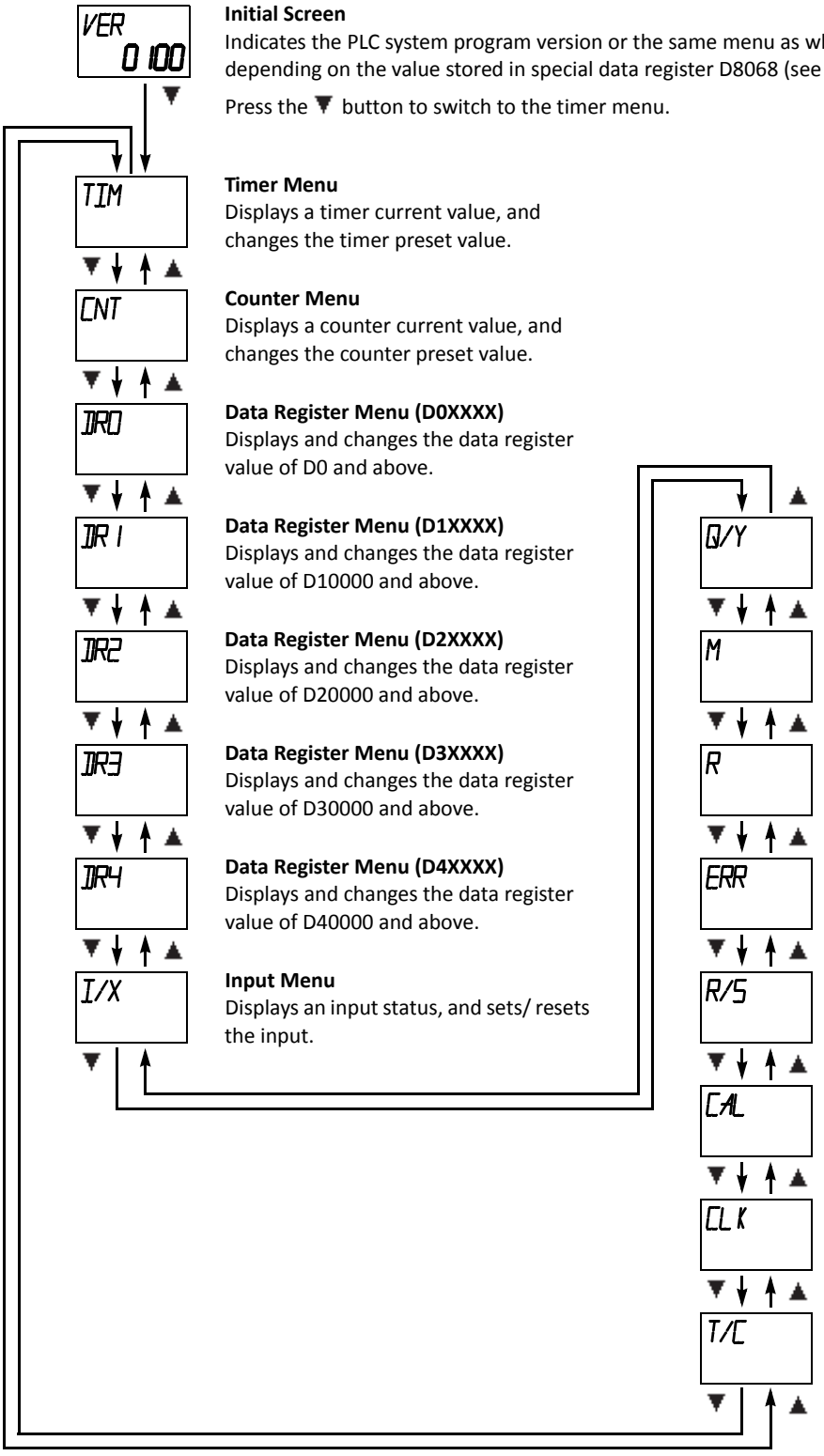
Caution

- Power up the MicroSmart CPU module after installing the HMI module. If the HMI module is installed or removed while the MicroSmart is powered up, the HMI module may fail to operate correctly.
- If an invalid device or a value over 65535 is entered, the display screen flashes to signal an error. When an error screen displays, press the **ESC** button and repeat the correct key operation.

Key Operation for Scrolling Menus after Power-up

The chart below shows the sequence of scrolling menus using the ▲ and ▼ buttons on the HMI module after power-up.

While a menu screen is shown, press the **OK** button to enter into each control screen where device addresses and values are selected. For details of each operation, see the following pages.



Initial Screen
Indicates the PLC system program version or the same menu as when the PLC was powered down, depending on the value stored in special data register D8068 (see the next page).

Press the ▼ button to switch to the timer menu.

Timer Menu
Displays a timer current value, and changes the timer preset value.

Counter Menu
Displays a counter current value, and changes the counter preset value.

Data Register Menu (D0XXXX)
Displays and changes the data register value of D0 and above.

Data Register Menu (D1XXXX)
Displays and changes the data register value of D10000 and above.

Data Register Menu (D2XXXX)
Displays and changes the data register value of D20000 and above.

Data Register Menu (D3XXXX)
Displays and changes the data register value of D30000 and above.

Data Register Menu (D4XXXX)
Displays and changes the data register value of D40000 and above.

Input Menu
Displays an input status, and sets/ resets the input.

Output Menu
Displays an output status, and sets/ resets the output.

Internal Relay Menu
Displays an internal relay status, and sets or resets the internal relay.

Shift Register Menu
Displays a shift register bit status, and sets/resets the shift register bit.

Error Menu
Displays/clears general error codes, and displays user program execution error codes.

Run/Stop Menu
Displays the run/stop status of the PLC, and starts or stops the PLC.

Calendar Menu
Displays and changes the calendar data.

Clock Menu
Displays and changes the clock data.

Timer/Counter Changed Preset Value Menu
Confirms or clears changed timer/counter preset values.
(The changed preset values in the MicroSmart CPU module RAM can be written to EEPROM.)

Special Internal Relays for HMI Module

Two special internal relays are provided protect the HMI operation.

Internal Relay	Name	Description
M8011	HMI Write Prohibit Flag	When M8011 is turned on, the HMI module is disabled from writing data to prevent unauthorized modifications, such as direct set/reset, changing timer/counter preset values, and entering data into data registers.
M8012	HMI Operation Prohibit Flag	When M8012 is turned on, the HMI module is disabled from all operations, reducing the scan time. To turn off M8012, power down and up the CPU, or use the Point Write on WindLDR.

Selection of HMI Module Initial Screen

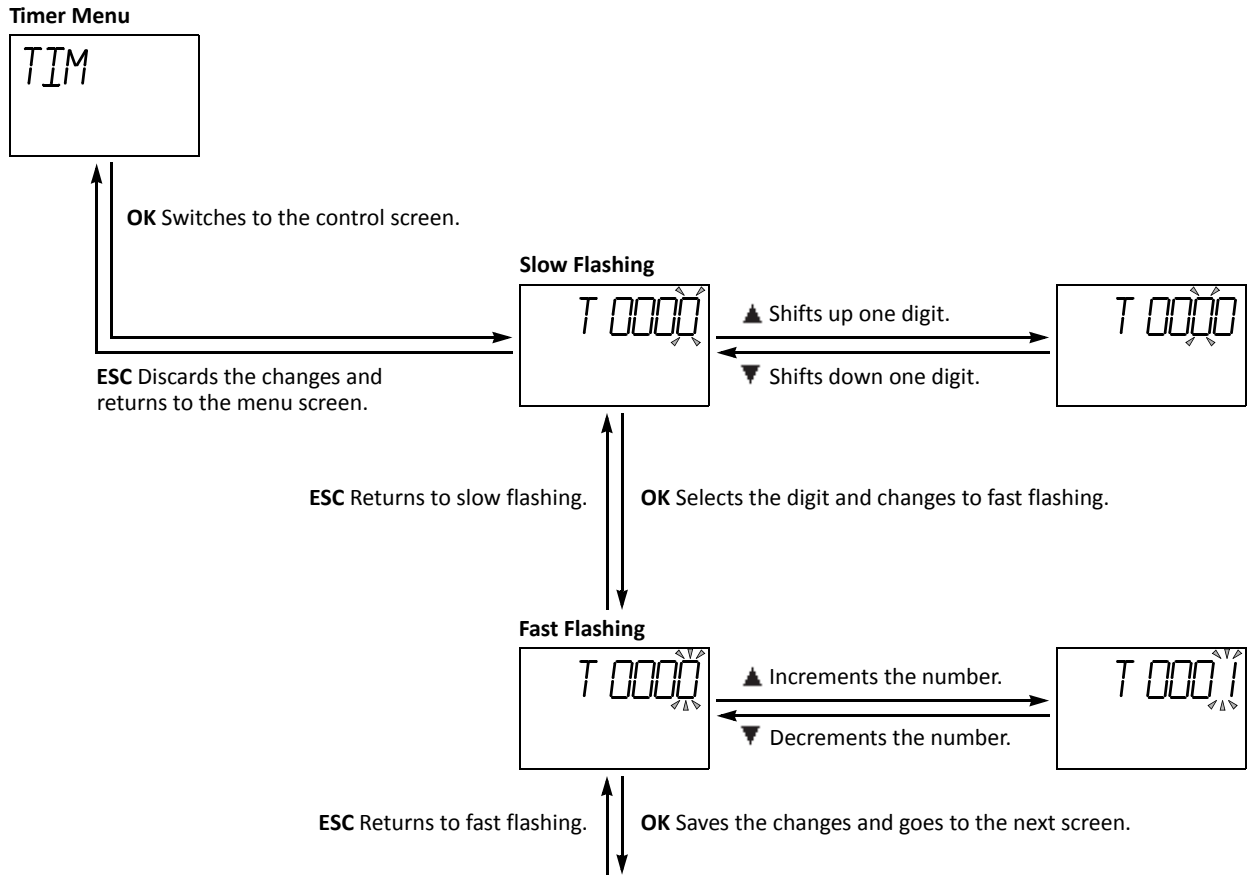
D8068 can be used to select the initial screen display of the HMI module when the CPU module is powered up.

Data Register	Value	Description
D8068	0, 2 through 65535	Mode 1: Indicates the PLC program version each time the PLC is powered up.
	1	Mode 2: Indicates the same menu as when the PLC was shut down.

When a keep data error occurs, mode 1 is enabled regardless of the value stored in data register D8068.

Key Operation for Selecting device address

When the **OK** button is pressed while a menu screen is shown, the screen switches to the control screen of the menu. For example, while the timer menu is on the display, pressing the **OK** button switches the screen to the timer control screen, where device addresses and values are selected. For operation examples, see the following pages.



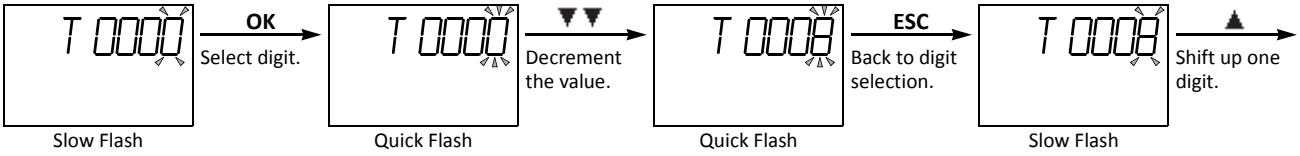
Displaying Timer/Counter Current Values and Changing Timer/Counter Preset Values

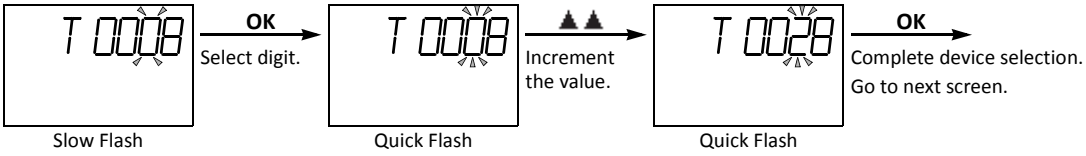
This section describes the procedure for displaying a timer current value and for changing the timer preset value for an example. The same procedure applies to counter current values and preset values.

Example: Change timer T28 preset value 820 to 900

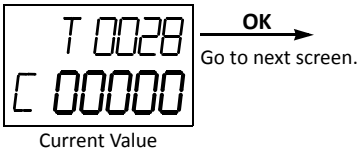
1. Select the Timer menu.

2. Select the device address.

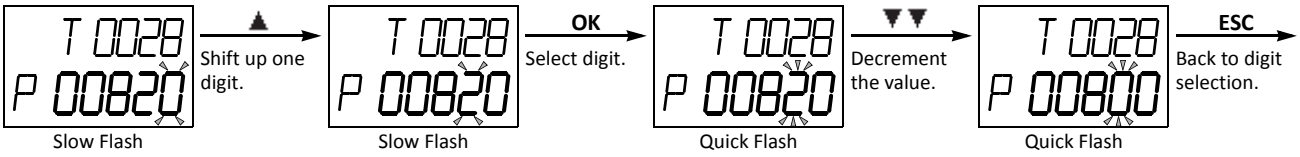


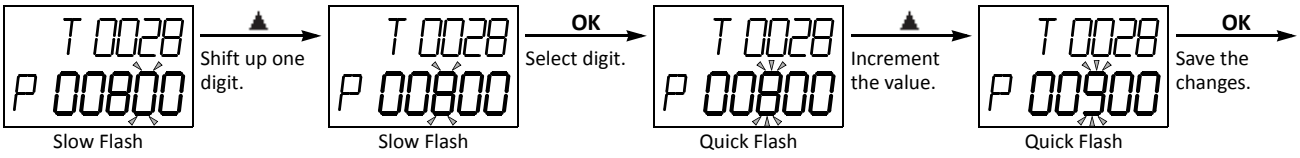


3. The current value of the selected timer number is displayed.

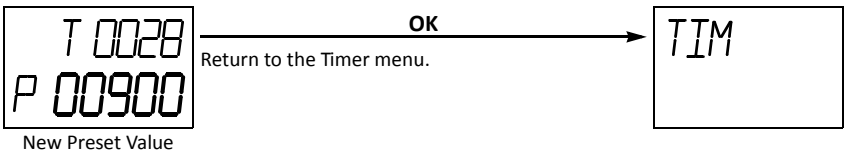


4. The preset value of the selected timer number is displayed. Change the preset value to 900 as described below.





5. The changed preset value is displayed without flashing.

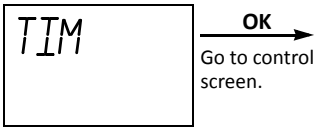


Note: The changed timer/counter preset values are stored in the MicroSmart CPU module RAM and backed up for 30 days by a lithium backup battery. If required, the changed preset values can be written from the MicroSmart CPU module RAM to the ROM using the Timer/Counter Changed Preset Value Confirm menu described on page 5-65. For the data movement in the CPU module, see page 7-18.

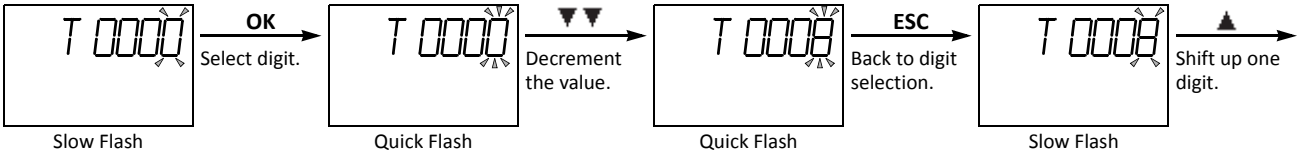
Example: When timer T28 preset value is designated using a data register

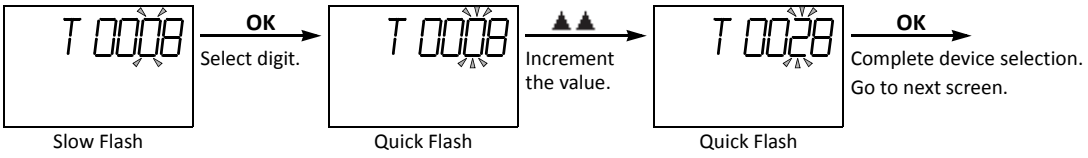
Note: Data registers designated as timer/counter preset values are displayed only for all-in-one CPU modules.

1. Select the Timer menu.

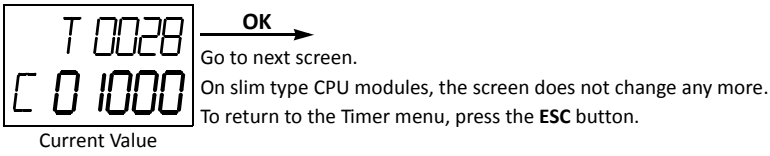


2. Select the device address.

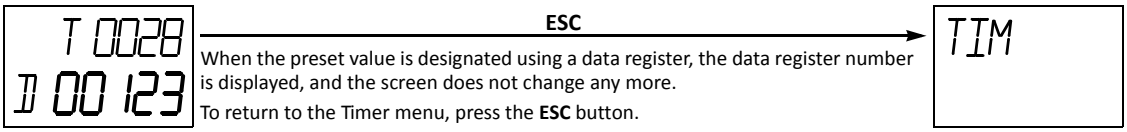




3. The current value of the selected timer number is displayed.



4. The data register number designated as a preset value is displayed.



Confirming/Clearing Changed Timer/Counter Preset Values

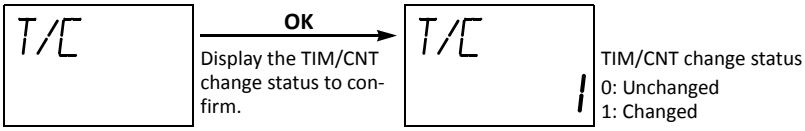
This section describes the procedure for writing changed timer/counter preset values from the MicroSmart CPU module RAM to the EEPROM. This operation writes the changed preset values of both timers and counters at once.

The changed timer/counter preset values are stored in the MicroSmart CPU module RAM and backed up for 30 days by a lithium backup battery. If required, the changed preset values can be written to the MicroSmart CPU module ROM as described below. For the data movement in the CPU module, see page 7-18.

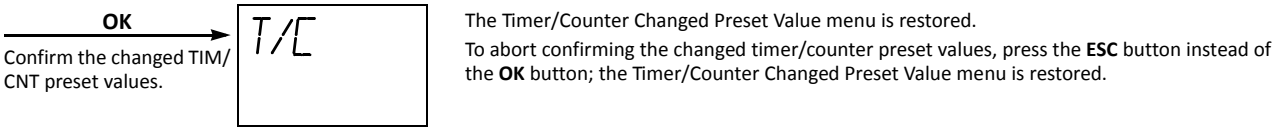
A new function to clear changed timer/counter preset values is available on the all-in-one type CPU modules with system program version 110 or higher and the slim type CPU modules with system program version 101 or higher.

Confirming Changed Timer/Counter Preset Values

1. Select the Timer/Counter Changed Preset Value Confirm menu.

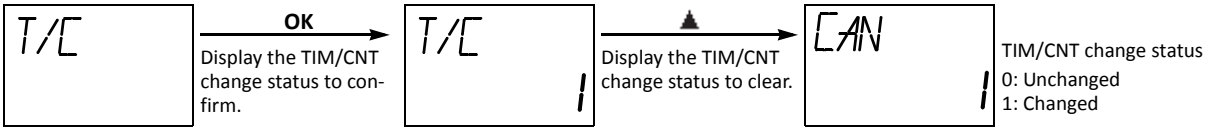


2. Confirm the changed timer/counter preset values, and write the changes from the RAM to the ROM.

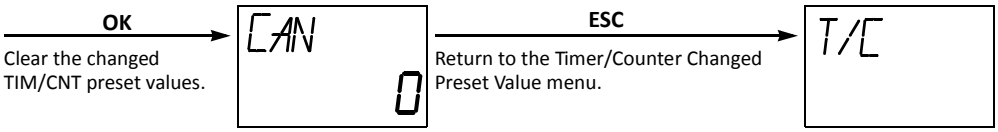


Clearing Changed Timer/Counter Preset Values

1. Select the Timer/Counter Changed Preset Value Cancel menu.



2. Clear the changed timer/counter preset values in the RAM.



Note: To abort canceling the changed timer/counter preset values, press the **ESC** or ▲ button instead of the **OK** button; the Timer/Counter Changed Preset Value menu is restored.

Displaying and Changing Data Register Values

This section describes the procedure for displaying and changing the data register value.

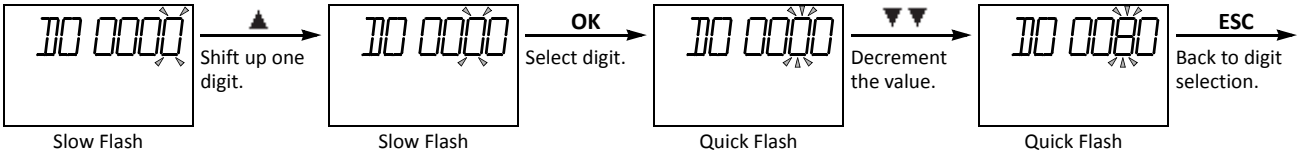
Data register menus DR0, DR1, DR2, DR3, and DR4 determine the 10,000's place of the data register number to display and change values.

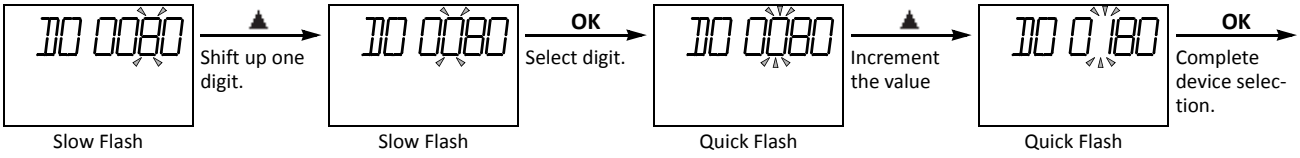
Note: When "Enable D10000 to D49999" has been selected in the Function Area Settings, and data register menu DR1, DR2, DR3, or DR4 is selected, then the data register value can be displayed and changed.

Example: Change data register D180 value to 1300

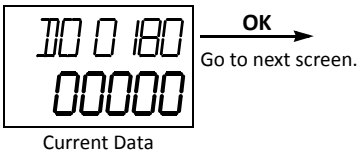
1. Select the Data Register menu DR0.

2. Select the device address.

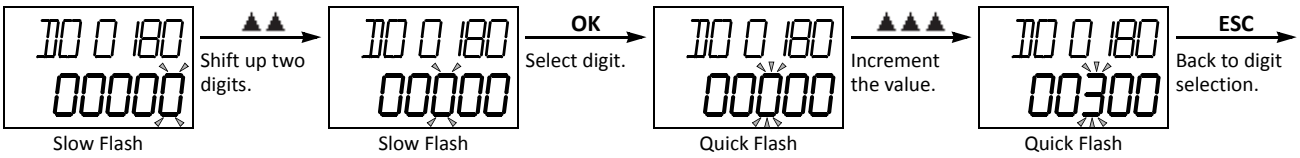


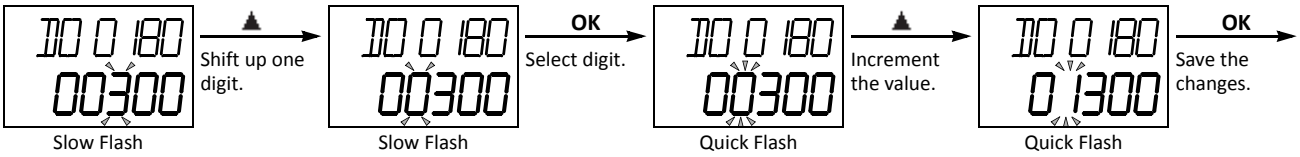


3. The data of the selected data register number is displayed.

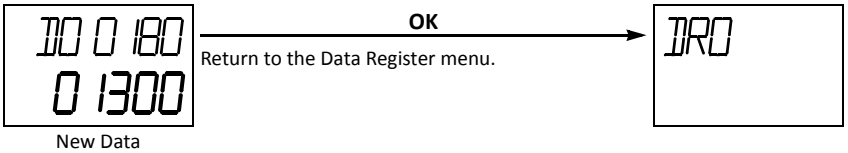


4. Change the data to 1300 as described below.





5. The changed data is displayed without flashing.



Setting and Resetting Bit Device Status

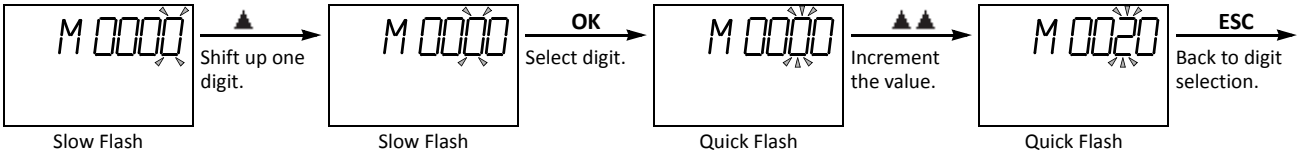
Bit device statuses, such as inputs, outputs, internal relays, and shift register bits, can be displayed, and set or reset using the MHI module.

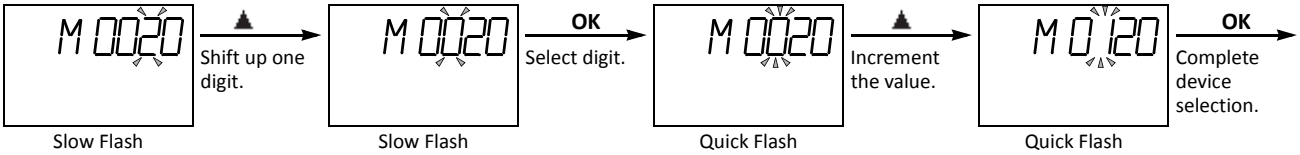
This section describes the procedure for displaying an internal relay status and for setting the internal relay for an example. The same procedure applies to inputs, outputs, and shift register bits.

Example: Set internal relay M120

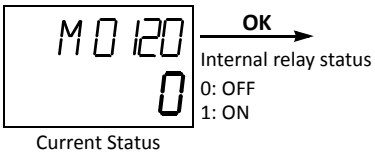
1. Select the Internal Relay menu.

2. Select the device address.

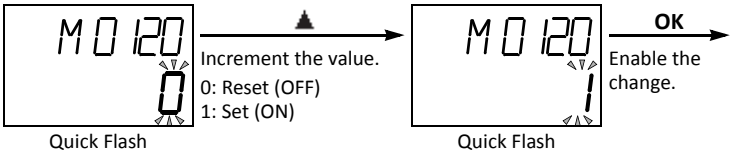




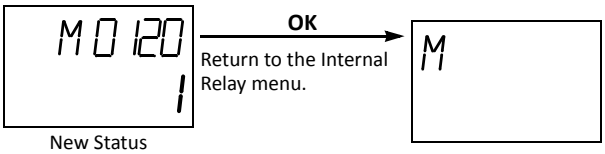
3. The status of the selected internal relay number is displayed.



4. Select 1 (set) or 0 (reset) using the ▲ or ▼ button.



5. The changed status is displayed without flashing.



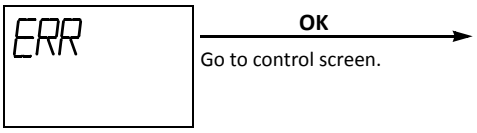
Displaying and Clearing Error Data

This section describes the procedure for displaying general error codes and for clearing the general error codes.

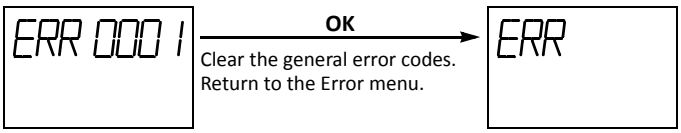
A new function to display user program execution error code is available on the all-in-one type CPU modules with system program version 110 or higher and the slim type CPU modules with system program version 101 or higher.

Displaying and Clearing General Error Codes

1. Select the Error menu.



2. General error codes are displayed. Clear the general error codes.

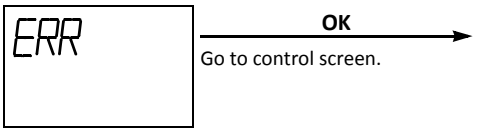


To abort clearing the general error codes, press the **ESC** button instead of the **OK** button; the Error menu is restored.

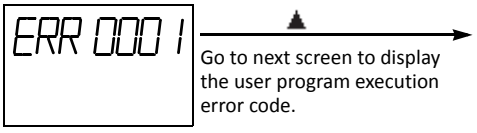
Note: For details about general error codes, see page 13-3 (Basic Vol.).

Displaying User Program Error Codes

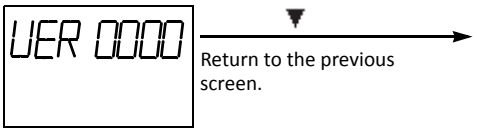
1. Select the Error menu.



2. General error codes are displayed.



3. User program execution error code is displayed.



Notes:

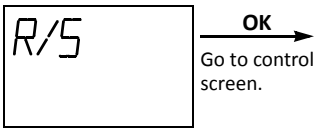
- Press the **ESC** button on any control screens to restore the Error menu.
- User program execution error codes cannot be cleared on the HMI module.
- For details about user program execution error codes, see page 13-6.

Starting and Stopping the PLC

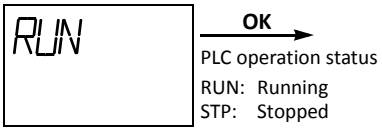
This section describes the procedure for starting and stopping the PLC operation using the HMI module.

Note: The procedure described below turns on or off start control special internal relay M8000 to start or stop the PLC operation. When a stop input is designated, the PLC cannot be started or stopped by turning start control special internal relay M8000 on or off; the procedure described below does not work. See page 4-5.

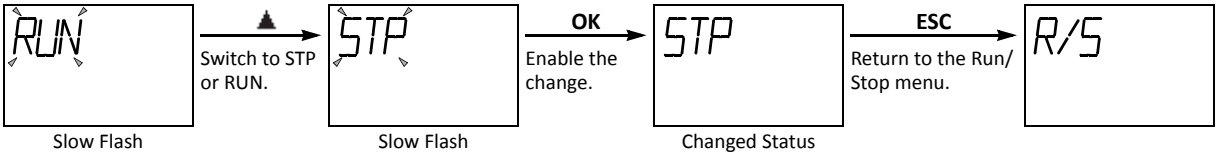
1. Select the Run/Stop menu.



2. The PLC operation status is displayed.



3. Select RUN or STP to start or stop the PLC operation, respectively, using the ▲ or ▼ button.

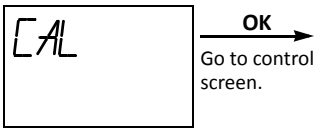


Displaying and Changing Calendar Data (only when using the clock cartridge)

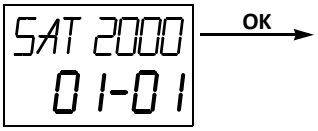
When an optional clock cartridge (FC4A-PT1) is installed in the MicroSmart CPU module, the calendar data of the clock cartridge can be displayed and changed using the HMI module as described in this section.

Example: Change calendar data from Saturday, 01/01/2000 to Wednesday, 04/04/2001

1. Select the Calendar menu.

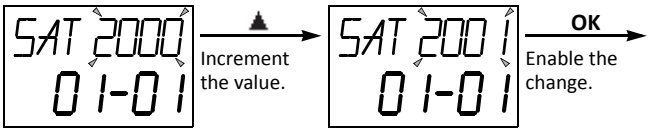


2. The calendar data is displayed.



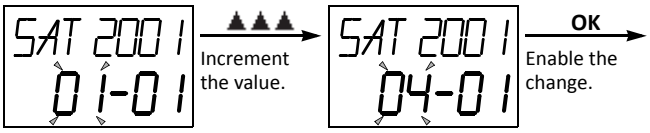
Current Data

3. Change the year data using the ▲ or ▼ button.



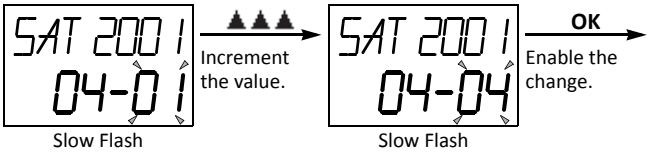
Slow Flash Slow Flash

4. Change the month data using the ▲ or ▼ button.



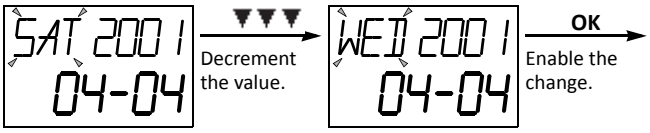
Slow Flash Slow Flash

5. Change the day data using the ▲ or ▼ button.



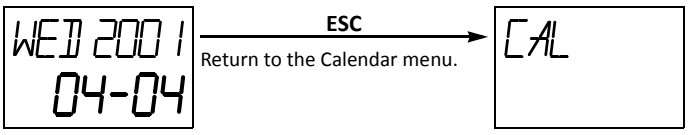
Slow Flash Slow Flash

6. Change the day of week data using the ▲ or ▼ button.



Slow Flash Slow Flash

7. The new calendar data is displayed without flashing.



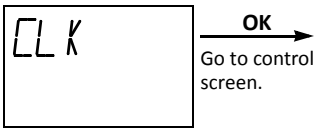
New Data

Displaying and Changing Clock Data (only when using the clock cartridge)

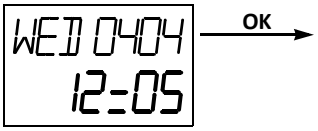
When an optional clock cartridge (FC4A-PT1) is installed in the MicroSmart CPU module, the clock data of the clock cartridge can be displayed and changed using the HMI module as described in this section.

Example: Change clock data from 12:05 to 10:10

1. Select the Clock menu.

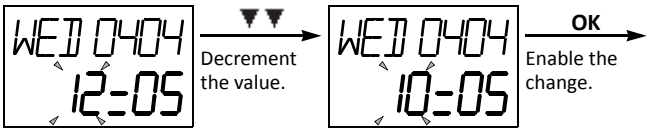


2. The clock data is displayed.



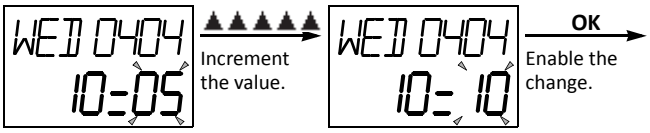
Current Data

3. Change the hour data using the ▲ or ▼ button.



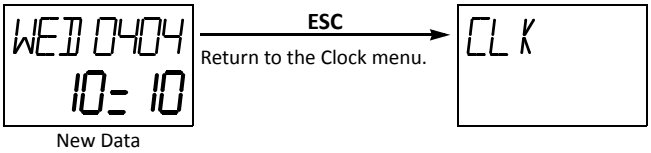
Slow Flash Slow Flash

4. Change the minute data using the ▲ or ▼ button.



Slow Flash Slow Flash

5. The new clock data is displayed without flashing.



New Data

Forced I/O

Inputs can be forced on/off regardless of the status of physical inputs, and outputs can be forced on/off regardless of the ladder logic using the forced I/O function in WindLDR. The force input function can be used in monitor or online edit mode to test the ladder logic without the need of wiring the input terminals or turning on the actual inputs. The force output function can be used to turn on/off the outputs to the external devices.

The forced I/O can be used on CPU modules with system program version 200 or higher and WindLDR 5.20 or higher.

⚠ Caution

- The forced I/O may cause unexpected operation of the MicroSmart. Make sure of safety before forcing inputs or outputs.

Devices

All the inputs and outputs of the MicroSmart can be forced on/off individually.

CPU Module Type	Device Range	
	Inputs	Outputs
FC5A-C10R2, FC5A-C10R2C, FC5A-C10R2D	I0 to I5	Q0 to Q3
FC5A-C16R2, FC5A-C16R2C, FC5A-C16R2D	I0 to I10	Q0 to Q6
FC5A-C24R2, FC5A-C24R2C	I0 to I15, I30 to I107	Q0 to Q11, Q30 to Q107
FC5A-C24R2D	I0 to I15	Q0 to Q11
FC5A-D16RK1, FC5A-D16RS1	I0 to I7, I30 to I627	Q0 to Q7, Q30 to Q627
FC5A-D32K3, FC5A-32S3	I0 to I17, I30 to I627	Q0 to Q17, Q30 to Q627
FC5A-D12K1E, FC5A-D12S1E	I0 to I7, I30 to I627	Q0 to Q3, Q30 to Q627

Forced I/O Status

Events of the MicroSmart and effects on the forced I/O settings are shown below.

Events	Forced I/O Status
When the MicroSmart starts running	The force settings are retained. The forced inputs and outputs are kept on/off even after the MicroSmart is stopped, regardless of the status of M8025 (maintain outputs while CPU is stopped).
When the MicroSmart is stopped.	
When the MicroSmart is powered up	The force settings are retained, but the force is suspended. If the battery is dead, the force settings are cleared.
When user program download is executed	The force settings are retained, and whether the force will be suspended or not can be selected in the Download Program dialog box.
When Run-Time Program Download or Download Test Program is executed	
When Confirm Test Program or Cancel Test Program is executed	The force settings are retained.
When Reset Input is turned on	The force settings are cleared.
When Clear All Devices is executed in the PLC Status dialog box of WindLDR	
When the system program is upgraded	

RUN LED

RUN LED flashes while inputs or outputs are forced on/off.

RUN LED Status	Description
Slow Flash (1-sec interval)	Inputs or outputs are forced on/off while the MicroSmart is running.
Quick Flash (100-ms interval)	Inputs or outputs are forced on/off while the MicroSmart is stopped.

Notes:

- Force function has no effect on high-speed counters, catch inputs, or interrupt inputs. The stop or reset input can be initiated using the force function, but the force settings will be cleared as soon as the reset input is turned on.
- Inputs or outputs can be forced while WindLDR is in monitor mode or in online edit mode.

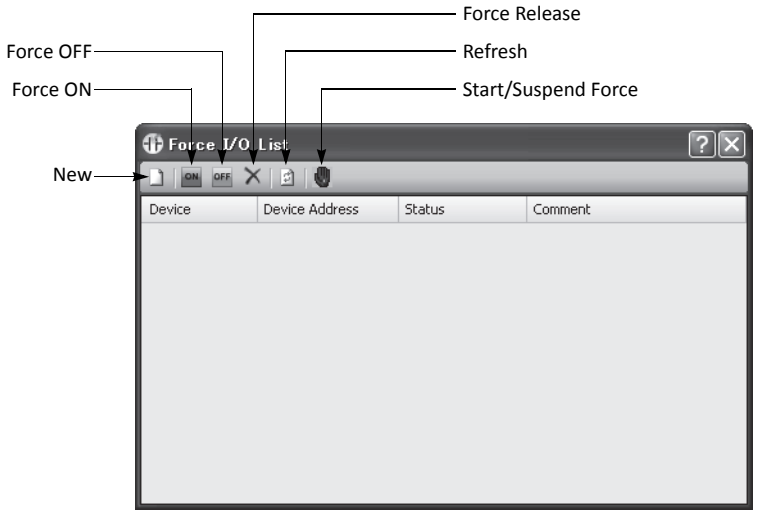
Programming WindLDR

1. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor** or **Online** > **Monitor** > **Online Edit.**

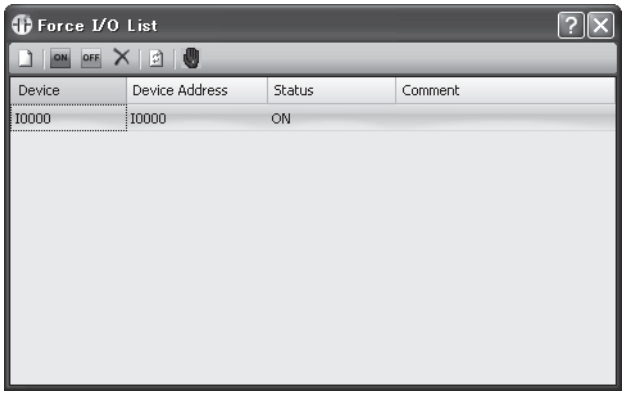
Online mode or Online Edit mode is activated.

2. From the WindLDR menu bar, select **Online** > **Forced I/O.**

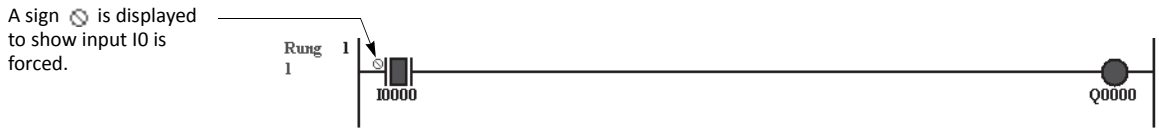
The Forced I/O List dialog box appears and shows a list of forced inputs and outputs. I/O numbers and force I/O statuses can be specified in this dialog box.



3. Click the New button and type an input or output number under Device in the list.
Click the Force On button or Force Off button to force on or off the designated input or output.



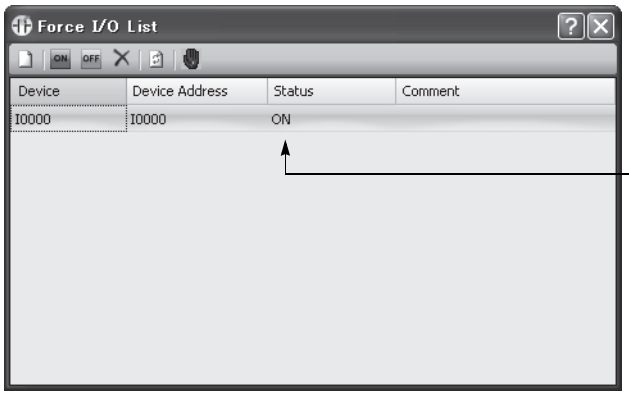
4. To start the forced I/O function, click the Start/Suspend Force button .



While the forced I/O is enabled, the RUN LED on the CPU module flashes. See page 5-72.

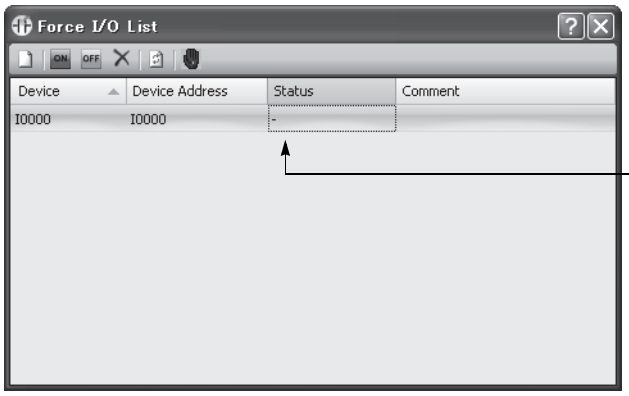
The forced I/O can be suspended temporarily by clicking the Start/Suspend Force button again.

5. To suspend the forced I/O, click the Start/Suspend Force button .



The forced inputs or outputs remain designated until the forced I/O designation is released.

6. To release the forced I/O designation, click the Force Release button .



Now input I0 works as a normal input.

Note: Make sure that all the forced inputs and outputs are released when the test using the forced I/O function is finished. Select **Delete All** from the right click menu in the Forced I/O List dialog box to release all the forced inputs and outputs at once.

6: DEVICE ADDRESSES

Introduction

This chapter describes device addresses available for the MicroSmart to program basic and advanced instructions. Special internal relays and special data registers are also described.

The MicroSmart is programmed using devices such as inputs, outputs, internal relays, timers, counters, shift registers, and data registers.

Inputs (I) are relays to receive input signals through the input terminals.
Outputs (Q) are relays to send the processed results of the user program to the output terminals.
Internal relays (M) are relays used in the CPU and cannot be outputted to the output terminals.
Special internal relays (M) are internal relays dedicated to specific functions.
Timers (T) are relays used in the user program, available in 1-sec, 100-ms, 10-ms, and 1-ms timers.
Counters (C) are relays used in the user program, available in adding counters and reversible counters.
Shift registers (R) are registers to shift the data bits according to pulse inputs.
Data registers (D) are registers used to store numerical data. Some of the data registers are dedicated to special functions.

Device Addresses

Available I/O numbers depend on the type of the MicroSmart CPU module and the combination of I/O modules. I/O modules can be used with only the 24-I/O type CPU module (except 12V DC power type) among all-in-one type CPU modules. All slim type CPU modules can be used with I/O modules to expand the I/O points. For details of I/O, internal relay, and special internal relay numbers, see page 6-3.

All-in-One Type CPU Modules

Device	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D		FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D		FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D		
	Device Address	Points	Device Address	Points	Device Address	Points	
Input (I)	I0 - I5	6	I0 - I7 I10	9	I0 - I7 I10 - I15	14	78 total (except 12V DC power type)
Expansion Input (I)	—	—	—	—	I30 - I107	64	
Output (Q)	Q0 - Q3	4	Q0 - Q6	7	Q0 - Q7 Q10 - Q11	10	74 total (except 12V DC power type)
Expansion Output (Q)	—	—	—	—	Q30 - Q107	64	
Internal Relay (M)	M0 - M2557	2048	M0 - M2557	2048	M0 - M2557	2048	
Special Internal Relay (M)	M8000 - M8157	128	M8000 - M8157	128	M8000 - M8157	128	
Shift Register (R)	R0 - R127	128	R0 - R127	128	R0 - R127	128	
Timer (T)	T0 - T255	256	T0 - T255	256	T0 - T255	256	
Counter (C)	C0 - C255	256	C0 - C255	256	C0 - C255	256	
Data Register (D)	D0 - D1999	2000	D0 - D1999	2000	D0 - D1999	2000	
Special Data Register (D)	D8000 - D8199	200	D8000 - D8199	200	D8000 - D8199	200	

Notes:

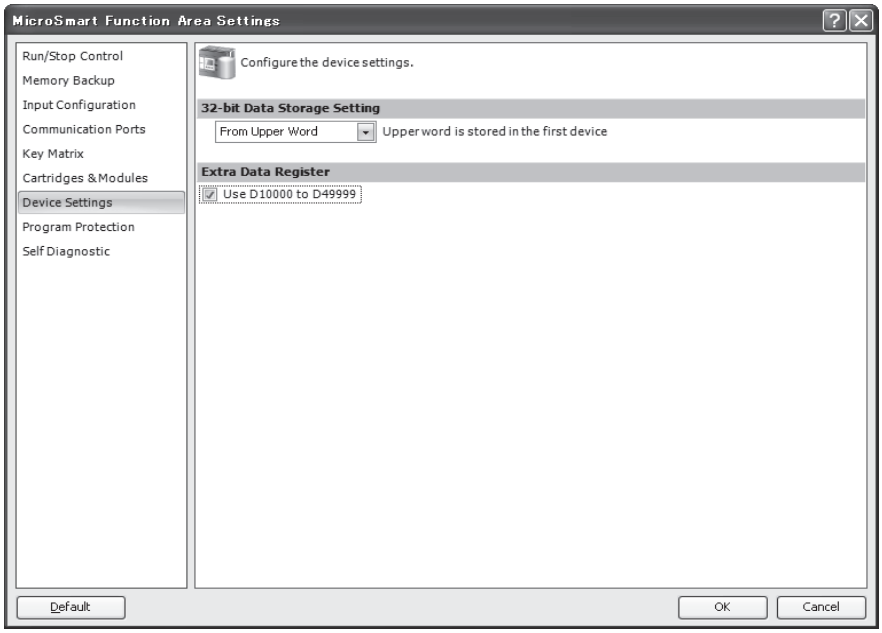
- The least significant digit of input, output, internal relay, and special internal relay device address is an octal number (0 through 7). Upper digits are decimal numbers.
- The device addresses of expansion inputs and outputs start with I30 and Q30, respectively.
- Note that input and output device addresses are not continuous between the CPU module and expansion I/O modules.
- The 24-I/O type CPU modules (FC5A-C24R2 and -C24R2C) can add a maximum of 64 I/O points, and use a maximum of 88 points of inputs and outputs in total. The 12V DC power type CPU module (FC5A-C24R2D) cannot expand I/O points.

Slim Type CPU Modules

Device	FC5A-D16RK1 FC5A-D16RS1			FC5A-D32K3 FC5A-D32S3			FC5A-D12K1E FC5A-D12S1E		
	Device Address	Points		Device Address	Points		Device Address	Points	
Input (I)	I0 - I7	8	488 total	I0 - I7 I10 - I17	16	496 total	I0 - I7	8	488 total
Expansion Input (I)	I30 - I627	480		I30 - I627	480		I30 - I627	480	
Output (Q)	Q0 - Q7	8	488 total	Q0 - Q7 Q10 - Q17	16	496 total	Q0 - Q3	4	484 total
Expansion Output (Q)	Q30 - Q627	480		Q30 - Q627	480		Q30 - Q627	480	
Internal Relay (M)	M0 - M2557	2,048		M0 - M2557	2,048		M0 - M2557	2,048	
Special Internal Relay (M)	M8000 - M8317	256		M8000 - M8317	256		M8000 - M8317	256	
Shift Register (R)	R0 - R255	256		R0 - R255	256		R0 - R255	256	
Timer (T)	T0 - T255	256		T0 - T255	256		T0 - T255	256	
Counter (C)	C0 - C255	256		C0 - C255	256		C0 - C255	256	
Data Register (D)	D0 - D1999	2,000		D0 - D1999	2,000		D0 - D1999	2,000	
Expansion Data Register (D) (Initial values can be stored in ROM)	D2000 - D7999	6,000		D2000 - D7999	6,000		D2000 - D7999	6,000	
Special Data Register (D)	D8000 - D8499	500		D8000 - D8499	500		D8000 - D8499	500	
Extra Data Register (D)	D10000 - D49999	40,000		D10000 - D49999	40,000		D10000 - D49999	40,000	

Notes:

- The least significant digit of input, output, internal relay, and special internal relay device address is an octal number (0 through 7). Upper digits are decimal numbers.
- The device addresses of expansion inputs and outputs start with I30 and Q30, respectively.
- Note that input and output device addresses are not continuous between the CPU module and expansion I/O modules.
- A maximum of 7 expansion I/O modules can be mounted on all slim type CPU modules. The maximum I/O points depend on the CPU module type as described below.
- The 16-I/O relay output type CPU module (FC5A-D16RK1 and FC5A-D16RS1) can add a maximum of 480 I/O points, and use a maximum of 496 points of inputs and outputs in total. When more than 224 I/O points are expanded, the expansion interface module is needed.
- The 32-I/O type CPU module (FC5A-D32K3 and FC5A-D32S3) can add a maximum of 480 I/O points, and use a maximum of 512 points of inputs and outputs in total. When more than 224 I/O points are expanded, the expansion interface module is needed.
- Extra data registers D10000 through D49999 can be enabled by designating in WindLDR. From the WindLDR menu bar, select **Configuration** > **Device Settings** > **Extra Data Registers**. When extra data registers are used, the online edit cannot be used.
- Extra data registers D10000 through D49999 are always available on the 12-I/O type CPU module (FC5A-D12K1E and FC5A-D12S1E).



I/O, Internal Relay, and Special Internal Relay Device Addresses

Device	Device Addresses				CPU Module
Input (I)	I0-I5				FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D
	I0-I7	I10			FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D
	I0-I7 I30-I37 I70-I77	I10-I15 I40-I47 I80-I87	 I50-I57 I90-I97	 I60-I67 I100-I107	FC5A-C24R2 FC5A-C24R2C
	I0-I7	I10-I15			FC5A-C24R2D
	I0-I7 I30-I37 I70-I77 I110-I117 I150-I157 I190-I197 I230-I237 I270-I277 I310-I317 I350-I357 I390-I397 I430-I437 I470-I477 I510-I517 I550-I557 I590-I597	 I40-I47 I80-I87 I120-I127 I160-I167 I200-I207 I240-I247 I280-I287 I320-I327 I360-I367 I400-I407 I440-I447 I480-I487 I520-I527 I560-I567 I600-I607	 I50-I57 I90-I97 I130-I137 I170-I177 I210-I217 I250-I257 I290-I297 I330-I337 I370-I377 I410-I417 I450-I457 I490-I497 I530-I537 I570-I577 I610-I617	 I60-I67 I100-I107 I140-I147 I180-I187 I220-I227 I260-I267 I300-I307 I340-I347 I380-I387 I420-I427 I460-I467 I500-I507 I540-I547 I580-I587 I620-I627	FC5A-D16RK1 FC5A-D16RS1 FC5A-D12K1E FC5A-D12S1E
	I0-I7 I30-I37 I70-I77 I110-I117 I150-I157 I190-I197 I230-I237 I270-I277 I310-I317 I350-I357 I390-I397 I430-I437 I470-I477 I510-I517 I550-I557 I590-I597	I10-I17 I40-I47 I80-I87 I120-I127 I160-I167 I200-I207 I240-I247 I280-I287 I320-I327 I360-I367 I400-I407 I440-I447 I480-I487 I520-I527 I560-I567 I600-I607	 I50-I57 I90-I97 I130-I137 I170-I177 I210-I217 I250-I257 I290-I297 I330-I337 I370-I377 I410-I417 I450-I457 I490-I497 I530-I537 I570-I577 I610-I617	 I60-I67 I100-I107 I140-I147 I180-I187 I220-I227 I260-I267 I300-I307 I340-I347 I380-I387 I420-I427 I460-I467 I500-I507 I540-I547 I580-I587 I620-I627	FC5A-D32K3 FC5A-D32S3
Output (Q)	Q0-Q3				FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D
	Q0-Q6				FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D
	Q0-Q7 Q30-Q37 Q70-Q77	Q10-Q11 Q40-Q47 Q80-Q87	 Q50-Q57 Q90-Q97	 Q60-Q67 Q100-Q107	FC5A-C24R2 FC5A-C24R2C
	Q0-Q7	Q10-Q11			FC5A-C24R2D

Device	Device Addresses				CPU Module
Output (Q)	Q0-Q7				FC5A-D16RK1 FC5A-D16RS1
	Q30-Q37	Q40-Q47	Q50-Q57	Q60-Q67	
	Q70-Q77	Q80-Q87	Q90-Q97	Q100-Q107	
	Q110-Q117	Q120-Q127	Q130-Q137	Q140-Q147	
	Q150-Q157	Q160-Q167	Q170-Q177	Q180-Q187	
	Q190-Q197	Q200-Q207	Q210-Q217	Q220-Q227	
	Q230-Q237	Q240-Q247	Q250-Q257	Q260-Q267	
	Q270-Q277	Q280-Q287	Q290-Q297	Q300-Q307	
	Q310-Q317	Q320-Q327	Q330-Q337	Q340-Q347	
	Q350-Q357	Q360-Q367	Q370-Q377	Q380-Q387	
	Q390-Q397	Q400-Q407	Q410-Q417	Q420-Q427	
	Q430-Q437	Q440-Q447	Q450-Q457	Q460-Q467	
	Q470-Q477	Q480-Q487	Q490-Q497	Q500-Q507	
	Q510-Q517	Q520-Q527	Q530-Q537	Q540-Q547	
	Q550-Q557	Q560-Q567	Q570-Q577	Q580-Q587	
	Q590-Q597	Q600-Q607	Q610-Q617	Q620-Q627	
	Q0-Q7	Q10-Q17			FC5A-D32K3 FC5A-D32S3
	Q30-Q37	Q40-Q47	Q50-Q57	Q60-Q67	
	Q70-Q77	Q80-Q87	Q90-Q97	Q100-Q107	
	Q110-Q117	Q120-Q127	Q130-Q137	Q140-Q147	
	Q150-Q157	Q160-Q167	Q170-Q177	Q180-Q187	
	Q190-Q197	Q200-Q207	Q210-Q217	Q220-Q227	
	Q230-Q237	Q240-Q247	Q250-Q257	Q260-Q267	
	Q270-Q277	Q280-Q287	Q290-Q297	Q300-Q307	
	Q310-Q317	Q320-Q327	Q330-Q337	Q340-Q347	
	Q350-Q357	Q360-Q367	Q370-Q377	Q380-Q387	
	Q390-Q397	Q400-Q407	Q410-Q417	Q420-Q427	
	Q430-Q437	Q440-Q447	Q450-Q457	Q460-Q467	
	Q470-Q477	Q480-Q487	Q490-Q497	Q500-Q507	
	Q510-Q517	Q520-Q527	Q530-Q537	Q540-Q547	
	Q550-Q557	Q560-Q567	Q570-Q577	Q580-Q587	
	Q590-Q597	Q600-Q607	Q610-Q617	Q620-Q627	
	Q0-Q3				FC5A-D12K1E FC5A-D12S1E
	Q30-Q37	Q40-Q47	Q50-Q57	Q60-Q67	
	Q70-Q77	Q80-Q87	Q90-Q97	Q100-Q107	
	Q110-Q117	Q120-Q127	Q130-Q137	Q140-Q147	
	Q150-Q157	Q160-Q167	Q170-Q177	Q180-Q187	
	Q190-Q197	Q200-Q207	Q210-Q217	Q220-Q227	
	Q230-Q237	Q240-Q247	Q250-Q257	Q260-Q267	
	Q270-Q277	Q280-Q287	Q290-Q297	Q300-Q307	
	Q310-Q317	Q320-Q327	Q330-Q337	Q340-Q347	
	Q350-Q357	Q360-Q367	Q370-Q377	Q380-Q387	
	Q390-Q397	Q400-Q407	Q410-Q417	Q420-Q427	
	Q430-Q437	Q440-Q447	Q450-Q457	Q460-Q467	
	Q470-Q477	Q480-Q487	Q490-Q497	Q500-Q507	
	Q510-Q517	Q520-Q527	Q530-Q537	Q540-Q547	
	Q550-Q557	Q560-Q567	Q570-Q577	Q580-Q587	
	Q590-Q597	Q600-Q607	Q610-Q617	Q620-Q627	

Device	Device Addresses				CPU Module
Internal Relay (M)	M0-M7	M10-M17	M20-M27	M30-M37	All types
	M40-M47	M50-M57	M60-M67	M70-M77	
	M80-M87	M90-M97	M100-M107	M110-M117	
	M120-M127	M130-M137	M140-M147	M150-M157	
	M160-M167	M170-M177	M180-M187	M190-M197	
	M200-M207	M210-M217	M220-M227	M230-M237	
	M240-M247	M250-M257	M260-M267	M270-M277	
	M280-M287	M290-M297	M300-M307	M310-M317	
	M320-M327	M330-M337	M340-M347	M350-M357	
	M360-M367	M370-M377	M380-M387	M390-M397	
	M400-M407	M410-M417	M420-M427	M430-M437	
	M440-M447	M450-M457	M460-M467	M470-M477	
	M480-M487	M490-M497	M500-M507	M510-M517	
	M520-M527	M530-M537	M540-M547	M550-M557	
	M560-M567	M570-M577	M580-M587	M590-M597	
	M600-M607	M610-M617	M620-M627	M630-M637	
	M640-M647	M650-M657	M660-M667	M670-M677	
	M680-M687	M690-M697	M700-M707	M710-M717	
	M720-M727	M730-M737	M740-M747	M750-M757	
	M760-M767	M770-M777	M780-M787	M790-M797	
	M800-M807	M810-M817	M820-M827	M830-M837	
	M840-M847	M850-M857	M860-M867	M870-M877	
	M880-M887	M890-M897	M900-M907	M910-M917	
	M920-M927	M930-M937	M940-M947	M950-M957	
	M960-M967	M970-M977	M980-M987	M990-M997	
	M1000-M1007	M1010-M1017	M1020-M1027	M1030-M1037	
	M1040-M1047	M1050-M1057	M1060-M1067	M1070-M1077	
	M1080-M1087	M1090-M1097	M1100-M1107	M1110-M1117	
	M1120-M1127	M1130-M1137	M1140-M1147	M1150-M1157	
	M1160-M1167	M1170-M1177	M1180-M1187	M1190-M1197	
Internal Relay (M)	M1200-M1207	M1210-M1217	M1220-M1227	M1230-M1237	All types
	M1240-M1247	M1250-M1257	M1260-M1267	M1270-M1277	
	M1280-M1287	M1290-M1297	M1300-M1307	M1310-M1317	
	M1320-M1327	M1330-M1337	M1340-M1347	M1350-M1357	
	M1360-M1367	M1370-M1377	M1380-M1387	M1390-M1397	
	M1400-M1407	M1410-M1417	M1420-M1427	M1430-M1437	
	M1440-M1447	M1450-M1457	M1460-M1467	M1470-M1477	
	M1480-M1487	M1490-M1497	M1500-M1507	M1510-M1517	
	M1520-M1527	M1530-M1537	M1540-M1547	M1550-M1557	
	M1560-M1567	M1570-M1577	M1580-M1587	M1590-M1597	
	M1600-M1607	M1610-M1617	M1620-M1627	M1630-M1637	
	M1640-M1647	M1650-M1657	M1660-M1667	M1670-M1677	
	M1680-M1687	M1690-M1697	M1700-M1707	M1710-M1717	
	M1720-M1727	M1730-M1737	M1740-M1747	M1750-M1757	
	M1760-M1767	M1770-M1777	M1780-M1787	M1790-M1797	
	M1800-M1807	M1810-M1817	M1820-M1827	M1830-M1837	

Device	Device Addresses				CPU Module
Internal Relay (M)	M1840-M1847	M1850-M1857	M1860-M1867	M1870-M1877	All types
	M1880-M1887	M1890-M1897	M1900-M1907	M1910-M1917	
	M1920-M1927	M1930-M1937	M1940-M1947	M1950-M1957	
	M1960-M1967	M1970-M1977	M1980-M1987	M1990-M1997	
	M2000-M2007	M2010-M2017	M2020-M2027	M2030-M2037	
	M2040-M2047	M2050-M2057	M2060-M2067	M2070-M2077	
	M2080-M2087	M2090-M2097	M2100-M2107	M2110-M2117	
	M2120-M2127	M2130-M2137	M2140-M2147	M2150-M2157	
	M2160-M2167	M2170-M2177	M2180-M2187	M2190-M2197	
	M2200-M2207	M2210-M2217	M2220-M2227	M2230-M2237	
	M2240-M2247	M2250-M2257	M2260-M2267	M2270-M2277	
	M2280-M2287	M2290-M2297	M2300-M2307	M2310-M2317	
	M2320-M2327	M2330-M2337	M2340-M2347	M2350-M2357	
	M2360-M2367	M2370-M2377	M2380-M2387	M2390-M2397	
	M2400-M2407	M2410-M2417	M2420-M2427	M2430-M2437	
	M2440-M2447	M2450-M2457	M2460-M2467	M2470-M2477	
	M2480-M2487	M2490-M2497	M2500-M2507	M2510-M2517	
	M2520-M2527	M2530-M2537	M2540-M2547	M2550-M2557	
Special Internal Relay (M)	M8000-M8007	M8010-M8017	M8020-M8027	M8030-M8037	FC5A-C10R2/C/D FC5A-C16R2/C/D FC5A-C24R2/C/D
	M8040-M8047	M8050-M8057	M8060-M8067	M8070-M8077	
	M8080-M8087	M8090-M8097	M8100-M8107	M8110-M8117	
	M8120-M8127	M8130-M8137	M8140-M8147	M8150-M8157	
	M8000-M8007	M8010-M8017	M8020-M8027	M8030-M8037	FC5A-D16RK1 FC5A-D16RS1 FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E
	M8040-M8047	M8050-M8057	M8060-M8067	M8070-M8077	
	M8080-M8087	M8090-M8097	M8100-M8107	M8110-M8117	
	M8120-M8127	M8130-M8137	M8140-M8147	M8150-M8157	
	M8160-M8167	M8170-M8177	M8180-M8187	M8190-M8197	
	M8200-M8207	M8210-M8217	M8220-M8227	M8230-M8237	
	M8240-M8247	M8250-M8257	M8260-M8267	M8270-M8277	
	M8280-M8287	M8290-M8297	M8300-M8307	M8310-M8317	

Device Addresses for END Refresh Type Analog I/O Modules

Analog I/O Module Number	Analog Input Channel 0	Analog Input Channel 1	Analog Output	Reserved
1	D760-D765	D766-D771	D772-D777	D778, D779
2	D780-D785	D786-D791	D792-D797	D798, D799
3	D800-D805	D806-D811	D812-D817	D818, D819
4	D820-D825	D826-D831	D832-D837	D838, D839
5	D840-D845	D846-D851	D852-D857	D858, D859
6	D860-D865	D866-D871	D872-D877	D878, D879
7	D880-D885	D886-D891	D892-D897	D898, D899

Note: Each analog I/O module uses 20 data registers. When analog modules are not connected, the corresponding data registers can be used as ordinary data registers.

Device Addresses for AS-Interface Master Module 1

MicroSmart CPU Module		AS-Interface Master Module EEPROM
Device	**Device Address**	**AS-Interface Object**
AS-Interface Internal Relays	M1300-M1617	Digital input (IDI)
	M1620-M1937	Digital output (ODI)
	M1940-M1997	Status information
AS-Interface Data Registers	D1700-D1731	Analog input
	D1732-D1763	Analog output
	D1764-D1767	List of active slaves (LAS)
	D1768-D1771	List of detected slaves (LDS)
	D1772-D1775	List of peripheral fault slaves (LPF)
	D1776-D1779	List of projected slaves (LPS)
	D1780-D1811	Configuration data image A (CDI)
	D1812-D1843	Configuration data image B (CDI)
	D1844-D1875	Permanent configuration data A (PCD)
	D1876-D1907	Permanent configuration data B (PCD)
	D1908-D1923	Parameter image (PI)
	D1924-D1939	Permanent parameter (PP)
	D1940	Slave 0 ID1 code
	D1941-D1945	For ASI command description
	D1946-D1999	— Reserved —

Note: AS-Interface master module 1 uses internal relays and data registers shown above. When AS-Interface master module is not connected, these internal relays and data registers can be used as ordinary internal relays and data registers. When two AS-Interface modules are used, devices are allocated to AS-Interface master module 2 using the RUNA instruction.

Device Addresses for Data Link Master Station

Slave Station Number	Device Address		
	Transmit Data to Slave Station	Receive Data from Slave Station	Data Link Communication Error
Slave Station 1	D900-D905	D906-D911	D8069
Slave Station 2	D912-D917	D918-D923	D8070
Slave Station 3	D924-D929	D930-D935	D8071
Slave Station 4	D936-D941	D942-D947	D8072
Slave Station 5	D948-D953	D954-D959	D8073
Slave Station 6	D960-D965	D966-D971	D8074
Slave Station 7	D972-D977	D978-D983	D8075
Slave Station 8	D984-D989	D990-D995	D8076
Slave Station 9	D996-D1001	D1002-D1007	D8077
Slave Station 10	D1008-D1013	D1014-D1019	D8078
Slave Station 11	D1020-D1025	D1026-D1031	D8079
Slave Station 12	D1032-D1037	D1038-D1043	D8080
Slave Station 13	D1044-D1049	D1050-D1055	D8081
Slave Station 14	D1056-D1061	D1062-D1067	D8082
Slave Station 15	D1068-D1073	D1074-D1079	D8083
Slave Station 16	D1080-D1085	D1086-D1091	D8084
Slave Station 17	D1092-D1097	D1098-D1103	D8085
Slave Station 18	D1104-D1109	D1110-D1115	D8086
Slave Station 19	D1116-D1121	D1122-D1127	D8087
Slave Station 20	D1128-D1133	D1134-D1139	D8088
Slave Station 21	D1140-D1145	D1146-D1151	D8089
Slave Station 22	D1152-D1157	D1158-D1163	D8090
Slave Station 23	D1164-D1169	D1170-D1175	D8091
Slave Station 24	D1176-D1181	D1182-D1187	D8092
Slave Station 25	D1188-D1193	D1194-D1199	D8093
Slave Station 26	D1200-D1205	D1206-D1211	D8094
Slave Station 27	D1212-D1217	D1218-D1223	D8095
Slave Station 28	D1224-D1229	D1230-D1235	D8096
Slave Station 29	D1236-D1241	D1242-D1247	D8097
Slave Station 30	D1248-D1253	D1254-D1259	D8098
Slave Station 31	D1260-D1265	D1266-D1271	D8099

Note: When any slave stations are not connected, master station data registers which are assigned to the vacant slave stations can be used as ordinary data registers.

Device Addresses for Data Link Slave Station

Data	Device Address		
	Transmit Data to Master Station	Receive Data from Master Station	Data Link Communication Error
Slave Station Data	D900-D905	D906-D911	D8069

Note: Slave station data registers D912 through D1271 and D8070 through D8099 can be used as ordinary data registers.

Special Internal Relays

Special internal relays M8000 through M8317 are used for controlling the CPU operation and communication and for indicating the CPU statuses. All special internal relays cannot be used as destinations of advanced instructions.

Read/Write	Special Internal Relay Number
Read/Write Special Internal Relays	M8000 - M8077
Read Only Special Internal Relays	All other special internal relays

Internal relays M300 through M317 are used to read input device statuses of the IOREF (I/O refresh) instruction.

⚠ Caution

- Do not change the status of reserved special internal relays, otherwise the MicroSmart may not operate correctly.

Special Internal Relay Device Addresses

Device Address	Description	CPU Stopped	Power OFF
M8000	Start Control	Maintained	Maintained
M8001	1-sec Clock Reset	Cleared	Cleared
M8002	All Outputs OFF	Cleared	Cleared
M8003	Carry (Cy) or Borrow (Bw)	Cleared	Cleared
M8004	User Program Execution Error	Cleared	Cleared
M8005	Communication Error	Maintained	Cleared
M8006	Data Link Communication Prohibit Flag (Master Station)	Maintained	Maintained
M8007	Data Link Communication Initialize Flag (Master Station) Data Link Communication Stop Flag (Slave Station)	Cleared	Cleared
M8010	Status LED	Operating	Cleared
M8011	HMI Write Prohibit Flag	Maintained	Cleared
M8012	HMI Operation Prohibit Flag	Maintained	Cleared
M8013	Calendar/Clock Data Write/Adjust Error Flag	Operating	Cleared
M8014	Calendar/Clock Data Read Error Flag	Operating	Cleared
M8015	Calendar/Clock Data Read Prohibit Flag	Maintained	Cleared
M8016	Calendar Data Write Flag	Operating	Cleared
M8017	Clock Data Write Flag	Operating	Cleared
M8020	Calendar/Clock Data Write Flag	Operating	Cleared
M8021	Clock Data Adjust Flag	Operating	Cleared
M8022	User Communication Receive Instruction Cancel Flag (Port 1)	Cleared	Cleared
M8023	User Communication Receive Instruction Cancel Flag (Port 2)	Cleared	Cleared
M8024	BMOV/WSFT Executing Flag	Maintained	Maintained
M8025	Maintain Outputs While CPU Stopped	Maintained	Cleared
M8026	Expansion Data Register Data Writing Flag (Preset Range 1)	Operating	Maintained
M8027	Expansion Data Register Data Writing Flag (Preset Range 2)	Operating	Maintained
M8030	High-speed Counter 1 (I0-I2) Comparison Output Reset	Cleared	Cleared
M8031	High-speed Counter 1 (I0-I2) Gate Input	Maintained	Cleared
M8032	High-speed Counter 1 (I0-I2) Reset Input	Maintained	Cleared
M8033	User Communication Receive Instruction Cancel Flag (Port 3)	Cleared	Cleared
M8034	High-speed Counter 2 (I3) Comparison Output Reset	Cleared	Cleared
M8035	High-speed Counter 2 (I3) Gate Input	Maintained	Cleared
M8036	High-speed Counter 2 (I3) Reset Input	Maintained	Cleared
M8037	— Reserved —	—	—
M8040	High-speed Counter 3 (I4) Comparison Output Reset	Cleared	Cleared

Device Address	Description	CPU Stopped	Power OFF
M8041	High-speed Counter 3 (I4) Gate Input	Maintained	Cleared
M8042	High-speed Counter 3 (I4) Reset Input	Maintained	Cleared
M8043	— Reserved —	—	—
M8044	High-speed Counter 4 (I5-I7) Comparison Output Reset	Cleared	Cleared
M8045	High-speed Counter 4 (I5-I7) Gate Input	Maintained	Cleared
M8046	High-speed Counter 4 (I5-I7) Reset Input	Maintained	Cleared
M8047	— Reserved —	—	—
M8050	Modem Mode (Originate): Initialization String Start	Maintained	Maintained
M8051	Modem Mode (Originate): ATZ Start	Maintained	Maintained
M8052	Modem Mode (Originate): Dialing Start	Maintained	Maintained
M8053	Modem Mode (Disconnect): Disconnect Line Start	Maintained	Maintained
M8054	Modem Mode (General Command): AT Command Start	Maintained	Maintained
M8055	Modem Mode (Answer): Initialization String Start	Maintained	Maintained
M8056	Modem Mode (Answer): ATZ Start	Maintained	Maintained
M8057	Modem Mode AT Command Execution	Maintained	Cleared
M8060	Modem Mode (Originate): Initialization String Completion	Maintained	Cleared
M8061	Modem Mode (Originate): ATZ Completion	Maintained	Cleared
M8062	Modem Mode (Originate): Dialing Completion	Maintained	Cleared
M8063	Modem Mode (Disconnect): Disconnect Line Completion	Maintained	Cleared
M8064	Modem Mode (General Command): AT Command Completion	Maintained	Cleared
M8065	Modem Mode (Answer): Initialization String Completion	Maintained	Cleared
M8066	Modem Mode (Answer): ATZ Completion	Maintained	Cleared
M8067	Modem Mode Operational State	Maintained	Cleared
M8070	Modem Mode (Originate): Initialization String Failure	Maintained	Cleared
M8071	Modem Mode (Originate): ATZ Failure	Maintained	Cleared
M8072	Modem Mode (Originate): Dialing Failure	Maintained	Cleared
M8073	Modem Mode (Disconnect): Disconnect Line Failure	Maintained	Cleared
M8074	Modem Mode (General Command): AT Command Failure	Maintained	Cleared
M8075	Modem Mode (Answer): Initialization String Failure	Maintained	Cleared
M8076	Modem Mode (Answer): ATZ Failure	Maintained	Cleared
M8077	Modem Mode Line Connection Status	Maintained	Cleared
M8080	Data Link Slave Station 1 Communication Completion Relay (Master Station) Data Link Communication Completion Relay (Slave Station) Modbus Communication Completion Relay (Modbus Master/Slave)	Operating	Cleared
M8081	Data Link Slave Station 2 Communication Completion Relay	Operating	Cleared
M8082	Data Link Slave Station 3 Communication Completion Relay	Operating	Cleared
M8083	Data Link Slave Station 4 Communication Completion Relay	Operating	Cleared
M8084	Data Link Slave Station 5 Communication Completion Relay	Operating	Cleared
M8085	Data Link Slave Station 6 Communication Completion Relay	Operating	Cleared
M8086	Data Link Slave Station 7 Communication Completion Relay	Operating	Cleared
M8087	Data Link Slave Station 8 Communication Completion Relay	Operating	Cleared
M8090	Data Link Slave Station 9 Communication Completion Relay	Operating	Cleared
M8091	Data Link Slave Station 10 Communication Completion Relay	Operating	Cleared
M8092	Data Link Slave Station 11 Communication Completion Relay	Operating	Cleared
M8093	Data Link Slave Station 12 Communication Completion Relay	Operating	Cleared
M8094	Data Link Slave Station 13 Communication Completion Relay	Operating	Cleared
M8095	Data Link Slave Station 14 Communication Completion Relay	Operating	Cleared

Device Address	Description	CPU Stopped	Power OFF
M8096	Data Link Slave Station 15 Communication Completion Relay	Operating	Cleared
M8097	Data Link Slave Station 16 Communication Completion Relay	Operating	Cleared
M8100	Data Link Slave Station 17 Communication Completion Relay	Operating	Cleared
M8101	Data Link Slave Station 18 Communication Completion Relay	Operating	Cleared
M8102	Data Link Slave Station 19 Communication Completion Relay	Operating	Cleared
M8103	Data Link Slave Station 20 Communication Completion Relay	Operating	Cleared
M8104	Data Link Slave Station 21 Communication Completion Relay	Operating	Cleared
M8105	Data Link Slave Station 22 Communication Completion Relay	Operating	Cleared
M8106	Data Link Slave Station 23 Communication Completion Relay	Operating	Cleared
M8107	Data Link Slave Station 24 Communication Completion Relay	Operating	Cleared
M8110	Data Link Slave Station 25 Communication Completion Relay	Operating	Cleared
M8111	Data Link Slave Station 26 Communication Completion Relay	Operating	Cleared
M8112	Data Link Slave Station 27 Communication Completion Relay	Operating	Cleared
M8113	Data Link Slave Station 28 Communication Completion Relay	Operating	Cleared
M8114	Data Link Slave Station 29 Communication Completion Relay	Operating	Cleared
M8115	Data Link Slave Station 30 Communication Completion Relay	Operating	Cleared
M8116	Data Link Slave Station 31 Communication Completion Relay	Operating	Cleared
M8117	Data Link All Slave Station Communication Completion Relay	Operating	Cleared
M8120	Initialize Pulse	Cleared	Cleared
M8121	1-sec Clock	Operating	Cleared
M8122	100-ms Clock	Operating	Cleared
M8123	10-ms Clock	Operating	Cleared
M8124	Timer/Counter Preset Value Changed	Maintained	Maintained
M8125	In-operation Output	Cleared	Cleared
M8126	Run-time Program Download Completion	Cleared	Cleared
M8127	— Reserved —	—	—
M8130	High-speed Counter 1 (I0-I2) Reset Status	Maintained	Cleared
M8131	High-speed Counter 1 (I0-I2) Current Value Overflow (all-in-one CPU) High-speed Counter 1 (I0-I2) Comparison 1 ON Status (all-in-one/slim CPU)	Maintained	Cleared
M8132	High-speed Counter 1 (I0-I2) Current Value Underflow (all-in-one CPU) High-speed Counter 1 (I0-I2) Comparison 2 ON Status (slim CPU)	Maintained	Cleared
M8133	High-speed Counter 2 (I3) Comparison ON Status	Maintained	Cleared
M8134	High-speed Counter 3 (I4) Comparison ON Status	Maintained	Cleared
M8135	High-speed Counter 4 (I5-I7) Reset Status	Maintained	Cleared
M8136	High-speed Counter 4 (I5-I7) Comparison 1 ON Status (all-in-one/slim CPU)	Maintained	Cleared
M8137	High-speed Counter 4 (I5-I7) Comparison 2 ON Status (slim CPU)	Maintained	Cleared
M8140	Interrupt Input I2 Status	Cleared	Cleared
M8141	Interrupt Input I3 Status	Cleared	Cleared
M8142	Interrupt Input I4 Status	Cleared	Cleared
M8143	Interrupt Input I5 Status	Cleared	Cleared
M8144	Timer Interrupt Status	Cleared	Cleared
M8145	User Communication Receive Instruction Cancel Flag (Port 4)	Cleared	Cleared
M8146	User Communication Receive Instruction Cancel Flag (Port 5)	Cleared	Cleared
M8147	User Communication Receive Instruction Cancel Flag (Port 6)	Cleared	Cleared
M8150	Comparison Result Greater Than	Maintained	Cleared
M8151	Comparison Result Less Than	Maintained	Cleared
M8152	Comparison Result Equal To	Maintained	Cleared

Device Address	Description	CPU Stopped	Power OFF
M8153	— Reserved —	—	—
M8154	Catch Input I2 ON/OFF Status	Maintained	Cleared
M8155	Catch Input I3 ON/OFF Status	Maintained	Cleared
M8156	Catch Input I4 ON/OFF Status	Maintained	Cleared
M8157	Catch Input I5 ON/OFF Status	Maintained	Cleared
M8160	— Reserved (available on slim type CPU modules only) —	—	—
M8161	High-speed Counter 1 (I0-I2) Current Value Overflow (slim CPU)	Maintained	Cleared
M8162	High-speed Counter 1 (I0-I2) Current Value Underflow (slim CPU)	Maintained	Cleared
M8163	High-speed Counter 4 (I5-I7) Current Value Overflow (slim CPU)	Maintained	Cleared
M8164	High-speed Counter 4 (I5-I7) Current Value Underflow (slim CPU)	Maintained	Cleared
M8165-M8167	— Reserved (available on slim type CPU modules only) —	—	—
M8170	User Communication Receive Instruction Cancel Flag (Port 7)	Cleared	Cleared
M8171	User Communication Receive Instruction Cancel Flag (Client 1)	Cleared	Cleared
M8172	User Communication Receive Instruction Cancel Flag (Client 2)	Cleared	Cleared
M8173	User Communication Receive Instruction Cancel Flag (Client 3)	Cleared	Cleared
M8174-M8187	— Reserved —	—	—
M8190	IP Address Change Flag	Operating	Cleared
M8191	SNTP Calendar/Clock Data Write Flag	Operating	Cleared
M8192	Interrupt Input I2 Edge (ON: Rising, OFF: Falling)	Cleared	Cleared
M8193	Interrupt Input I3 Edge (ON: Rising, OFF: Falling)	Cleared	Cleared
M8194	Interrupt Input I4 Edge (ON: Rising, OFF: Falling)	Cleared	Cleared
M8195	Interrupt Input I5 Edge (ON: Rising, OFF: Falling)	Cleared	Cleared
M8196-M8197	— Reserved —	—	—
M8200	User Communication Receive Instruction Cancel Flag (Server 1)	Cleared	Cleared
M8201	User Communication Receive Instruction Cancel Flag (Server 2)	Cleared	Cleared
M8202	User Communication Receive Instruction Cancel Flag (Server 3)	Cleared	Cleared
M8203	User Communication Receive Instruction Cancel Flag (Server 4)	Cleared	Cleared
M8204	User Communication Receive Instruction Cancel Flag (Server 5)	Cleared	Cleared
M8205	User Communication Receive Instruction Cancel Flag (Server 6)	Cleared	Cleared
M8206	User Communication Receive Instruction Cancel Flag (Server 7)	Cleared	Cleared
M8207	User Communication Receive Instruction Cancel Flag (Server 8)	Cleared	Cleared
M8210-M8211	— Reserved —	—	—
M8212	Maintenance Communication Server 1 Status	Operating	Cleared
M8213	Maintenance Communication Server 2 Status	Operating	Cleared
M8214	Maintenance Communication Server 3 Status	Operating	Cleared
M8215	Client Connection 1 Status	Operating	Cleared
M8216	Client Connection 2 Status	Operating	Cleared
M8217	Client Connection 3 Status	Operating	Cleared
M8220	Server Connection 1 Status	Operating	Cleared
M8221	Server Connection 2 Status	Operating	Cleared
M8222	Server Connection 3 Status	Operating	Cleared
M8223	Server Connection 4 Status	Operating	Cleared
M8224	Server Connection 5 Status	Operating	Cleared
M8225	Server Connection 6 Status	Operating	Cleared
M8226	Server Connection 7 Status	Operating	Cleared

Device Address	Description	CPU Stopped	Power OFF
M8227	Server Connection 8 Status	Operating	Cleared
M8230	Client Connection 1 Disconnect Flag	Maintained	Cleared
M8231	Client Connection 2 Disconnect Flag	Maintained	Cleared
M8232	Client Connection 3 Disconnect Flag	Maintained	Cleared
M8233-M8317	— Reserved —	—	—

Note: Special internal relays M8171 through M8232 are available on FC5A-D12K1E/S1E.

M8000 Start Control

M8000 is used to control the operation of the CPU. The CPU stops operation when M8000 is turned off while the CPU is running. M8000 can be turned on or off using the WindLDR Online menu. When a stop or reset input is designated, M8000 must remain on to control the CPU operation using the stop or reset input. For the start and stop operation, see page 4-5.

M8000 maintains its status when the CPU is powered down. When the data to be maintained during power failure is broken after the CPU has been off for a period longer than the battery backup duration, the CPU restarts operation or not as selected in **Configuration** > **Run/Stop Control** > **Run/Stop Selection at Memory Backup Error**. See page 5-3.

M8001 1-sec Clock Reset

While M8001 is on, M8121 (1-sec clock) is turned off.

M8002 All Outputs OFF

When M8002 is turned on, all outputs (Q0 through Q627) go off until M8002 is turned off. Self-maintained circuits using outputs also go off and are not restored when M8002 is turned off.

M8003 Carry (Cy) and Borrow (Bw)

When a carry or borrow results from executing an addition or subtraction instruction, M8003 turns on. M8003 is also used for the bit shift and rotate instructions. See pages 5-2 and 7-1 (Advanced Vol.).

M8004 User Program Execution Error

When an error occurs while executing a user program, M8004 turns on. The cause of the user program execution error can be checked using **Online** > **Monitor** > **Monitor,** then **Online** > **Status** > **Error Status** > **Details**. See page 13-6.

M8005 Communication Error

When an error occurs during communication in the data link or Modbus communication of port 2, M8005 turns on. The M8005 status is maintained when the error is cleared and remains on until M8005 is reset using WindLDR or until the CPU is turned off. The cause of the communication error can be checked using **Online** > **Monitor** > **Monitor,** then **Online** > **Status** > **Error Status** > **Details**. See page 11-5. This flag is available for port 2 only.

M8006 Data Link Communication Prohibit Flag (Master Station)

When M8006 at the master station is turned on in the data link system, data link communication is stopped. The M8006 status is maintained when the CPU is turned off and remains on until M8006 is reset using WindLDR.

M8007 Data Link Communication Initialize Flag (Master Station)
Data Link Communication Stop Flag (Slave Station)

M8007 has a different function at the master or slave station of the data link communication system.

Master station: Data link communication initialize flag

When M8007 at the master station is turned on during operation, the link configuration is checked to initialize the data link system. When a slave station is powered up after the master station, turn M8007 on to initialize the data link system. After a data link setup is changed, M8007 must also be turned on to ensure correct communication.

Slave station: Data link communication stop flag

When a slave station does not receive communication data from the master station for 10 sec or more in the data link system, M8007 turns on. When the slave station receives correct communication data, M8007 turns off.

M8010 Status LED

When M8010 is turned on or off, the STAT LED on the CPU module turns on or off, respectively.

M8011 HMI Write Prohibit Flag

When M8011 is turned on, the HMI module is disabled from writing data to prevent unauthorized modifications, such as direct set/reset, changing timer/counter preset values, and entering data into data registers.

M8012 HMI Operation Prohibit Flag

When M8012 is turned on, the HMI module is disabled from all operations, reducing the scan time. To turn off M8012, power down and up the CPU, or use the **Monitor** > **Custom Monitor** on WindLDR.

M8013 Calendar/Clock Data Write/Adjust Error Flag

When an error occurs while calendar/clock data is written or clock data is adjusted, M8013 turns on. If calendar/clock data is written or clock data is adjusted successfully, M8013 turns off.

M8014 Calendar/Clock Data Read Error Flag

When an error occurs while calendar/clock data is read, M8014 turns on. If calendar/clock data is read successfully, M8014 turns off.

M8015 Calendar/Clock Data Read Prohibit Flag

When a clock cartridge is installed, the calendar/clock data is continuously read to the special data registers D8008 through D8014 for calendar/clock current data whether the CPU is running or stopped. When M8015 is turned on while the CPU is running, calendar/clock data reading is prohibited to reduce the scan time.

M8016 Calendar Data Write Flag

When M8016 is turned on, data in data registers D8015 through D8018 (calendar new data) are set to the clock cartridge installed on the CPU module. See page 9-7 (Advanced Vol.).

M8017 Clock Data Write Flag

When M8017 is turned on, data in data registers D8019 through D8021 (clock new data) are set to the clock cartridge installed on the CPU module. See page 9-7 (Advanced Vol.).

M8020 Calendar/Clock Data Write Flag

When M8020 is turned on, data in data registers D8015 through D8021 (calendar/clock new data) are set to the clock cartridge installed on the CPU module. See page 9-7 (Advanced Vol.).

M8021 Clock Data Adjust Flag

When M8021 is turned on, the clock is adjusted with respect to seconds. If *seconds* are between 0 and 29 for current time, adjustment for *seconds* will be set to 0 and minutes remain the same. If *seconds* are between 30 and 59 for current time, adjustment for *seconds* will be set to 0 and *minutes* are incremented one. See page 9-7 (Advanced Vol.).

M8022 User Communication Receive Instruction Cancel Flag (Port 1)

When M8022 is turned on, all RXD1 instructions ready for receiving user communication through port 1 are disabled.

M8023 User Communication Receive Instruction Cancel Flag (Port 2)

When M8023 is turned on, all RXD2 instructions ready for receiving user communication through port 2 are disabled.

M8024 BMOV/WSFT Executing Flag

While the BMOV or WSFT is executed, M8024 turns on. When completed, M8024 turns off. If the CPU is powered down while executing BMOV or WSFT, M8024 remains on when the CPU is powered up again.

M8025 Maintain Outputs While CPU Stopped

Outputs are normally turned off when the CPU is stopped. M8025 is used to maintain the output statuses when the CPU is stopped. When the CPU is stopped with M8025 turned on, the output ON/OFF statuses are maintained. When the CPU restarts, M8025 is turned off automatically.

M8026 Expansion Data Register Data Writing Flag (Preset Range 1)
M8027 Expansion Data Register Data Writing Flag (Preset Range 2)

While data write from the CPU RAM to expansion data register preset range 1 or 2 in the EEPROM is in progress, M8026 or M8027 turns on, respectively. When data write is complete, the special internal relay turns off.

M8030, M8034, M8040, M8044 High-speed Counter Comparison Output Reset

When M8030, M8034, M8040, or M8044 is turned on, the comparison output of high-speed counter 1, 2, 3, or 4 is turned off, respectively. See page 5-7 and after.

M8031, M8035, M8041, M8045 High-speed Counter Gate Input

While M8031, M8035, M8041, or M8045 is on, counting is enabled for high-speed counter 1, 2, 3, or 4, respectively. See page 5-7 and after.

M8032, M8036, M8042, M8046 High-speed Counter Reset Input

When M8032, M8036, M8042, or M8046 is turned on, the current values of high-speed counters 1 through 4 are reset to the reset values or 0, depending on the selected high-speed counter mode. See page 5-7 and after.

M8033 User Communication Receive Instruction Cancel Flag (Port 3)

When M8033 is turned on, all RXD3 instructions ready for receiving user communication through port 3 are disabled.

M8050-M8077 Special Internal Relays for Modem Mode

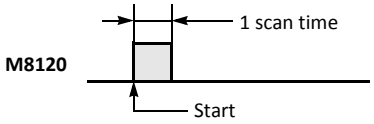
See page 5-7 (Basic Vol.).

M8080-M8117 Special Internal Relays for Data Link Communication and Modbus Communication

See pages 11-7, 12-9, and 12-14.

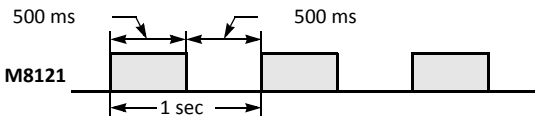
M8120 Initialize Pulse

When the CPU starts operation, M8120 turns on for a period of one scan.



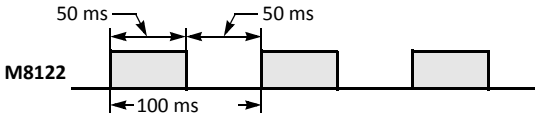
M8121 1-sec Clock

While M8001 (1-sec clock reset) is off, M8121 generates clock pulses in 1-sec increments, with a duty ratio of 1:1 (500 ms on and 500 ms off).



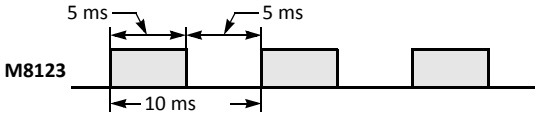
M8122 100-ms Clock

M8122 always generates clock pulses in 100-ms increments, whether M8001 is on or off, with a duty ratio of 1:1 (50 ms on and 50 ms off).



M8123 10-ms Clock

M8123 always generates clock pulses in 10-ms increments, whether M8001 is on or off, with a duty ratio of 1:1 (5 ms on and 5 ms off).



M8124 Timer/Counter Preset Value Changed

When timer or counter preset values are changed in the CPU module RAM, M8124 turns on. When a user program is downloaded to the CPU from WindLDR or when the changed timer/counter preset value is cleared, M8124 turns off.

Timer or counter preset and current values can be changed using WindLDR without transferring the entire program to the CPU again (see pages 7-9 and 7-12). When a timer or counter is designated as a destination of an advanced instruction, the timer/counter preset value is also changed.

M8125 In-operation Output

M8125 remains on while the CPU is running.

M8126 Run-Time Program Download Completion (ON for 1 scan)

M8126 turns on for one scan when the CPU starts to run after the run-time program download has been completed.

M8130-M8137 Special Internal Relays for High-speed Counter

See page 5-7 and after.

M8140, M8141, M8142, M8143 Interrupt Input Status

When interrupt inputs I2 through I5 are enabled, M8140 through M8143 are turned on, respectively. When disabled, these internal relays are turned off.

M8144 Timer Interrupt Status

When timer interrupt is enabled, M8144 is turned on. When disabled, M8144 is turned off.

M8145, M8146, M8147 User Communication Receive Instruction Cancel Flag (Port 4, Port 5, Port 6)

When M8145, M8146, or M8147 is turned on, all RXD4, RXD5, or RXD6 instructions ready for receiving user communication through port 4, port 5, or port 6 are disabled, respectively.

M8150 Comparison Result Greater Than

When the CMP= instruction is used, M8150 is turned on when the value of device designated by S1 is greater than that of device designated by S2 (S1 > S2). See page 4-2 (Advanced Vol.).

When the ICMP>= instruction is used, M8150 is turned on when the value of device designated by S2 is greater than that of device designated by S1 (S2 < S1). See page 4-6 (Advanced Vol.).

M8151 Comparison Result Equal To

When the CMP= instruction is used, M8151 is turned on when the value of device designated by S1 is equal to that of device designated by S2 (S1 = S2). See page 4-2 (Advanced Vol.).

When the ICMP>= instruction is used, M8151 is turned on when the value of device designated by S3 is greater than that of device designated by S2 (S3 > S2). See page 4-6 (Advanced Vol.).

M8152 Comparison Result Less Than

When the CMP= instruction is used, M8152 is turned on when the value of device designated by S1 is less than that of device designated by S2 (S1 < S2). See page 4-2 (Advanced Vol.).

When the ICMP>= instruction is used, M8152 is turned on when the value of device designated by S2 is less than that of device designated by S1 and greater than that of device designated by S3 (S1 > S2 > S3). See page 4-6 (Advanced Vol.).

M8154, M8155, M8156, M8157 Catch Input ON/OFF Status

When a rising or falling input edge is detected during a scan, the input statuses of catch inputs I2 through I5 at the moment are set to M8154 through M8157, respectively, without regard to the scan status. Only one edge is detected in one scan. For the catch input function, see page 5-32.

M8161-M8164 Special Internal Relays for High-speed Counter

See page 5-7 and after.

M8170 User Communication Receive Instruction Cancel Flag (Port 7)

When M8170 is turned on, all RXD7 instructions ready for receiving user communication through port 7 are disabled.

M8171 User Communication Receive over Ethernet Instruction Cancel Flag (Client Connection 1)

When M8171 is turned on, all ERXD C1 instructions ready for receiving user communication through client connection 1 are disabled.

M8172 User Communication Receive over Ethernet Instruction Cancel Flag (Client Connection 2)

When M8172 is turned on, all ERXD C2 instructions ready for receiving user communication through client connection 2 are disabled.

M8173 User Communication Receive over Ethernet Instruction Cancel Flag (Client Connection 3)

When M8173 is turned on, all ERXD C3 instructions ready for receiving user communication through client connection 3 are disabled.

M8190 IP Address Change Flag

Network settings are not changed by just changing the values in D8303 through D8323. Turn on M8190 to update the network settings according to the values stored in D8303 through D8323.

M8191 SNTP Calendar/Clock Data Write Flag

When M8191 is turned on, data in data registers D8414 to D8420 (calendar/clock data obtained from SNTP) are set to the clock cartridge installed on the CPU module. When M8191 remains on, the same action is repeated every 24 hours.

M8192-M8195 Interrupt Input I2 through I5 Edge (ON: Rising, OFF: Falling)

This flag indicates whether the interrupt input is triggered with a rising edge or falling edge.

M8200 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 1)

When M8200 is turned on, all ERXD S1 instructions ready for receiving user communication through server connection 1 are disabled.

M8201 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 2)

When M8201 is turned on, all ERXD S2 instructions ready for receiving user communication through server connection 2 are disabled.

M8202 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 3)

When M8202 is turned on, all ERXD S3 instructions ready for receiving user communication through server connection 3 are disabled.

M8203 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 4)

When M8203 is turned on, all ERXD S4 instructions ready for receiving user communication through server connection 4 are disabled.

M8204 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 5)

When M8204 is turned on, all ERXD S5 instructions ready for receiving user communication through server connection 5 are disabled.

M8205 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 6)

When M8205 is turned on, all ERXD S6 instructions ready for receiving user communication through server connection 6 are disabled.

M8206 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 7)

When M8206 is turned on, all ERXD S7 instructions ready for receiving user communication through server connection 7 are disabled.

M8207 User Communication Receive over Ethernet Instruction Cancel Flag (Server Connection 8)

When M8207 is turned on, all ERXD S8 instructions ready for receiving user communication through server connection 8 are disabled.

M8212-M8214 Maintenance Communication Server (1 through 3) Status

While the connection of the maintenance communication server is in use, the corresponding relay turns on. When the connection is not in use, the corresponding relay turns off.

M8215-M8217 Client Connection (1 through 3) Status

While the connection of the client connection is in use, the corresponding relay turns on. When the connection is not in use, the corresponding relay turns off.

M8220-M8227 Server Connection (1 through 8) Status

While the connection of the server connection is in use, the corresponding relay turns on. When the connection is not in use, the corresponding relay turns off.

M8230-M8232 Client Connection (1 through 3) Disconnect Flag

When this relay is turned on while the corresponding client connection is in use, the connection is disconnected.

Special Data Registers

Caution • Do not change the data of reserved special data registers, otherwise the MicroSmart may not operate correctly.

Special Data Register Device Addresses

Device Address	Description			Updated	See Page
D8000	System Setup ID (Quantity of Inputs)			When I/O initialized	6-24
D8001	System Setup ID (Quantity of Outputs)			When I/O initialized	6-24
D8002	CPU Module Type Information			Power-up	6-24
D8003	Memory Cartridge Information			Power-up	6-24
D8004	— Reserved —			—	—
D8005	General Error Code			When error occurred	Basoc Vol. 13-3
D8006	User Program Execution Error Code			When error occurred	13-6
D8007	Communication Mode Switching (Port 1 and 2)			—	6-25
D8008	Year	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8009	Month	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8010	Day	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8011	Day of Week	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8012	Hour	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8013	Minute	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8014	Second	(Current Data)	Read only	Every 500 ms	Advanced Vol. 9-6
D8015	Year	(New Data)	Write only	—	Advanced Vol. 9-6
D8016	Month	(New Data)	Write only	—	Advanced Vol. 9-6
D8017	Day	(New Data)	Write only	—	Advanced Vol. 9-6
D8018	Day of Week	(New Data)	Write only	—	Advanced Vol. 9-6
D8019	Hour	(New Data)	Write only	—	Advanced Vol. 9-6
D8020	Minute	(New Data)	Write only	—	Advanced Vol. 9-6
D8021	Second	(New Data)	Write only	—	Advanced Vol. 9-6
D8022	Constant Scan Time Preset Value (1 to 1,000 ms)			—	5-50
D8023	Scan Time Current Value (ms)			Every scan	5-50
D8024	Scan Time Maximum Value (ms)			At occurrence	5-50
D8025	Scan Time Minimum Value (ms)			At occurrence	5-50
D8026	Communication Mode Information (Port 1 through Port 7)			Every scan	6-25
D8027	Port 1 Communication Network Number (0 through 31)			Every scan	Advanced Vol. 21-2
D8028	Port 2 Communication Network Number (0 through 31)			Every scan	Advanced Vol. 21-2
D8029	System Program Version			Power-up	6-25
D8030	Communication Adapter Information			Power-up	6-25
D8031	Optional Cartridge Information			Power-up	6-25
D8032	Interrupt Input Jump Destination Label No. (I2)			—	5-34
D8033	Interrupt Input Jump Destination Label No. (I3)			—	5-34
D8034	Interrupt Input Jump Destination Label No. (I4)			—	5-34
D8035	Interrupt Input Jump Destination Label No. (I5)			—	5-34
D8036	Timer Interrupt Jump Destination Label No.			—	5-36
D8037	Quantity of Expansion I/O Modules			When I/O initialized	6-26
D8038-D8039	— Reserved —			—	—

Special Data Registers for Communication Ports

Device Address	Description	Updated	See Page
D8040	Data Link Slave Station Number (Port 3)	—	11-9
	Modbus Slave Number (Port 3)	—	12-14
D8041	Data Link Slave Station Number (Port 4)	—	11-9
	Modbus Slave Number (Port 4)	—	12-14
D8042	Data Link Slave Station Number (Port 5)	—	11-9
	Modbus Slave Number (Port 5)	—	12-14
D8043	Data Link Slave Station Number (Port 6)	—	11-9
	Modbus Slave Number (Port 6)	—	12-14
D8044	Data Link Slave Station Number (Port 7)	—	11-9
	Modbus Slave Number (Port 7)	—	12-14

Special Data Registers for High-speed Counters (All-in-one type CPU modules only)

D8045	High-speed Counter 1 (I0-I2) Current Value	Every scan	5-8, 5-10
D8046	High-speed Counter 1 (I0-I2) Reset Value	—	5-8, 5-10
D8047	High-speed Counter 2 (I3) Current Value	Every scan	5-8
D8048	High-speed Counter 2 (I3) Preset Value	—	5-8
D8049	High-speed Counter 3 (I4) Current Value	Every scan	5-8
D8050	High-speed Counter 3 (I4) Preset Value	—	5-8
D8051	High-speed Counter 4 (I5-I7) Current Value	Every scan	5-8
D8052	High-speed Counter 4 (I5-I7) Reset Value	—	5-8

Special Data Registers for Modbus Communication

D8053	Modbus communication error code	Every scan	12-14
D8054	Modbus communication transmission wait time	When communication initialized	12-14

Special Data Registers for Pulse Outputs

D8055	Current Pulse Frequency of PULS1 or RAMP1 (Q0)	Every scan	Advanced Vol. 13-5, 13-19
D8056	Current Pulse Frequency of PULS2 or RAMP1 (Q1)	Every scan	Advanced Vol. 13-5, 13-19
D8059	Current Pulse Frequency of PULS3 or RAMP2 (Q2)	Every scan	Advanced Vol. 13-5, 13-19

Special Data Registers for Analog Potentiometers

D8057	Analog Potentiometer 1 Value (All CPU modules)	Every scan	5-58
D8058	Analog Potentiometer 2 Value (All-in-one 24-I/O type CPU) Analog Voltage Input (Slim type CPU modules)	Every scan	5-58, 5-59

Special Data Registers for Frequency Measurement

D8060	Frequency Measurement Value I1 (All-in-one type CPU) Frequency Measurement Value I1 High Word (Slim type CPU)	Every scan	5-30
D8061	— Reserved (All-in-one type CPU) — Frequency Measurement Value I1 Low Word (Slim type CPU)	Every scan	5-30
D8062	Frequency Measurement Value I3 (All-in-one type CPU) Frequency Measurement Value I3 High Word (Slim type CPU)	Every scan	5-30

Device Address	Description	Updated	See Page
D8063	— Reserved (All-in-one type CPU) — Frequency Measurement Value I3 Low Word (Slim type CPU)	Every scan	5-30
D8064	Frequency Measurement Value I4 (All-in-one type CPU) Frequency Measurement Value I4 High Word (Slim type CPU)	Every scan	5-30
D8065	— Reserved (All-in-one type CPU) — Frequency Measurement Value I4 Low Word (Slim type CPU)	Every scan	5-30
D8066	Frequency Measurement Value I5 (All-in-one type CPU) Frequency Measurement Value I7 High Word (Slim type CPU)	Every scan	5-30
D8067	— Reserved (All-in-one type CPU) — Frequency Measurement Value I7 Low Word (Slim type CPU)	Every scan	5-30

Note: Devices for high and low words can be swapped on upgraded CPU modules with system program version 110 or higher. See page 5-47.

Special Data Register for HMI Module

D8068	HMI Module Initial Screen Selection	Power-up	5-62

Special Data Registers for Data Link Master/Slave Stations and Modbus Master Station

D8069	Slave Station 1 Communication Error (at Master Station) Slave Station Communication Error (at Slave Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8070	Slave Station 2 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8071	Slave Station 3 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8072	Slave Station 4 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8073	Slave Station 5 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8074	Slave Station 6 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8075	Slave Station 7 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8076	Slave Station 8 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8077	Slave Station 9 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8078	Slave Station 10 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8079	Slave Station 11 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8080	Slave Station 12 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8081	Slave Station 13 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8082	Slave Station 14 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8083	Slave Station 15 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8084	Slave Station 16 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14

Device Address	Description	Updated	See Page
D8085	Slave Station 17 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8086	Slave Station 18 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8087	Slave Station 19 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8088	Slave Station 20 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8089	Slave Station 21 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8090	Slave Station 22 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8091	Slave Station 23 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8092	Slave Station 24 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8093	Slave Station 25 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8094	Slave Station 26 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8095	Slave Station 27 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8096	Slave Station 28 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8097	Slave Station 29 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8098	Slave Station 30 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14
D8099	Slave Station 31 Communication Error (at Master Station) Error station number and error code (at Modbus Master)	When error occurred	11-4, 12-14

Special Data Registers for Communication Ports (D8200-D8209: Slim type CPU modules only)

D8100	Data Link Slave Station Number (Port 2)	—	11-9
	Modbus Slave Number (Port 2)	—	12-14
D8101	Data Link Transmit Wait Time (ms)	—	11-13
D8102	— Reserved —	—	—
D8103	Online Mode Protocol Selection	When sending/ receiving data	Advanced Vol. 22-3
D8104	RS232C Control Signal Status (Ports 2 to 6)	Every scan	10-34
D8105	RS232C DSR Input Control Signal Option (Ports 2 to 6)	When sending/ receiving data	10-36
D8106	RS232C DTR Output Control Signal Option (Ports 2 to 6)	When sending/ receiving data	10-37
D8107-D8108	— Reserved —	—	—
D8109	Retry Cycles	At retry	Advanced Vol. 22-3
D8110	Retry Interval	Every scan during retry	Advanced Vol. 22-3
D8111	Modem Mode Status	At status transition	Advanced Vol. 22-3
D8112-D8114	— Reserved —	—	—

Device Address	Description	Updated	See Page
D8115-D8129	AT Command Result Code	When returning result code	Advanced Vol. 22-3
D8130-D8144	AT Command String	When sending AT command	Advanced Vol. 22-3
D8145-D8169	Initialization String	When sending init. string	Advanced Vol. 22-3
D8170-D8199	Telephone Number	When dialing	Advanced Vol. 22-4
D8200-D8203	— Reserved —	—	—
D8204	RS232C Control Signal Status (Port 7)	Every scan	10-34
D8205	RS232C DSR Input Control Signal Option (Port 7)	When sending/ receiving data	10-36
D8206	RS232C DTR Output Control Signal Option (Port 7)	When sending/ receiving data	10-37
D8207-D8209	— Reserved —	—	—

Special Data Registers for High-speed Counters (Slim type CPU modules only)

D8210	High-speed Counter 1 (I0-I2) Current Value (high word)	Every scan	5-17, 5-20
D8211	High-speed Counter 1 (I0-I2) Current Value (low word)	Every scan	5-17, 5-20
D8212	High-speed Counter 1 (I0-I2) Preset Value 1 (high word)	—	5-17, 5-20
D8213	High-speed Counter 1 (I0-I2) Preset Value 1 (low word)	—	5-17, 5-20
D8214	High-speed Counter 1 (I0-I2) Preset Value 2 (high word)	—	5-17, 5-20
D8215	High-speed Counter 1 (I0-I2) Preset Value 2 (low word)	—	5-17, 5-20
D8216	High-speed Counter 1 (I0-I2) Reset Value (high word)	—	5-17, 5-20
D8217	High-speed Counter 1 (I0-I2) Reset Value (low word)	—	5-17, 5-20
D8218	High-speed Counter 2 (I3) Current Value (high word)	Every scan	5-17
D8219	High-speed Counter 2 (I3) Current Value (low word)	Every scan	5-17
D8220	High-speed Counter 2 (I3) Preset Value (high word)	—	5-17
D8221	High-speed Counter 2 (I3) Preset Value (low word)	—	5-17
D8222	High-speed Counter 3 (I4) Current Value (high word)	Every scan	5-17
D8223	High-speed Counter 3 (I4) Current Value (low word)	Every scan	5-17
D8224	High-speed Counter 3 (I4) Preset Value (high word)	—	5-17
D8225	High-speed Counter 3 (I4) Preset Value (low word)	—	5-17
D8226	High-speed Counter 4 (I5-I7) Current Value (high word)	Every scan	5-17, 5-20
D8227	High-speed Counter 4 (I5-I7) Current Value (low word)	Every scan	5-17, 5-20
D8228	High-speed Counter 4 (I5-I7) Preset Value 1 (high word)	—	5-17, 5-20
D8229	High-speed Counter 4 (I5-I7) Preset Value 1 (low word)	—	5-17, 5-20
D8230	High-speed Counter 4 (I5-I7) Preset Value 2 (high word)	—	5-17, 5-20
D8231	High-speed Counter 4 (I5-I7) Preset Value 2 (low word)	—	5-17, 5-20
D8232	High-speed Counter 4 (I5-I7) Reset Value (high word)	—	5-17, 5-20
D8233	High-speed Counter 4 (I5-I7) Reset Value (low word)	—	5-17, 5-20
D8234-D8251	— Reserved —	—	—

Note: Devices for high and low words can be swapped on upgraded CPU modules with system program version 110 or higher. See page 5-47.

Special Data Register for Expansion Interface Module (Slim type CPU modules only)

Device Address	Description	Updated	See Page
D8252	Expansion Interface Module I/O Refresh Time (x100 µs)	Every scan	2-75
D8253-D8277	— Reserved —	—	—

Special Data Register for slim type web server CPU modules

D8278	Communication Mode Information (Client Connection)			Every scan	6-27
D8279	Communication Mode Information (Server Connection)			Every scan	6-27
D8280-D8301	— Reserved —			—	—
D8302	Memory Cartridge Capacity			Power-up	6-27
D8303	IP Address Switching			—	6-27
D8304-D8307	IP Address	(New Data)	Write only	—	6-27
D8308-D8311	Subnet Mask	(New Data)	Write only	—	6-27
D8312-D8315	Default Gateway	(New Data)	Write only	—	6-28
D8316-D8319	Preferred DNS Server	(New Data)	Write only	—	6-28
D8320-D8323	Alternate DNS Server	(New Data)	Write only	—	6-28
D8324-D8329	MAC Address	(Read only)		Every 1 sec	6-28
D8330-D8333	IP Address	(Current Data)	Read only	Every 1 sec	6-27
D8334-D8337	Subnet Mask	(Current Data)	Read only	Every 1 sec	6-27
D8338-D8341	Default Gateway	(Current Data)	Read only	Every 1 sec	6-28
D8342-D8345	Preferred DNS Server	(Current Data)	Read only	Every 1 sec	6-28
D8346-D8349	Alternate DNS Server	(Current Data)	Read only	Every 1 sec	6-28
D8350-D8353	Maintenance Communication Server 1 Connected IP Address			Every 1 sec	6-28
D8354-D8357	Maintenance Communication Server 2 Connected IP Address			Every 1 sec	6-28
D8358-D8361	Maintenance Communication Server 3 Connected IP Address			Every 1 sec	6-28
D8362-D8365	Server Connection 1 Connected IP Address			Every 1 sec	6-28
D8366-D8369	Server Connection 2 Connected IP Address			Every 1 sec	6-28
D8370-D8373	Server Connection 3 Connected IP Address			Every 1 sec	6-28
D8374-D8377	Server Connection 4 Connected IP Address			Every 1 sec	6-28
D8378-D8381	Server Connection 5 Connected IP Address			Every 1 sec	6-28
D8382-D8385	Server Connection 6 Connected IP Address			Every 1 sec	6-28
D8386-D8389	Server Connection 7 Connected IP Address			Every 1 sec	6-28
D8390-D8393	Server Connection 8 Connected IP Address			Every 1 sec	6-28
D8394-D8397	Client Connection 1 Remote IP Address			Every 1 sec	6-28
D8398-D8401	Client Connection 2 Remote IP Address			Every 1 sec	6-28
D8402-D8405	Client Connection 3 Remote IP Address			Every 1 sec	6-28
D8406-D8412	— Reserved —			—	—
D8413	Time Zone Offset			—	6-28
D8414	Year (Obtained from SNTP)			Every 500 ms	6-28
D8415	Month (Obtained from SNTP)			Every 500 ms	6-28
D8416	Day (Obtained from SNTP)			Every 500 ms	6-28
D8417	Day of Week (Obtained from SNTP)			Every 500 ms	6-28
D8418	Hour (Obtained from SNTP)			Every 500 ms	6-28
D8419	Minute (Obtained from SNTP)			Every 500 ms	6-28
D8420	Second (Obtained from SNTP)			Every 500 ms	6-28
D8421	Maintenance Communication Server 1 Port Number of Client			Every 1 sec	6-28

Device Address	Description	Updated	See Page
D8422	Maintenance Communication Server 2 Port Number of Client	Every 1 sec	6-28
D8423	Maintenance Communication Server 3 Port Number of Client	Every 1 sec	6-28
D8424	Server Connection 1 Port Number of Client	Every 1 sec	6-28
D8425	Server Connection 2 Port Number of Client	Every 1 sec	6-28
D8426	Server Connection 3 Port Number of Client	Every 1 sec	6-28
D8427	Server Connection 4 Port Number of Client	Every 1 sec	6-28
D8428	Server Connection 5 Port Number of Client	Every 1 sec	6-28
D8429	Server Connection 6 Port Number of Client	Every 1 sec	6-28
D8430	Server Connection 7 Port Number of Client	Every 1 sec	6-28
D8431	Server Connection 8 Port Number of Client	Every 1 sec	6-28
D8432-D8456	— Reserved —	—	—
D8457	EMAIL Error Information	—	6-28
D8458-D8499	— Reserved —	—	—

Note: Special data registers D8278 through D8457 are available on FC5A-D12K1E/S1E.

D8000 System Setup ID (Quantity of Inputs)

The total of input points provided on the CPU module and connected expansion input modules is stored to D8000. When a mixed I/O module (4 inputs and 4 outputs) is connected, 8 input points are added to the total.

D8001 System Setup ID (Quantity of Outputs)

The total of output points provided on the CPU module and connected expansion output modules is stored to D8001. When a mixed I/O module (4 inputs and 4 outputs) is connected, 8 output points are added to the total.

D8002 CPU Module Type Information

Information about the CPU module type is stored to D8002.

0: FC5A-C10R2, FC5A-C10R2C, or FC5A-C10R2D
1: FC5A-C16R2, FC5A-C16R2C, or FC5A-C16R2D
2: FC5A-D12K1E or FC5A-D12S1E
3: FC5A-C24R2, FC5A-C24R2C, or FC5A-C24R2D
4: FC5A-D32K3 or FC5A-D32S3
6: FC5A-D16RK1 or FC5A-D16RS1

D8003 Memory Cartridge Information

When an optional memory cartridge is installed on the CPU module cartridge connector, information about the user program stored on the memory cartridge is stored to D8003.

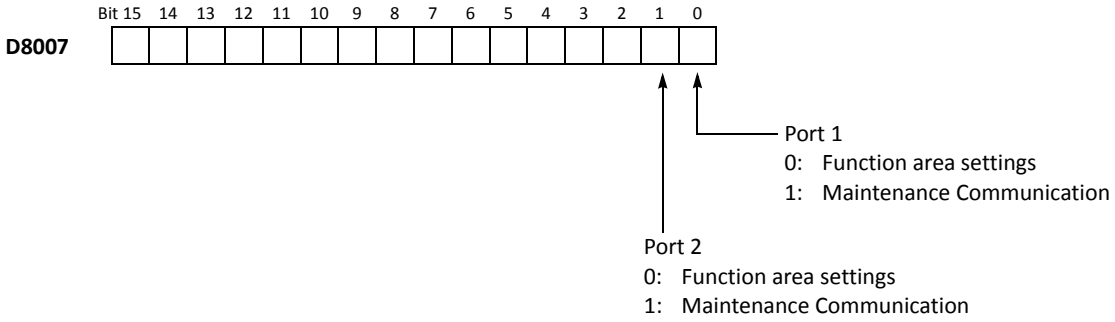
0: FC5A-C10R2, FC5A-C10R2C, or FC5A-C10R2D
1: FC5A-C16R2, FC5A-C16R2C, or FC5A-C16R2D
2: FC5A-D12K1E or FC5A-D12S1E
3: FC5A-C24R2, FC5A-C24R2C, or FC5A-C24R2D
4: FC5A-D32K3 or FC5A-D32S3
6: FC5A-D16RK1 or FC5A-D16RS1
255: The memory cartridge does not store any user program.

D8007 Communication Mode Switching (Port 1 and 2)

Communication modes for ports 1 and 2 can be changed to maintenance communication.

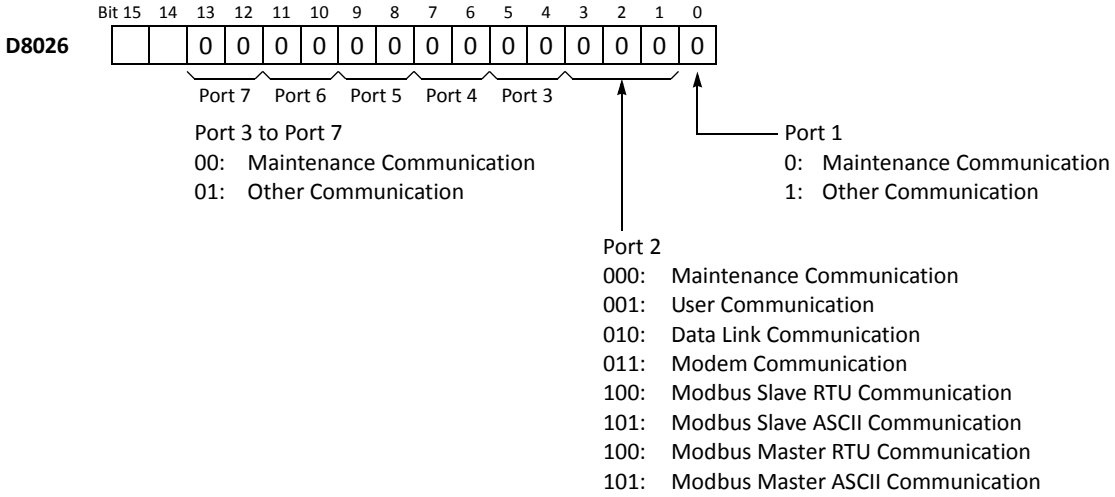
The communication mode is switched to maintenance communication by writing '1' to the bit corresponding to each port. When '0' is written, the communication mode configured in the function area settings takes effect. This function can be used with system program version 220 or higher.

Bit allocation of D8007 for each port is shown below.



D8026 Communication Mode Information (Port 1 to Port 7)

Communication mode information of port 1 through port 7 is stored to D8026.



D8029 System Program Version

The PLC system program version number is stored to D8029. This value is indicated in the PLC status dialog box called from the WindLDR menu bar. Select **Online** > **Monitor** > **Monitor**, then select **Online** > **Status**. See page 13-1.

D8030 Communication Adapter Information

Information about the communication adapter installed on the port 2 connector is stored to D8030.

0: RS232C communication adapter is installed
1: RS485 communication adapter is installed or no communication adapter is installed

D8031 Optional Cartridge Information

Information about the optional cartridge installed on the CPU module is stored to D8031.

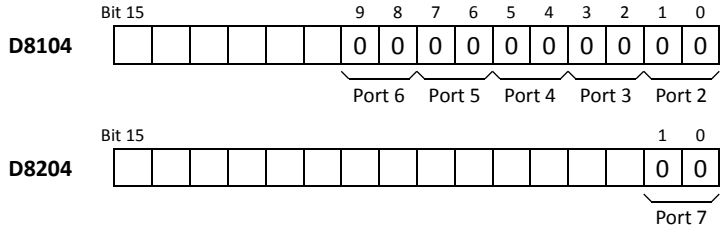
0: No optional cartridge is installed
1: Clock cartridge is installed
2: Memory cartridge is installed
3: Clock cartridge and memory cartridge are installed

D8037 Quantity of Expansion I/O Modules

The quantity of expansion I/O modules connected to the all-in-one 24-I/O type CPU module (except 12V DC power type) or any slim type CPU module is stored to D8037.

D8104 RS232C Control Signal Status (Port 2 to Port 6)
D8204 RS232C Control Signal Status (Port 7)

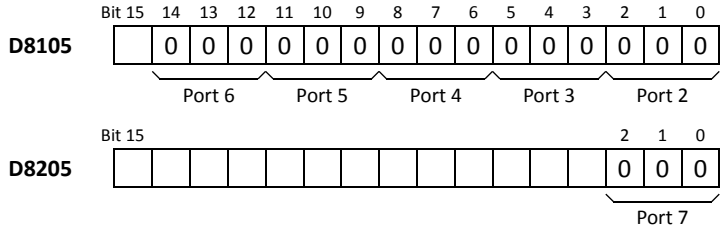
RS232C control signal status of port 2 through port 7 is stored to D8104 and D8204.



00: Both DSR and DTR are off
01: DSR is off, DTR is on
10: DSR is on, DTR is off
11: Both DSR and DTR are on

D8105 RS232C DSR Input Control Signal Option (Port 2 to Port 6)
D8205 RS232C DSR Input Control Signal Option (Port 7)

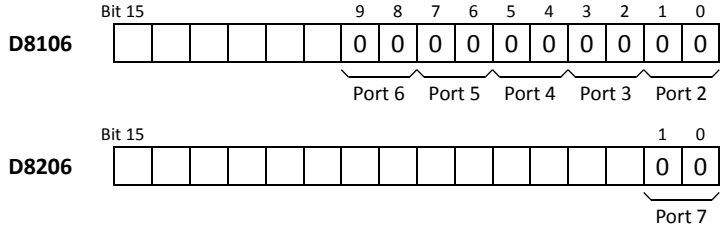
Special data registers D8105 and D8205 are used to control data flow between the MicroSmart RS232C port 2 through port 7 and the remote terminal depending on the DSR (data set ready) signal sent from the remote terminal.



000: DSR is not used for data flow control
001: When DSR is on, MicroSmart can transmit and receive data
010: When DSR is off, MicroSmart can transmit and receive data
011: When DSR is on, MicroSmart can transmit data (busy control)
010: When DSR is off, MicroSmart can transmit data
Others: Same as 000

D8106 RS232C DTR Output Control Signal Option (Port 2 to Port 6)
D8206 RS232C DTR Output Control Signal Option (Port 7)

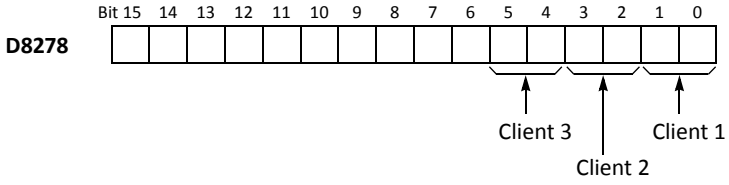
Special data registers D8106 and D8206 are used to control the DTR (data terminal ready) signal to indicate the MicroSmart operating status or transmitting/receiving status.



00: DTR is on (off while MicroSmart is stopped)
01: DTR is off
10: DSR is on while MicroSmart can receive data (auto switching)
11: Same as 00

D8278 Communication Mode Information (Client Connection)

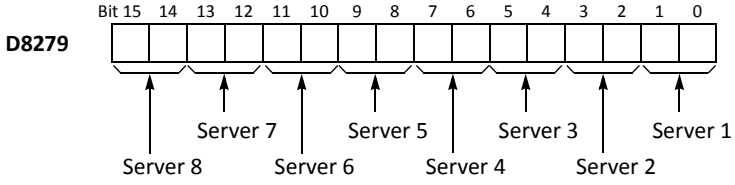
Communication mode information for client connections 1 through 3 is stored in D8278.



00: Reserved
01: User Communication
10: Modbus TCP Client
11: Unused

D8279 Communication Mode Information (Server Connection)

Communication mode information for server connections 1 through 8 is stored in D8279.



00: Maintenance Communication
01: User Communication
10: Modbus TCP Server
11: Unused

D8302 Memory Cartridge Capacity

The capacity of the memory cartridge installed on the CPU module is stored in D8302.

0: No memory cartridge is installed
32: 32 KB
64: 64 KB
128: 128 KB

D8303 IP Address Switching

Writing a value in D8303 makes it possible to forcibly change the way the network settings, such as IP address and DNS address, are acquired.

0: Function are settings
1: Enable DHCP
2: Use values in data registers D8303 through D8323

D8304-D8307, D8330-D8333 IP Address

IP address is stored in data registers as shown below.

Example) IP address: aaa.bbb.ccc.ddd

D8304=aaa, D8305=bbb, D8306=ccc, D8307=ddd

D8308-D8311, D8334-D8337 Subnet Mask

Subnet mask is stored in data registers as shown below.

Example) Subnet mask: aaa.bbb.ccc.ddd

D8308=aaa, D8309=bbb, D8310=ccc, D8311=ddd

D8312-D8315, D8338-D8341 Default Gateway

Default gateway is stored in data registers as shown below.

Example) Default gateway: aaa.bbb.ccc.ddd

D8312=aaa, D8313=bbb, D8314=ccc, D8315=ddd

D8316-D8319, D8342-D8345 Preferred DNS Server

Preferred DNS server address is stored in data registers as shown below.

Example) Preferred DNS server: aaa.bbb.ccc.ddd

D8316=aaa, D8317=bbb, D8318=ccc, D8319=ddd

D8320-D8323, D8346-D8349 Alternate DNS Server

Alternate DNS server address is stored in data registers as shown below.

Example) Alternate DNS server: aaa.bbb.ccc.ddd

D8320=aaa, D8321=bbb, D8322=ccc, D8323=ddd

D8324-D8329 MAC Address

MAC address is stored in data registers as shown below.

Example) MAC address: AA-BB-CC-DD-EE-FF

D8324=AA, D8325=BB, D8326=CC, D8327=DD, D8328=EE, D8329=FF

D8350-D8361 Maintenance Communication Server (1 through 3) Connected IP Address

The IP address of the remote host accessing the maintenance communication server is stored in special data registers.

Example) Maintenance Communication Server 1 Connected IP Address: aaa.bbb.ccc.ddd

D8350=aaa, D8351=bbb, D8352=ccc, D8353=ddd

D8362-D8393 Server Connection (1 through 8) Connected IP Address

The IP address of the remote host accessing the server connection 1 through 8 is stored in special data registers.

Example) Server Connection 1 Connected IP Address: aaa.bbb.ccc.ddd

D8362=aaa, D8363=bbb, D8364=ccc, D8365=ddd

D8394-D8405 Client Connection (1 through 3) Remote IP Address

The IP address of the remote host that the client connection 1 through 3 is accessing is stored in special data registers.

Example) Client Connection 1 Remote IP Address: aaa.bbb.ccc.ddd

D8394=aaa, D8395=bbb, D8396=ccc, D8397=ddd

D8413 Time Zone Offset

The time zone configured in the Function Area Settings can be adjusted with a multiple of 15 minutes. For details, see chapter 5 of FC5A User's Manual Web Server Vol.

D8414-D8420 Obtained from SNTP

When the SNTP server function is enabled, time data obtained from an SNTP server is adjusted according to the time zone, and the adjusted time is stored in special data registers D8414 to D8420. For details about the SNTP server and time zones, see Chapter 5 of FC5A User's Manual Web Server CPU Module Volume.

D8421-D8431 Port Number of Client

While a remote client is connecting to the server, the port number of the client is stored in the corresponding special data register.

D8457 EMAIL Error Information

The error information of EMAIL instruction execution is stored in D8457. For detail about EMAIL instruction, see chapter 10 of FC5A User's Manual Web Server Vol.

Expansion Data Registers

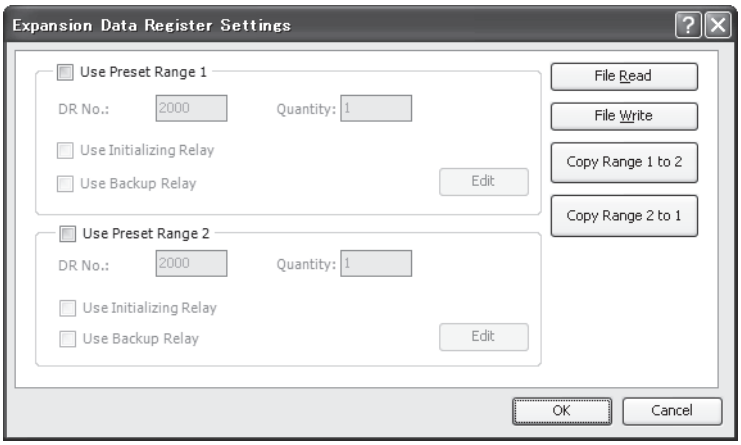
Slim type CPU modules FC5A-D16RK1, FC5A-D16RS1, FC5A-D32K3, FC5A-D32S3, FC5A-D12K1E, and FC5A-D12S1E have expansion data registers D2000 through D7999. These expansion data registers are normally used as ordinary data registers to store numerical data while the CPU module is executing a user program. In addition, numerical data can be set to designated ranges of expansion data registers using the expansion data register editor on WindLDR. When the user program is downloaded from WindLDR to the CPU module, the preset values of the expansion data registers are also downloaded to the ROM in the CPU module. Each time the CPU is powered up, the preset values of the expansion data registers stored in the ROM are loaded to the RAM and the user program in the RAM is executed.

Since the data in the ROM is non-volatile, the preset values of the expansion data registers are maintained semi-permanently and restored in the RAM each time the CPU is powered up. This feature is useful when particular numerical data must not be lost. Furthermore, data register values can be easily entered in the form of either numbers or character strings using the expansion data register editor on WindLDR.

Programming WindLDR

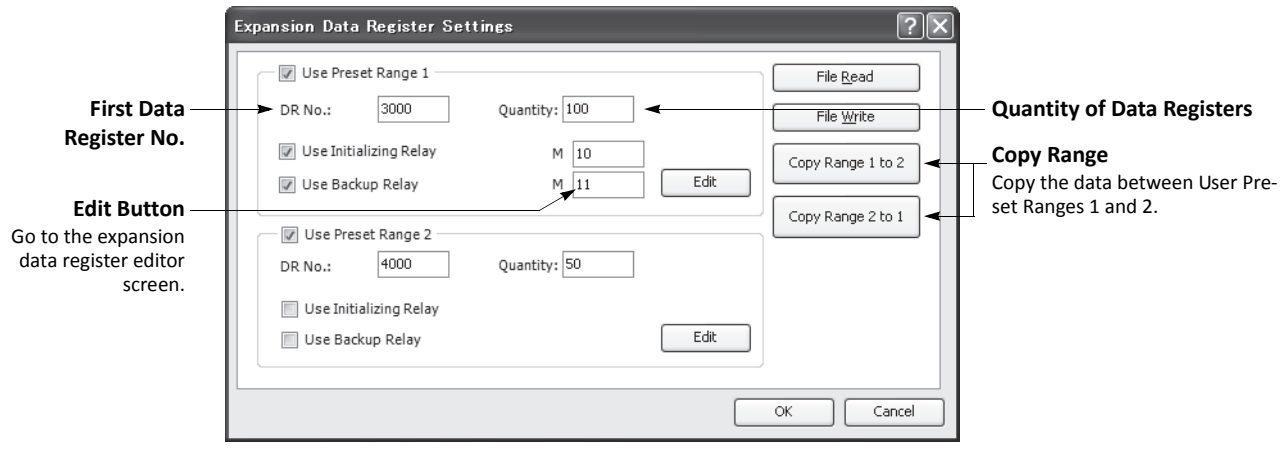
1. From the WindLDR menu bar, select **Configuration** > **Expansion Data Register**.

The Expansion Data Register Settings dialog box appears.



2. Click the check box to use the preset range 1 or 2.

Among expansion data registers D2000 through D7999, two ranges can be specified for preset data registers.

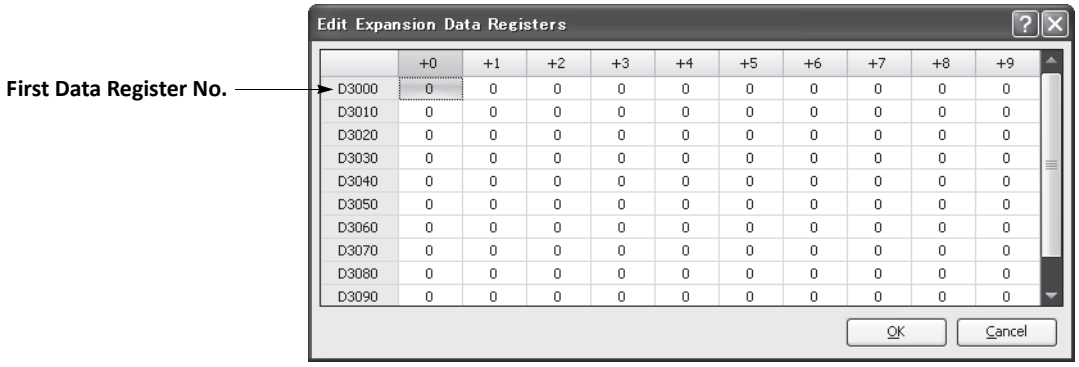


Use Preset Range 1 or 2: Click the check box, and type the first data register number in the **DR No.** box and the quantity of data registers to store preset values in the **Quantity** box.

Use Initializing Relay: Click the check box and specify an internal relay number to use as an initializing relay. When the initializing relay is turned on while the CPU is powered up, the preset values of the expansion data registers in the ROM are loaded to the RAM.

Use Backup Relay: Click the check box and specify an internal relay number to use as a backup relay. When the backup relay is turned on while the CPU is powered up, the values of the preset expansion data registers in the RAM overwrite the preset values in the ROM.

3. Click the **Edit** button. The Edit Expansion Data Registers screen appears.

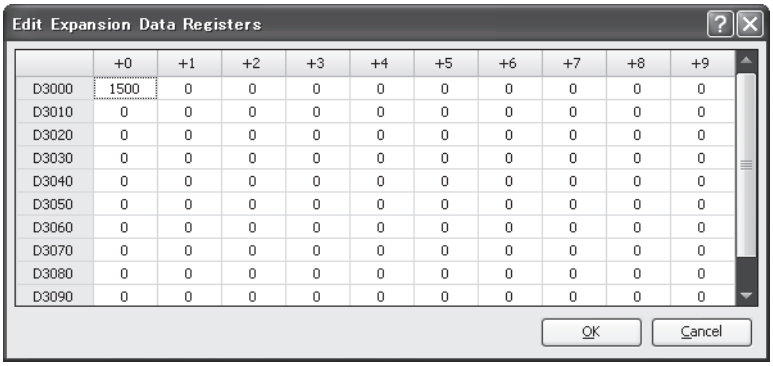


	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9
D3000	0	0	0	0	0	0	0	0	0	0
D3010	0	0	0	0	0	0	0	0	0	0
D3020	0	0	0	0	0	0	0	0	0	0
D3030	0	0	0	0	0	0	0	0	0	0
D3040	0	0	0	0	0	0	0	0	0	0
D3050	0	0	0	0	0	0	0	0	0	0
D3060	0	0	0	0	0	0	0	0	0	0
D3070	0	0	0	0	0	0	0	0	0	0
D3080	0	0	0	0	0	0	0	0	0	0
D3090	0	0	0	0	0	0	0	0	0	0

The specified quantity of data registers are reserved to store preset values in the Edit Expansion Data Registers screen. You can enter numerical values to these data registers individually, in the form of character strings, or fill the same value to consecutive data registers.

Enter Individual Values

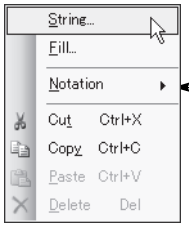
Click the data register number in the Edit Expansion Data Registers screen where you want to enter a numerical value, and type a value 0 through 65535. When finished, click **OK** to return to the Expansion Data Register Settings dialog box.



	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9
D3000	1500	0	0	0	0	0	0	0	0	0
D3010	0	0	0	0	0	0	0	0	0	0
D3020	0	0	0	0	0	0	0	0	0	0
D3030	0	0	0	0	0	0	0	0	0	0
D3040	0	0	0	0	0	0	0	0	0	0
D3050	0	0	0	0	0	0	0	0	0	0
D3060	0	0	0	0	0	0	0	0	0	0
D3070	0	0	0	0	0	0	0	0	0	0
D3080	0	0	0	0	0	0	0	0	0	0
D3090	0	0	0	0	0	0	0	0	0	0

Enter Character String

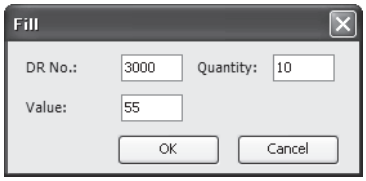
Click the right mouse button at the data register number in the Edit Expansion Data Registers screen where you want to enter a character string. A pop-up menu appears. Select **String** in the pop-up menu, then the String dialog box appears. Type required characters, and click **OK**. The entered characters are converted in pairs into ASCII decimal values and stored to data registers, starting with the selected data register number.



Select a notation to show the data in decimal, hexadecimal, or ASCII characters on the Edit Expansion Data Register screen.

Fill Same Value

Click the right mouse button at the data register number in the Edit Expansion Data Registers screen where you want to enter numerical values. A pop-up menu appears. Select **Fill** in the pop-up menu, then the Fill dialog box appears. Type the first data register number, the quantity of data registers, and the value. When finished, click **OK**. The value is entered to consecutive data registers.



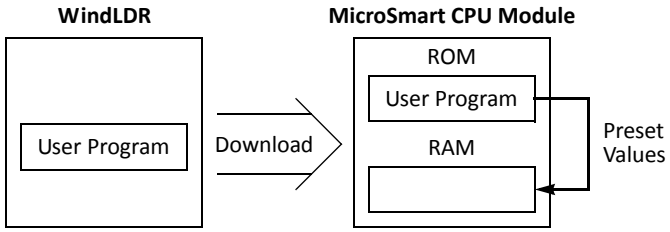
4. After editing the preset values of expansion data registers, download the user program to the CPU module since these settings relate to the user program.

Data Movement of Preset Data Registers

Like preset values for timers and counters (page 7-18), the preset data of expansion data registers can be changed in the RAM, the changed data can be cleared, and also stored to the ROM. The data movement is described below.

At Power-up and User Program Download

When the user program is downloaded to the CPU module, the data of preset data registers are also downloaded to the ROM. Each time the CPU is powered up, the data of preset data registers are loaded to the RAM. If the data of the expansion data registers have been changed as a result of advanced instructions or through communication, the changed data is cleared and initialized with the data of the preset data registers when the CPU is powered up again.

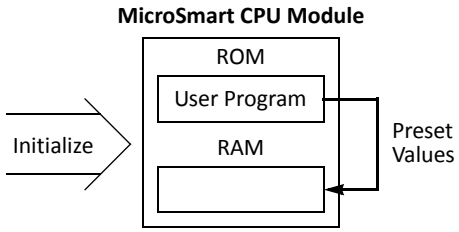


Since expansion data registers D2000 through D7999 are all "keep" types, the data in ordinary data registers are retained when the CPU is powered down.

Initializing Relay

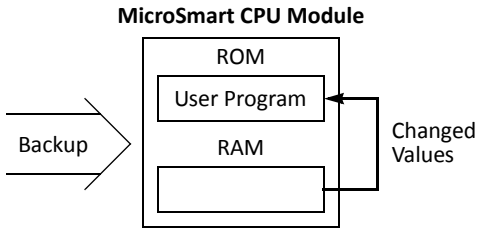
When the internal relay designated as an initializing relay is turned on, the data of preset data registers are loaded to the RAM as is the case when the CPU is powered up.

When the initialization is complete, the initializing relay is turned off automatically. When a user program is used to turn on the initializing relay, use a SOTU or SOTD to make sure that the initializing relay turns on for one scan only. When an initializing relay is not designated, the initialization cannot be performed.



Backup Relay

When the internal relay designated as a backup relay is turned on, the data of preset data registers are written from the RAM to the ROM as is the case with confirming changed timer/counter preset values. When the CPU is powered up again, the new data is loaded from the ROM to the RAM. When the user program is uploaded to WindLDR, the new data is also uploaded to the expansion data registers.



When the backup is complete, the backup relay is turned off automatically. When a user program is used to turn on the backup relay, use a SOTU or SOTD to make sure that the backup relay turns on for one scan only. When a backup relay is not designated, the backup cannot be performed.

Special Internal Relays for Expansion Data Registers

While data write from the RAM to expansion data register preset range 1 or 2 in the ROM is in progress, special internal relay M8026 or M8027 turns on, respectively. When data write is complete, the special internal relay turns off.

Notes for Using Expansion Data Registers:

- All expansion data registers are "keep" types and cannot be designated as "clear" types using the Function Area Settings.
- When expansion data registers are designated as source or destination devices of advanced instructions, the execution time takes slightly longer compared with ordinary data registers D0 through D1999.
- When a user program RAM sum check error has occurred, the data of preset expansion data registers are loaded to the RAM as is the case when the CPU is powered up.
- When the initializing relay is turned on, the scan time is extended until the data load from the ROM is completed by approximately 7 ms for every 1000 words of data read from the ROM. The data size can be calculated from the following formula:

  Data size (words) = 8.5 + Quantity of preset data registers

- When the backup relay is turned on, the scan time is extended until the data write to the ROM is completed for several scans by approximately 200 ms in every scan.
- Writing to the ROM can be repeated a maximum of 100,000 times. Keep writing to the ROM to a minimum.

Expansion I/O Module Devices

Expansion I/O modules are available in digital I/O modules and analog I/O modules.

Among the all-in-one type CPU modules, only the 24-I/O type CPU modules (except 12V DC power type) can connect a maximum of four expansion I/O modules including analog I/O modules.

All slim type CPU modules can connect a maximum of seven expansion I/O modules including analog I/O modules. When using the expansion interface module, another eight expansion I/O modules can be added.

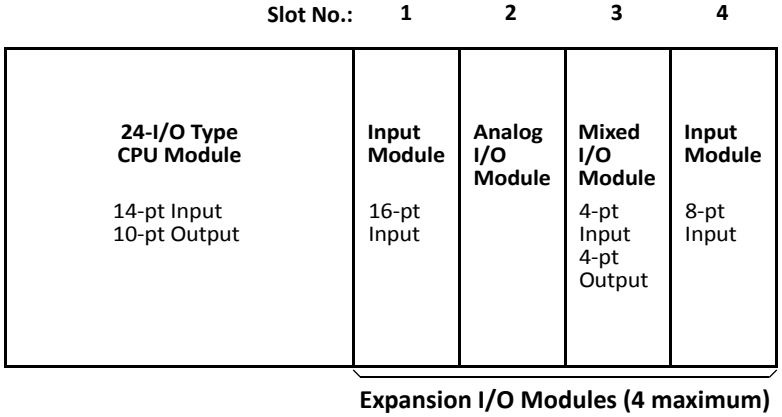
I/O Expansion for All-in-One Type CPU Modules

A maximum of four input, output, mixed I/O, or analog I/O modules can be mounted with the 24-I/O type CPU module (except 12V DC power type), so that the I/O points can be expanded to a maximum of 78 inputs or 74 outputs. The total of inputs and outputs can be a maximum of 88 points. Input and output numbers are automatically allocated to each digital I/O module, starting with I30 and Q30, in the order of increasing distance from the CPU module. Expansion I/O modules cannot be mounted with the 10- and 16-I/O type CPU modules, and the 24-I/O 12V DC power type CPU module.

I/O Device Addresses (All-in-One Type CPU Modules)

Device	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D		FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D		FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D		
	Device Adrs	Points	Device Adrs	Points	Device Adrs	Points	
Input (I)	I0 - I5	6	I0 - I7 I10	9	I0 - I7 I10 - I15	14	78 total (except 12V DC power type)
Expansion Input (I)	—	—	—	—	I30 - I107	64	
Output (Q)	Q0 - Q3	4	Q0 - Q6	7	Q0 - Q7 Q10 - Q11	10	74 total (except 12V DC power type)
Expansion Output (Q)	—	—	—	—	Q30 - Q107	64	

Example:



The system setup shown above will have I/O device addresses allocated for each module as follows:

Slot No.	Module	I/O Device Addresses
	24-I/O Type CPU Module	I0 to I7, I10 to I15, Q0 to Q7, Q10 and Q11
1	**16-pt Input Module**	I30 to I37, I40 to I47
2	**Analog I/O Module**	See page 9-9.
3	**4/4-pt Mixed I/O Module**	I50 to I53, Q30 to Q33
4	**8-pt Input Module**	I60 to I67

The I/O numbers of the CPU module start with I0 and Q0. The I/O numbers of the expansion I/O modules start with I30 and Q30. The mixed I/O module has 4 inputs and 4 outputs. When an I/O module is mounted next to a mixed I/O module, note that the device addresses skip four points as shown above.

Input and output modules may be grouped together for easy identification of I/O numbers. When the I/O modules are relocated, the I/O numbers are renumbered automatically.

I/O Expansion for Slim Type CPU Modules

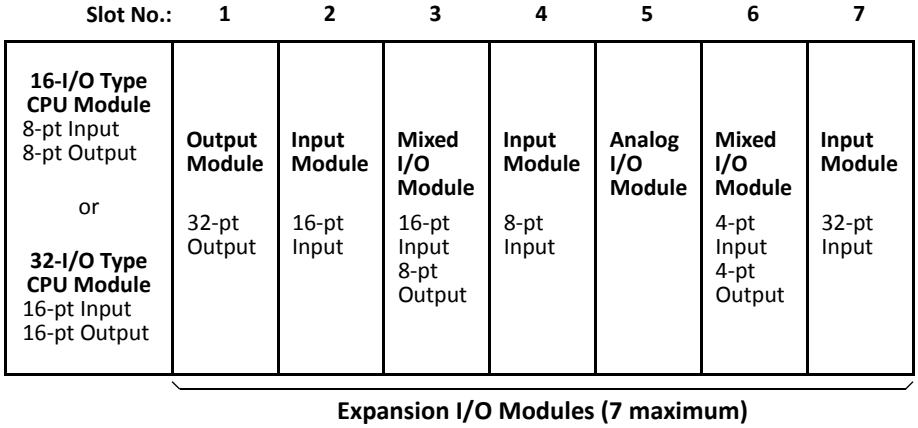
All slim type CPU modules can connect a maximum of seven expansion I/O modules including analog I/O modules. When using the expansion interface module, another eight expansion I/O modules can be added. For mounting AS-Interface master module, see page 24-1 (Advanced Vol.).

The expandable I/O points and the maximum total I/O points vary with the type of CPU module as listed below.

Device Addresses (Slim Type CPU Modules)

Device	FC5A-D16RK1 FC5A-D16RS1			FC5A-D32K3 FC5A-D32S3			FC5A-D12K1E FC5A-D12S1E		
	Device Address	Points		Device Address	Points		Device Address	Points	
Input (I)	I0 - I7	8	488 total	I0 - I7 I10 - I17	16	496 total	I0 - I7	8	488 total
Expansion Input (I)	I30 - I627	480		I30 - I627	480		I30 - I627	480	
Output (Q)	Q0 - Q7	8	488 total	Q0 - Q7 Q10 - Q17	16	496 total	Q0 - Q3	4	484 total
Expansion Output (Q)	Q30 - Q627	480		Q30 - Q627	480		Q30 - Q627	480	
Maximum Total I/O Points	496			512			492		

Example:



The system setup shown above will have I/O device addresses allocated for each module as follows:

Slot No.	Module	I/O Device Addresses
	32-I/O Type CPU Module	I0 to I7, I10 to I17, Q0 to Q7, Q10 to Q27
1	**32-pt Output Module**	Q30 to Q37, Q40 to Q47, Q50 to Q57, Q60 to Q67
2	**16-pt Input Module**	I30 to I37, I40 to I47
3	**16/8-pt Mixed I/O Module**	I50 to I57, I60 to I67, Q70 to Q77
4	**8-pt Input Module**	I70 to I77
5	**Analog I/O Module**	See page 9-9.
6	**4/4-pt Mixed I/O Module**	I80 to I83, Q80 to Q83
7	**32-pt Input Module**	I90 to I97, I100 to I107, I110 to I117, I120 to I127

The I/O numbers of the CPU module start with I0 and Q0. The I/O numbers of the expansion I/O modules start with I30 and Q30. When an I/O module is mounted next to a 4/4-point mixed I/O module, note that the device addresses skip four points as shown above.

Input and output modules may be grouped together for easy identification of I/O numbers. When the I/O modules are relocated, the I/O numbers are renumbered automatically.

7: BASIC INSTRUCTIONS

Introduction

This chapter describes programming of the basic instructions, available devices, and sample programs.

New basic instructions CDPD, DNTD, CUDD, TIMO, TMHO, TMLO, and TMSO are available on FC5A MicroSmart CPU module with system program version 200 or higher.

All other basic instructions are available on all FC5A MicroSmart CPU modules.

Basic Instruction List

Symbol	Name	Function	See Page
AND	And	Series connection of NO contact	7-5
AND LOD	And Load	Series connection of circuit blocks	7-6
ANDN	And Not	Series connection of NC contact	7-5
BPP	Bit Pop	Restores the result of bit logical operation which was saved temporarily	7-7
BPS	Bit Push	Saves the result of bit logical operation temporarily	7-7
BRD	Bit Read	Reads the result of bit logical operation which was saved temporarily	7-7
CC=	Counter Comparison (=)	Equal to comparison of counter current value	7-19
CC≥	Counter Comparison (≥)	Greater than or equal to comparison of counter current value	7-19
CDP	Dual Pulse Reversible Counter	Dual pulse reversible counter (0 to 65,535)	7-12
CDPD	Double-word Dual Pulse Reversible Counter	Double-word dual pulse reversible counter (0 to 4,294,967,295)	7-16
CNT	Adding Counter	Adding counter (0 to 65,535)	7-12
CNTD	Double-word Adding Counter	Double-word adding counter (0 to 4,294,967,295)	7-15
CUD	Up/Down Selection Reversible Counter	Up/down selection reversible counter (0 to 65,535)	7-12
CUDD	Double-word Up/Down Selection Reversible Counter	Double-word up/down selection reversible counter (0 to 4,294,967,295)	7-17
DC=	Data Register Comparison (=)	Equal to comparison of data register value	7-21
DC≥	Data Register Comparison (≥)	Greater than or equal to comparison of data register value	7-21
END	End	Ends a program	7-31
JEND	Jump End	Ends a jump instruction	7-30
JMP	Jump	Jumps a designated program area	7-30
LOD	Load	Stores intermediate results and reads contact status	7-3
LODN	Load Not	Stores intermediate results and reads inverted contact status	7-3
MCR	Master Control Reset	Ends a master control	7-28
MCS	Master Control Set	Starts a master control	7-28
OR	Or	Parallel connection of NO contact	7-5
OR LOD	Or Load	Parallel connection of circuit blocks	7-6
ORN	Or Not	Parallel connection of NC contact	7-5
OUT	Output	Outputs the result of bit logical operation	7-3
OUTN	Output Not	Outputs the inverted result of bit logical operation	7-3
RST	Reset	Resets output, internal relay, or shift register bit	7-4
SET	Set	Sets output, internal relay, or shift register bit	7-4

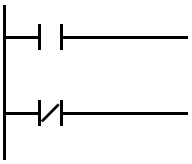
Symbol	Name	Function	See Page
SFR	Shift Register	Forward shift register	7-23
SFRN	Shift Register Not	Reverse shift register	7-23
SOTD	Single Output Down	Falling-edge differentiation output	7-27
SOTU	Single Output Up	Rising-edge differentiation output	7-27
TIM	100-ms Timer	Subtracting 100-ms timer (0 to 6553.5 sec)	7-8
TIMO	100-ms Off-delay Timer	Subtracting 100-ms off-delay timer (0 to 6553.5 sec)	7-11
TMH	10-ms Timer	Subtracting 10-ms timer (0 to 655.35 sec)	7-8
TMHO	10-ms Off-delay Timer	Subtracting 10-ms off-delay timer (0 to 655.35 sec)	7-11
TML	1-sec Timer	Subtracting 1-sec timer (0 to 65535 sec)	7-8
TMLO	1-sec Off-delay Timer	Subtracting 1-sec off-delay timer (0 to 65535 sec)	7-11
TMS	1-ms Timer	Subtracting 1-ms timer (0 to 65.535 sec)	7-8
TMSO	1-ms Off-delay Timer	Subtracting 1-ms off-delay timer (0 to 65.535 sec)	7-11

LOD (Load) and LODN (Load Not)

The LOD instruction starts the logical operation with a NO (normally open) contact. The LODN instruction starts the logical operation with a NC (normally closed) contact.

A total of eight LOD and/or LODN instructions can be programmed consecutively.

Ladder Diagram



Valid Devices

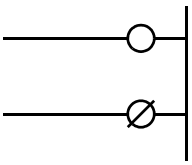
Instruction	I	Q	M	T	C	R	D
LOD LODN	0-627	0-627	0-2557 8000-8317	0-255	0-255	0-255	0.0-49999.15

The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
Data registers can be used as bit devices with the data register number and the bit position separated by a period.

OUT (Output) and OUTN (Output Not)

The OUT instruction outputs the result of bit logical operation to the specified device. The OUTN instruction outputs the inverted result of bit logical operation to the specified device.

Ladder Diagram



Valid Devices

Instruction	I	Q	M	T	C	R	D
OUT OUTN	—	0-627	0-2557 8000-8317	—	—	—	0.0-49999.15

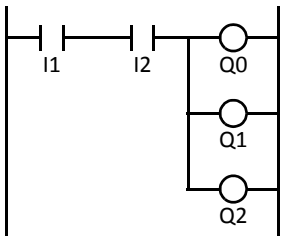
The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
Data registers can be used as bit devices with the data register number and the bit position separated by a period.

Caution • For restrictions on ladder programming of OUT and OUTN instructions, see page 7-32.

Multiple OUT and OUTN

There is no limit to the number of OUT and OUTN instructions that can be programmed into one rung.

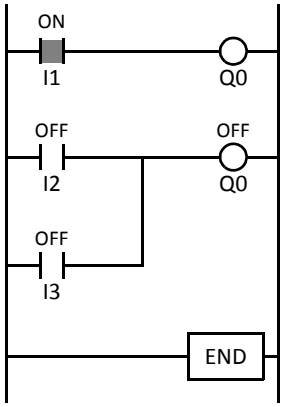
Ladder Diagram



Programming multiple outputs of the same output number is not recommended. However, when doing so, it is good practice to separate the outputs with the JMP/JEND set of instructions, or the MCS/MCR set of instructions. These instructions are detailed later in this chapter.

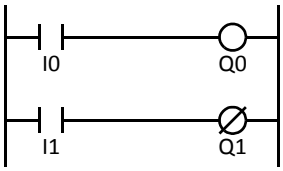
When the same output number is programmed more than once within one scan, the output nearest to the END instruction is given priority for outputting. In the example on the right, output Q0 is off.

Ladder Diagram



Examples: LOD (Load), OUT (Output), and NOT

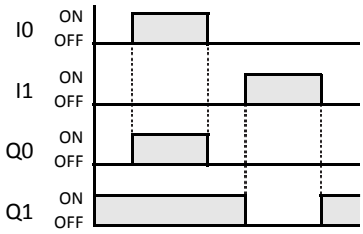
Ladder Diagram



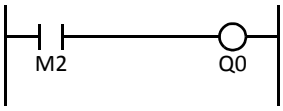
Program List

Instruction	Data
LOD	I0
OUT	Q0
LOD	I1
OUTN	Q1

Timing Chart



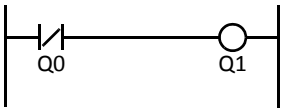
Ladder Diagram



Program List

Instruction	Data
LOD	M2
OUT	Q0

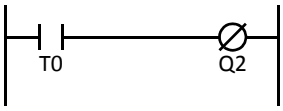
Ladder Diagram



Program List

Instruction	Data
LODN	Q0
OUT	Q1

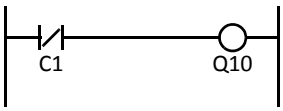
Ladder Diagram



Program List

Instruction	Data
LOD	T0
OUTN	Q2

Ladder Diagram



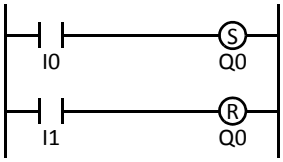
Program List

Instruction	Data
LODN	C1
OUT	Q10

SET and RST (Reset)

The SET and RST (reset) instructions are used to set (on) or reset (off) outputs, internal relays, and shift register bits. The same output can be set and reset many times within a program. SET and RST instructions operate in every scan while the input is on.

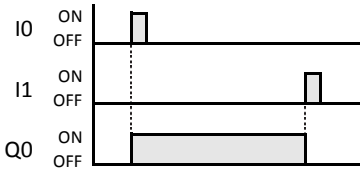
Ladder Diagram



Program List

Instruction	Data
LOD	I0
SET	Q0
LOD	I1
RST	Q0

Timing Chart



Valid Devices

Instruction	I	Q	M	T	C	R	D
SET RST	—	0-627	0-2557 8000-8317	—	—	0-255	0.0-49999.15

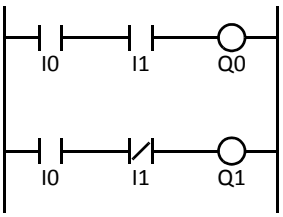
The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.

Caution • For restrictions on ladder programming of SET and RST instructions, see page 7-32.

AND and ANDN (And Not)

The AND instruction is used for programming a NO contact in series. The ANDN instruction is used for programming a NC contact in series. The AND or ANDN instruction is entered after the first set of contacts.

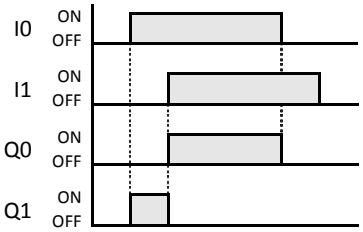
Ladder Diagram



Program List

Instruction	Data
LOD	I0
AND	I1
OUT	Q0
LOD	I0
ANDN	I1
OUT	Q1

Timing Chart



When both inputs I0 and I1 are on, output Q0 is on. When either input I0 or I1 is off, output Q0 is off.
When input I0 is on and input I1 is off, output Q1 is on. When either input I0 is off or input I1 is on, output Q1 is off.

Valid Devices

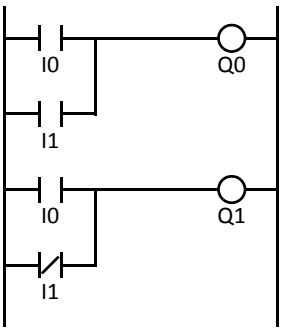
Instruction	I	Q	M	T	C	R	D
AND ANDN	0-627	0-627	0-2557 8000-8317	0-255	0-255	0-255	0.0-49999.15

The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
Data registers can be used as bit devices with the data register number and the bit position separated by a period.

OR and ORN (Or Not)

The OR instruction is used for programming a NO contact in parallel. The ORN instruction is used for programming a NC contact in parallel. The OR or ORN instruction is entered after the first set of contacts.

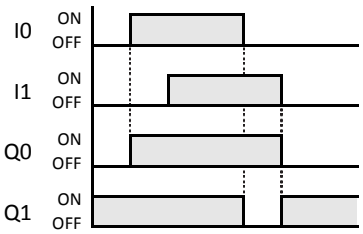
Ladder Diagram



Program List

Instruction	Data
LOD	I0
OR	I1
OUT	Q0
LOD	I0
ORN	I1
OUT	Q1

Timing Chart



When either input I0 or I1 is on, output Q0 is on. When both inputs I0 and I1 are off, output Q0 is off.
When either input I0 is on or input I1 is off, output Q1 is on. When input I0 is off and input I1 is on, output Q1 is off.

Valid Devices

Instruction	I	Q	M	T	C	R	D
OR ORN	0-627	0-627	0-2557 8000-8317	0-255	0-255	0-255	0.0-49999.15

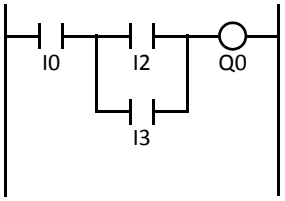
The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
Data registers can be used as bit devices with the data register number and the bit position separated by a period.

AND LOD (Load)

The AND LOD instruction is used to connect, in series, two or more circuits starting with the LOD instruction. The AND LOD instruction is the equivalent of a “node” on a ladder diagram.

When using WindLDR, the user need not program the AND LOD instruction. The circuit in the ladder diagram shown below is converted into AND LOD when the ladder diagram is compiled.

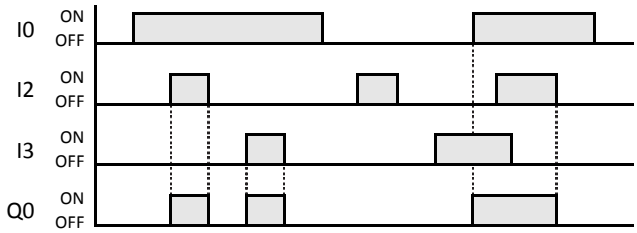
Ladder Diagram



Program List

Instruction	Data
LOD	I0
LOD	I2
OR	I3
ANDLOD	
OUT	Q0

Timing Chart



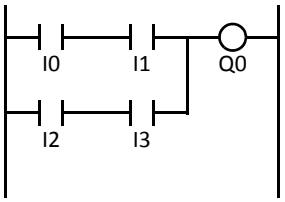
When input I0 is on and either input I2 or I3 is on, output Q0 is on.
When input I0 is off or both inputs I2 and I3 are off, output Q0 is off.

OR LOD (Load)

The OR LOD instruction is used to connect, in parallel, two or more circuits starting with the LOD instruction. The OR LOD instruction is the equivalent of a “node” on a ladder diagram.

When using WindLDR, the user need not program the OR LOD instruction. The circuit in the ladder diagram shown below is converted into OR LOD when the ladder diagram is compiled.

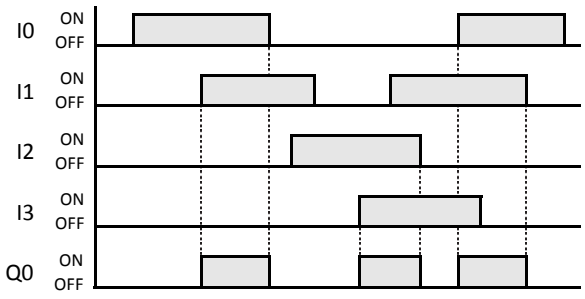
Ladder Diagram



Program List

Instruction	Data
LOD	I0
AND	I1
LOD	I2
AND	I3
ORLOD	
OUT	Q0

Timing Chart



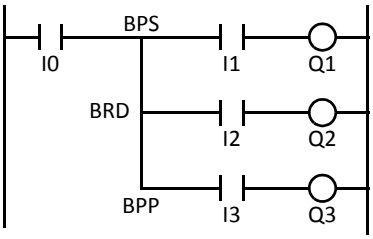
When both inputs I0 and I1 are on or both inputs I2 and I3 are on, output Q0 is on.
When either input I0 or I1 is off and either input I2 or I3 is off, output Q0 is off.

BPS (Bit Push), BRD (Bit Read), and BPP (Bit Pop)

The BPS (bit push) instruction is used to save the result of bit logical operation temporarily.
The BRD (bit read) instruction is used to read the result of bit logical operation which was saved temporarily.
The BPP (bit pop) instruction is used to restore the result of bit logical operation which was saved temporarily.

When using WindLDR, the user need not program the BPS, BRD, and BPP instructions. The circuit in the ladder diagram shown below is converted into BPS, BRD, and BPP when the ladder diagram is compiled.

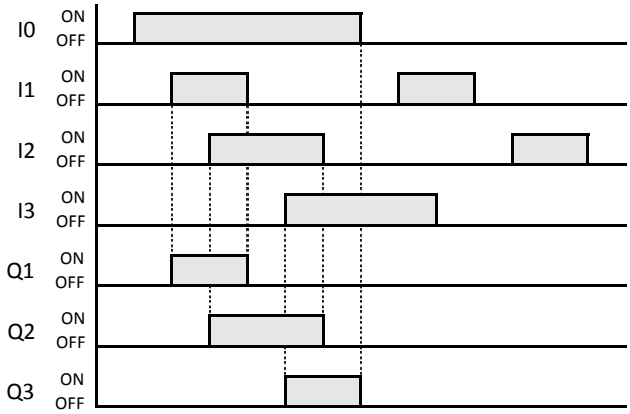
Ladder Diagram



Program List

Instruction	Data
LOD	I0
BPS	
AND	I1
OUT	Q1
BRD	
AND	I2
OUT	Q2
BPP	
AND	I3
OUT	Q3

Timing Chart



When both inputs I0 and I1 are on, output Q1 is turned on.
When both inputs I0 and I2 are on, output Q2 is turned on.
When both inputs I0 and I3 are on, output Q3 is turned on.

TML, TIM, TMH, and TMS (Timer)

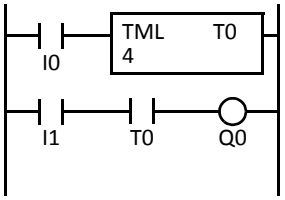
Four types of timedown timers are available; 1-sec timer TML, 100-ms timer TIM, 10-ms timer TMH, and 1-ms timer TMS. A total of 256 timers can be programmed in a user program for any type of CPU module. Each timer must be allocated to a unique number T0 through T255.

Timer	Device Address	Range	Increments	Preset Value
TML (1-sec timer)	T0 to T255	0 to 65535 sec	1 sec	Constant: 0 to 65535 Data registers: D0 to D1999 D2000 to D7999 D10000 to D49999
TIM (100-ms timer)	T0 to T255	0 to 6553.5 sec	100 ms	
TMH (10-ms timer)	T0 to T255	0 to 655.35 sec	10 ms	
TMS (1-ms timer)	T0 to T255	0 to 65.535 sec	1 ms	

The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
The preset value can be 0 through 65535 and designated using a decimal constant or data register.

TML (1-sec Timer)

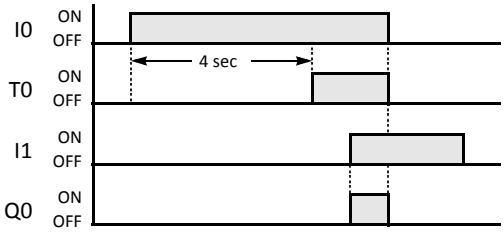
Ladder Diagram (TML)



Program List

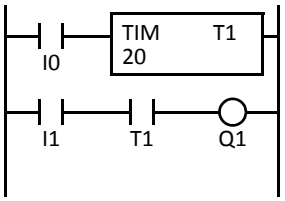
Instruction	Data
LOD	I0
TML	T0
	4
LOD	I1
AND	T0
OUT	Q0

Timing Chart



TIM (100-ms Timer)

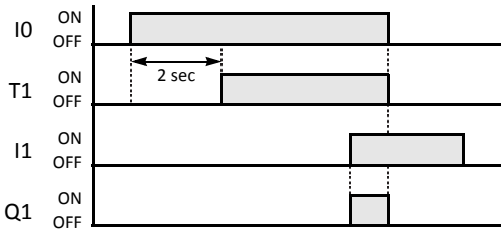
Ladder Diagram (TIM)



Program List

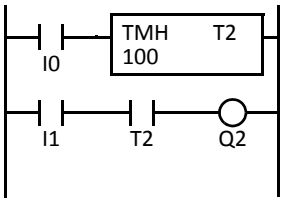
Instruction	Data
LOD	I0
TIM	T1
	20
LOD	I1
AND	T1
OUT	Q1

Timing Chart



TMH (10-ms Timer)

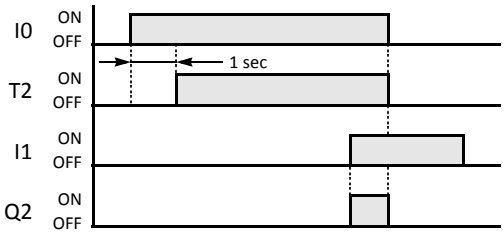
Ladder Diagram (TMH)



Program List

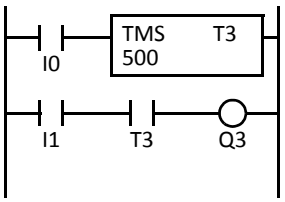
Instruction	Data
LOD	I0
TMH	T2
	100
LOD	I1
AND	T2
OUT	Q2

Timing Chart



TMS (1-ms Timer)

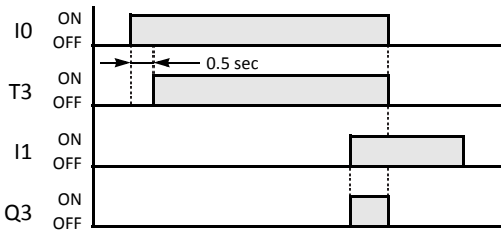
Ladder Diagram (TMS)



Program List

Instruction	Data
LOD	I0
TMS	T3
	500
LOD	I1
AND	T3
OUT	Q3

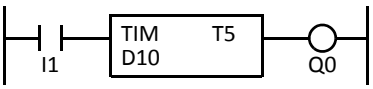
Timing Chart



Timer Circuit

The preset value 0 through 65535 can be designated using a data register D0 through D1999 or D2000 through D7999; then the data of the data register becomes the preset value. Directly after the TML, TIM, TMH, or TMS instruction, the OUT, OUTN, SET, RST, TML, TIM, TMH, or TMS instruction can be programmed.

Ladder Diagram



Program List

Instruction	Data
LOD	I1
TIM	T5
	D10
OUT	Q0

Caution

- For restrictions on ladder programming of timer instructions, see page 7-32.

- Timedown from the preset value is initiated when the operation result directly before the timer input is on.
- The timer output turns on when the current value (timed value) reaches 0.
- The current value returns to the preset value when the timer input is off.
- Timer preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor > Monitor**, then **Online** > **Custom** > **New Custom Monitor**.
- If a timer preset value is changed during timedown, the timer remains unchanged for that cycle. The change will be reflected in the next time cycle.
- If a timer preset value is changed to 0, then the timer stops operation, and the timer output is turned on immediately.
- If a current value is changed during timedown, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18. Preset values can also be changed and changed preset values can be confirmed using the HMI module. See pages 5-63 and 5-65.
- WindLDR ladder diagrams show TP (timer preset value) and TC (timer current value) in advanced instruction devices.

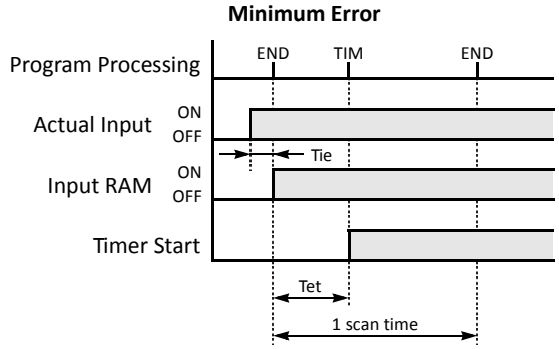
Timer Accuracy

Timer accuracy due to software configuration depends on three factors: timer input error, timer counting error, and time-out output error. These errors are not constant but vary with the user program and other causes.

Timer Input Error

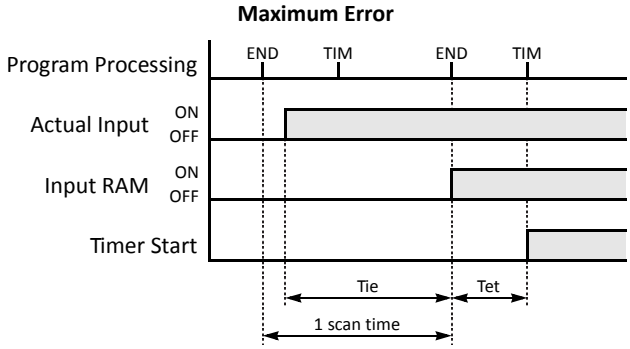
The input status is read at the END processing and stored to the input RAM. So, an error occurs depending on the timing when the timer input turns on in a scan cycle. The same error occurs on the normal input and the catch input. The timer input error shown below does not include input delay caused by the hardware.

Minimum Error



When the input turns on immediately before the END processing, Tie is almost 0. Then the timer input error is only Tet (behind error) and is at its minimum.

Maximum Error



When the input turns on immediately after the END processing, Tie is almost equal to one scan time. Then the timer input error is Tie + Tet = one scan time + Tet (behind error) and is at its maximum.

Tie: Time from input turning on to the END processing
Tet: Time from the END processing to the timer instruction execution

Timer Accuracy, continued

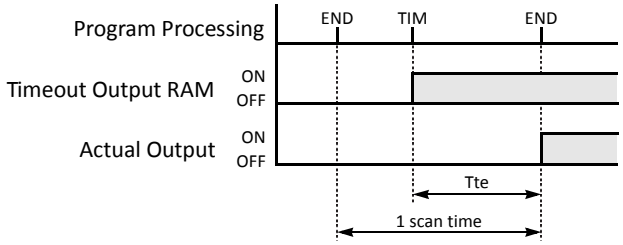
Timer Counting Error

Every timer instruction operation is individually based on asynchronous 16-bit reference timers. Therefore, an error occurs depending on the status of the asynchronous 16-bit timer when the timer instruction is executed. Use of the TMS (1-ms timer) is recommended as often as possible to make sure that the advance error is reduced to the minimum.

Error		TML (1-sec timer)	TIM (100-ms timer)	TMH (10-ms timer)	TMS (1-ms timer)
Maximum	Advance error	1000 ms	100 ms	10 ms	1 ms
	Behind error	1 scan time	1 scan time	1 scan time	1 scan time

Timeout Output Error

The output RAM status is set to the actual output when the END instruction is processed. So, an error occurs depending on the timing when the timeout output turns on in a scan cycle. The timeout output error shown below does not include output delay caused by the hardware.



Timeout output error is equal to Tte (behind error) and can be between 0 and one scan time.

0 < Tte < 1 scan time

Tte: Time from the timer instruction execution to the END processing

Maximum and Minimum of Errors

Error		Timer Input Error	Timer Counting Error	Timeout Output Error	Total Error
Minimum	Advance error	0 (Note)	0	0 (Note)	0
	Behind error	Tet	0	Tte	0
Maximum	Advance error	0 (Note)	Increment	0 (Note)	Increment – (Tet + Tte)
	Behind error	1 scan time + Tet	1 scan time	Tte	2 scan times + (Tet + Tte)

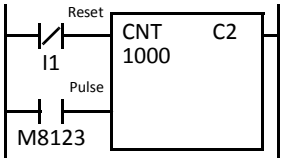
Notes: Advance error does not occur at the timer input and timeout output.
Tet + Tte = 1 scan time
Increment is 1 sec (TML), 100 ms (TIM), 10 ms (TMH), or 1 ms (TMS).
The maximum advance error is: Increment – 1 scan time
The maximum behind error is: 3 scan times

The timer input error and timeout output error shown above do not include the input response time (behind error) and output response time (behind error) caused by hardware.

Power Failure Memory Protection

Timers TML, TIM, TMH, and TMS do not have power failure protection. A timer with this protection can be devised using a counter instruction and special internal relay M8121 (1-sec clock), M8122 (100-ms clock), or M8123 (10-ms clock).

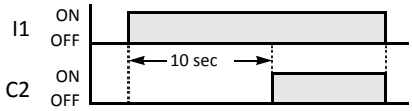
Ladder Diagram
(10-sec Timer)



Program List

Instruction	Data
LODN	I1
LOD	M8123
CNT	C2
	1000

Timing Chart



Note: Designate counter C2 used in this program as a keep type counter. See page 5-5.

TMLO, TIMO, TMHO, and TMSO (Off-Delay Timer)

Four types of timedown off-delay timers are available; 1-sec off-delay timer TMLO, 100-ms off-delay timer TIMO, 10-ms off-delay timer TMHO, and 1-ms off-delay timer TMSO. A total of 256 on- and off-delay timers can be programmed in a user program for any type of CPU module. Each timer must be allocated to a unique number T0 through T255.

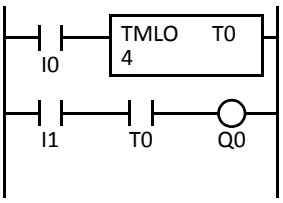
These instructions are available on upgraded CPU modules with system program version 200 or higher.

Timer	Device Address	Range	Increments	Preset Value
TMLO (1-sec off-delay timer)	T0 to T255	0 to 65535 sec	1 sec	Constant: 0 to 65535 Data registers: D0 to D1999 D2000 to D7999 D10000 to D49999
TIMO (100-ms off-delay timer)	T0 to T255	0 to 6553.5 sec	100 ms	
TMHO (10-ms off-delay timer)	T0 to T255	0 to 655.35 sec	10 ms	
TMSO (1-ms off-delay timer)	T0 to T255	0 to 65.535 sec	1 ms	

The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
The preset value can be 0 through 65535 and designated using a constant or a data register.

TMLO (1-sec Off-delay Timer)

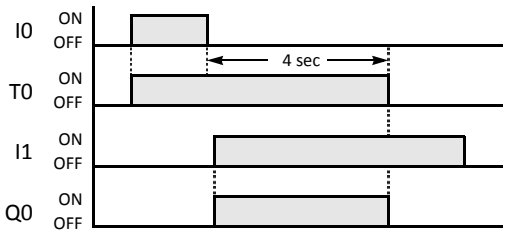
Ladder Diagram (TMLO)



Program List

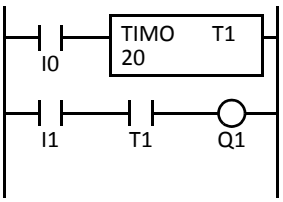
Instruction	Data
LOD	I0
TMLO	T0
	4
LOD	I1
AND	T0
OUT	Q0

Timing Chart



TIMO (100-ms Off-delay Timer)

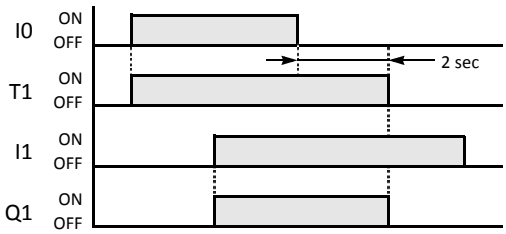
Ladder Diagram (TIMO)



Program List

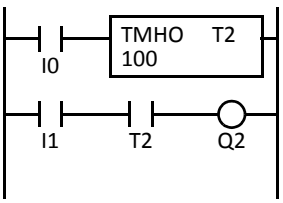
Instruction	Data
LOD	I0
TIMO	T1
	20
LOD	I1
AND	T1
OUT	Q1

Timing Chart



TMHO (10-ms Off-delay Timer)

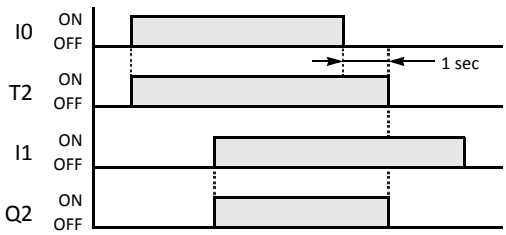
Ladder Diagram (TMHO)



Program List

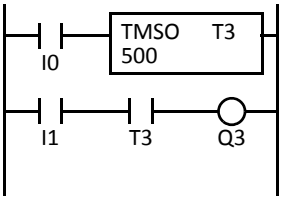
Instruction	Data
LOD	I0
TMHO	T2
	100
LOD	I1
AND	T2
OUT	Q2

Timing Chart



TMSO (1-ms Off-delay Timer)

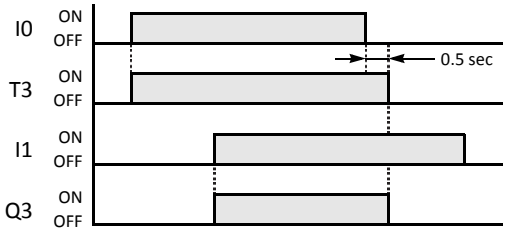
Ladder Diagram (TMSO)



Program List

Instruction	Data
LOD	I0
TMSO	T3
	500
LOD	I1
AND	T3
OUT	Q3

Timing Chart



CNT, CDP, and CUD (Counter)

Three types of counters are available; adding (up) counter CNT, dual-pulse reversible counter CDP, and up/down selection reversible counter CUD. A total of 256 counters can be programmed in a user program for any type of CPU module. Each counter must be allocated to a unique number C0 through C255.

Counter	Device Address	Preset Value
CNT (adding counter)	C0 to C255	Constant: 0 to 65535 Data registers: D0 to D1999 D2000 to D7999 D10000 to D49999
CDP (dual-pulse reversible counter)	C0 to C255	
CUD (up/down selection reversible counter)	C0 to C255	

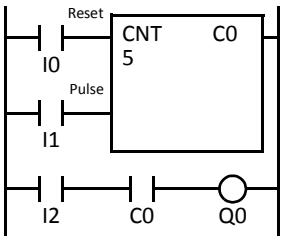
The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
The preset value can be 0 through 65535 and designated using a decimal constant or data register.

CNT (Adding Counter)

When counter instructions are programmed, two addresses are required. The circuit for an adding (UP) counter must be programmed in the following order: reset input, pulse input, the CNT instruction, and a counter number C0 through C255, followed by a counter preset value from 0 to 65535.

The preset value can be designated using a decimal constant or a data register. When a data register is used, the data of the data register becomes the preset value.

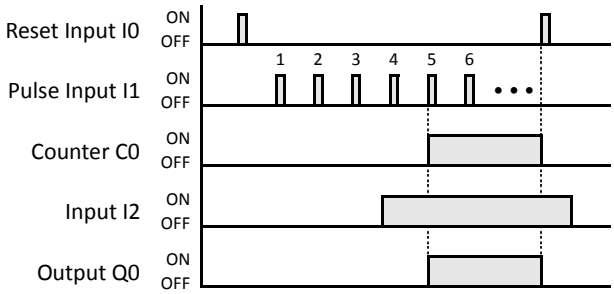
Ladder Diagram



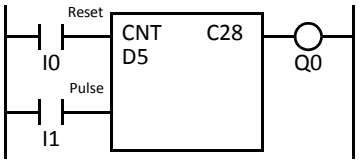
Program List

Instruction	Data
LOD	I0
LOD	I1
CNT	C0
	5
LOD	I2
AND	C0
OUT	Q0

Timing Chart



- The preset value 0 through 65535 can be designated using a data register D0 through D1999 (all CPU modules) or D2000 through D7999 and D10000 through D49999 (slim type CPU modules); then the data of the data register becomes the preset value. Directly after the CNT instruction, the OUT, OUTN, SET, RST, TML, TIM, TMH, or TMS instruction can be programmed.



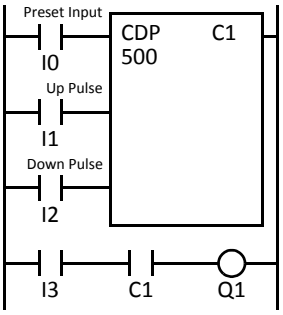
- The same counter number cannot be programmed more than once.
- While the reset input is off, the counter counts the leading edges of pulse inputs and compares them with the preset value.
- When the current value reaches the preset value, the counter turns output on. The output stays on until the reset input is turned on.
- When the reset input changes from off to on, the current value is reset.
- When the reset input is on, all pulse inputs are ignored.
- The reset input must be turned off before counting may begin.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. Change the current value while the counter reset input is off.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18. Preset values can also be changed and changed preset values can be confirmed using the HMI module. See pages 5-63 and 5-65.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

CDP (Dual-Pulse Reversible Counter)

The dual-pulse reversible counter CDP has up and down pulse inputs, so that three inputs are required. The circuit for a dual-pulse reversible counter must be programmed in the following order: preset input, up-pulse input, down-pulse input, the CDP instruction, and a counter number C0 through C255, followed by a counter preset value from 0 to 65535.

The preset value can be designated using a decimal constant or a data register. When a data register is used, the data of the data register becomes the preset value.

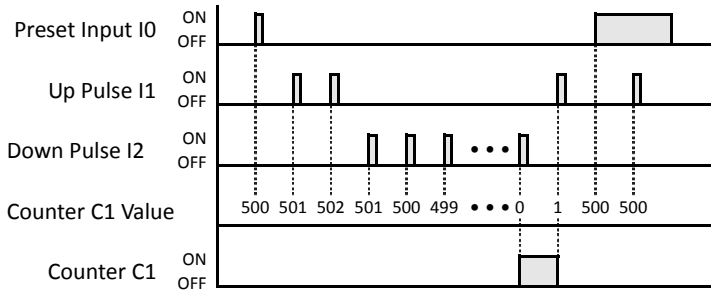
Ladder Diagram



Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
CDP	C1
	500
LOD	I3
AND	C1
OUT	Q1

Timing Chart



Caution

- For restrictions on ladder programming of counter instructions, see page 7-32.

Counter Operation after Count out

Condition	Counter Output
When the counter has counted out, either the current value or preset value is changed.	The counter maintains the counted out status.
Before the counter has counted out, the current value is changed to a larger value than the preset.	The counter output is turned on.
The preset value is changed to 0.	The counter output is turned on without regard to the current value.
When the reset value is on, the preset value is changed to 0.	The counter output is not turned on.

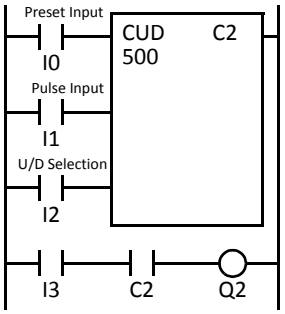
- The same counter number cannot be programmed more than once.
- The preset input must be turned on initially so that the current value returns to the preset value.
- The preset input must be turned off before counting may begin.
- When the up pulse and down pulses are on simultaneously, no pulse is counted.
- The counter output is on only when the current value is 0.
- After the current value reaches 0 (counting down), it changes to 65535 on the next count down.
- After the current value reaches 65535 (counting up), it changes to 0 on the next count up.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using the Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. Change the current value while the counter preset input is off.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18. Preset values can also be changed and changed preset values can be confirmed using the HMI module. See pages 5-63 and 5-65.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

CUD (Up/Down Selection Reversible Counter)

The up/down selection reversible counter CUD has a selection input to switch the up/down gate, so that three inputs are required. The circuit for an up/down selection reversible counter must be programmed in the following order: preset input, pulse input, up/down selection input, the CUD instruction, and a counter number C0 through C255, followed by a counter preset value from 0 to 65535.

The preset value can be designated using a decimal constant or a data register. When a data register is used, the data of the data register becomes the preset value.

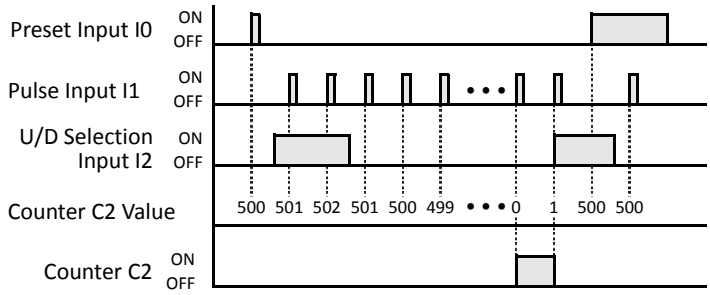
Ladder Diagram



Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
CUD	C2
	500
LOD	I3
AND	C2
OUT	Q2

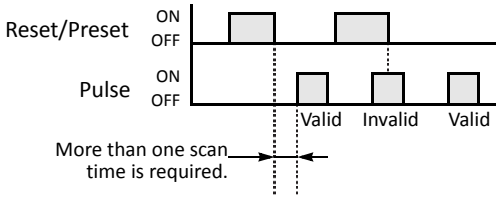
Timing Chart



- The same counter number cannot be programmed more than once.
- The preset input must be turned on initially so that the current value returns to the preset value.
- The preset input must be turned off before counting may begin.
- The up mode is selected when the up/down selection input is on.
- The down mode is selected when the up/down selection input is off.
- The counter output is on only when the current value is 0.
- After the current value reaches 0 (counting down), it changes to 65535 on the next count down.
- After the current value reaches 65535 (counting up), it changes to 0 on the next count up.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using the Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. Change the current value while the counter preset input is off.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18. Preset values can also be changed and changed preset values can be confirmed using the HMI module. See pages 5-63 and 5-65.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

Valid Pulse Inputs

The reset or preset input has priority over the pulse input. One scan after the reset or preset input has changed from on to off, the counter starts counting the pulse inputs as they change from off to on.



Caution

- For restrictions on ladder programming of counter instructions, see page 7-32.

CNTD, CDPD, and CUDD (Double-Word Counter)

Three types of double-word counters are available; adding (up) counter CNTD, dual-pulse reversible counter CDPD, and up/down selection reversible counter CUDD. A total of 128 double-word counters can be programmed in a user program for any type of CPU module. Each double-word counter uses 2 consecutive devices starting with the allocated device, which can be C0 through C254. Once used in a user program, counters cannot be used in any other counter instructions.

These instructions are available on upgraded CPU modules with system program version 200 or higher.

Counter	Device Address	Preset Value
CNTD (double-word adding counter)	C0 to C254	Constant: 0 to 4294967295 Data registers: D0 to D1998 D2000 to D7998 D10000 to D49998
CDPD (double-word dual-pulse reversible counter)	C0 to C254	
CUDD (double-word up/down selection reversible counter)	C0 to C254	

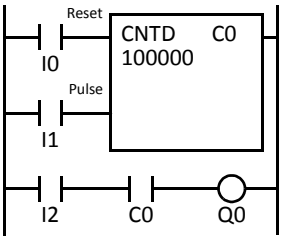
The valid device range depends on the CPU module type. For details, see pages 6-1 and 6-2.
The preset value can be 0 through 4,294,967,295 and designated using a constant or a data register. If a data register is designated as the preset value, two consecutive data registers are used.

CNTD (Double-Word Adding Counter)

When double-word adding counter instructions are programmed, two addresses are required. The circuit for a double-word adding (UP) counter must be programmed in the following order: reset input, pulse input, the CNTD instruction, and a counter number C0 through C254, followed by a counter preset value from 0 to 4,294,967,295.

The preset value can be designated using a constant or a data register. When a data register is used, the double-word data of two consecutive data registers becomes the preset value. For 32-bit data storage setting, see page 5-48.

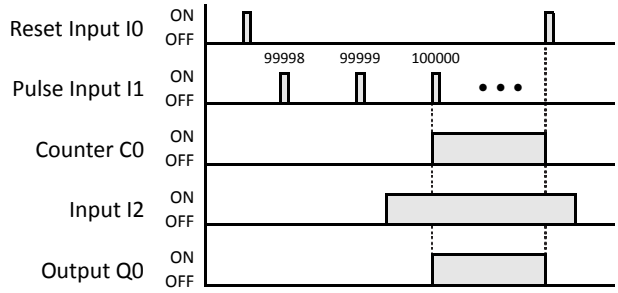
Ladder Diagram



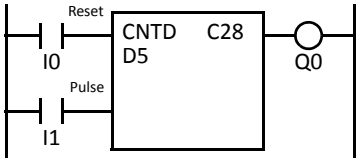
Program List

Instruction	Data
LOD	I0
LOD	I1
CNTD	C0
	100000
LOD	I2
AND	C0
OUT	Q0

Timing Chart



- The preset value 0 through 4,294,967,295 can be designated using a data register D0 through D1998 (all CPU modules) or D2000 through D7998 and D10000 through D49998 (slim type CPU modules); then the data of the data registers becomes the preset value. Directly after the CNTD instruction, the OUT, OUTN, SET, RST, TML, TIM, TMH, TMS, TMLO, TIMO, TMHO, or TMSO instruction can be programmed.



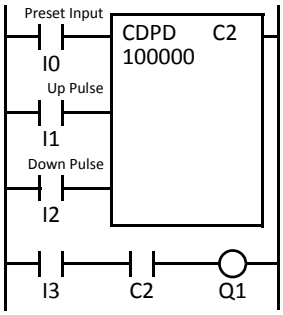
- Double-word counter instructions use two consecutive counters, and counters cannot be used more than once in a user program.
- While the reset input is off, the counter counts the leading edges of pulse inputs and compares them with the preset value.
- When the current value reaches the preset value, the counter turns output on. The output stays on until the reset input is turned on.
- When the reset input changes from off to on, the current value is reset.
- When the reset input is on, all pulse inputs are ignored.
- The reset input must be turned off before counting may begin.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. To change a counter preset value, select DEC(D) in the pull-down list box.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

CDPD (Double-Word Dual-Pulse Reversible Counter)

The double-word dual-pulse reversible counter CDPD has up and down pulse inputs, so that three inputs are required. The circuit for a double-word dual-pulse reversible counter must be programmed in the following order: preset input, up-pulse input, down-pulse input, the CDPD instruction, and a counter number C0 through C254, followed by a counter preset value from 0 to 4,294,967,295.

The preset value can be designated using a constant or a data register. When a data register is used, the double-word data of two consecutive data registers becomes the preset value. For 32-bit data storage setting, see page 5-48.

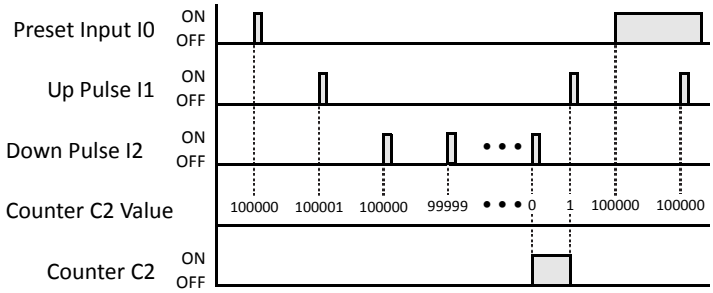
Ladder Diagram



Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
CDPD	C2
	100000
LOD	I3
AND	C2
OUT	Q1

Timing Chart



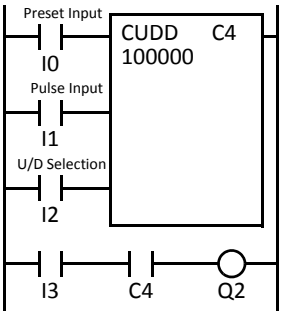
- Double-word counter instructions use two consecutive counters, and counters cannot be used more than once in a user program.
- The preset input must be turned on initially so that the current value returns to the preset value.
- The preset input must be turned off before counting may begin.
- When the up pulse and down pulses are on simultaneously, no pulse is counted.
- The counter output is on only when the current value is 0.
- After the current value reaches 0 (counting down), it changes to 4,294,967,295 on the next count down.
- After the current value reaches 4,294,967,295 (counting up), it changes to 0 on the next count up.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using the Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. To change a counter preset value, select DEC(D) in the pull-down list box.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

CUDD (Double-Word Up/Down Selection Reversible Counter)

The double-word up/down selection reversible counter CUDD has a selection input to switch the up/down gate, so that three inputs are required. The circuit for a double-word up/down selection reversible counter must be programmed in the following order: preset input, pulse input, up/down selection input, the CUDD instruction, and a counter number C0 through C254, followed by a counter preset value from 0 to 4,294,967,295.

The preset value can be designated using a constant or a data register. When a data register is used, the double-word data of two consecutive data registers becomes the preset value. For 32-bit data storage setting, see page 5-48.

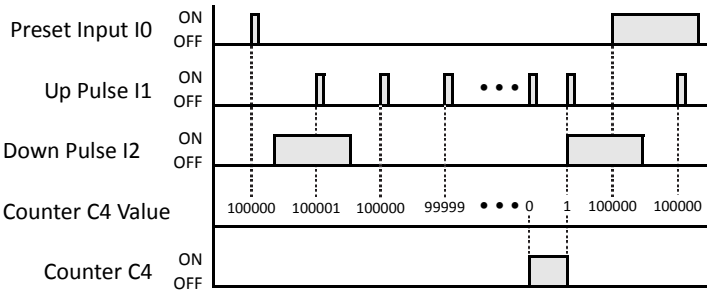
Ladder Diagram



Program List

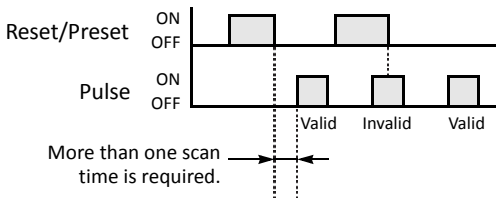
Instruction	Data
LOD	I0
LOD	I1
LOD	I2
CUDD	C4
	100000
LOD	I3
AND	C4
OUT	Q2

Timing Chart



Valid Pulse Inputs

The reset or preset input has priority over the pulse input. One scan after the reset or preset input has changed from on to off, the counter starts counting the pulse inputs as they change from off to on.

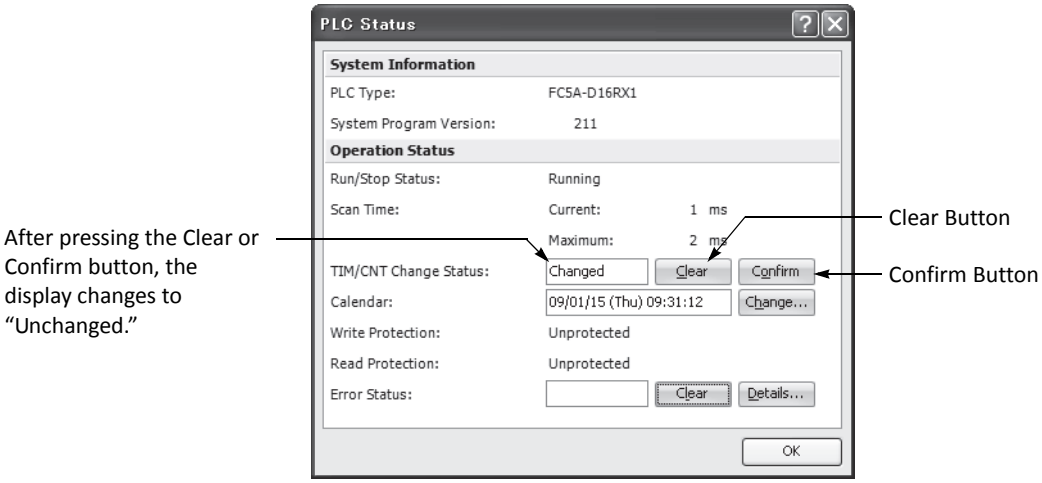


- Double-word counter instructions use two consecutive counters, and counters cannot be used more than once in a user program.
- The preset input must be turned on initially so that the current value returns to the preset value.
- The preset input must be turned off before counting may begin.
- The up mode is selected when the up/down selection input is on.
- The down mode is selected when the up/down selection input is off.
- The counter output is on only when the current value is 0.
- After the current value reaches 0 (counting down), it changes to 4,294,967,295 on the next count down.
- After the current value reaches 4,294,967,295 (counting up), it changes to 0 on the next count up.
- When power is off, the counter's current value is held, and can also be designated as "clear" type counters using the Function Area Settings (see page 5-5).
- Counter preset and current values can be changed using WindLDR without downloading the entire program to the CPU again. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Custom** > **New Custom Monitor**. To change a counter preset value, select DEC(D) in the pull-down list box.
- When the preset or current value is changed during counter operation, the change becomes effective immediately.
- For the data movement when changing, confirming, and clearing preset values, see page 7-18.
- WindLDR ladder diagrams show CP (counter preset value) and CC (counter current value) in advanced instruction devices.

Changing, Confirming, and Clearing Preset Values for Timers and Counters

Preset values for timers and counters can be changed by selecting **Online > Monitor** > **Monitor**, followed by **Online** > **Custom > New Custom Monitor** on WindLDR for transferring a new value to the MicroSmart CPU module RAM as described on preceding pages. After changing the preset values temporarily, the changes can be written to the user program in the MicroSmart CPU module EEPROM or cleared from the RAM.

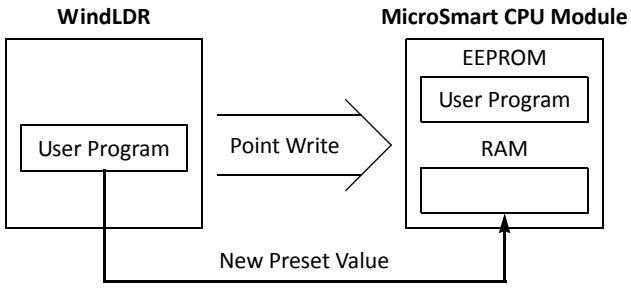
To access the PLC Status dialog box from the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**, then **Online** > **Status**.



Data movement when changing a timer/counter preset value

When changing a timer/counter preset value using Point Write on WindLDR, the new preset value is written to the MicroSmart CPU module RAM. The user program and preset values in the EEPROM are not changed.

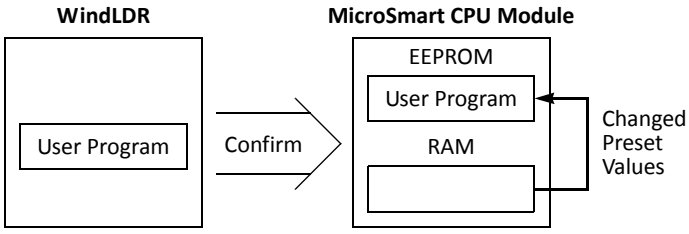
Note: The HMI module can also be used to change preset values and confirm changed preset values. See pages 5-63 and 5-65.



Data movement when confirming changed preset values

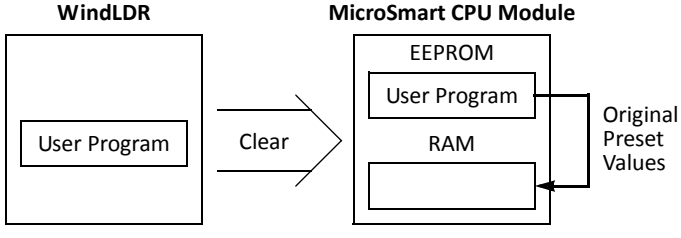
When the Confirm button is pressed before pressing the Clear button, the changed timer/counter preset values in the MicroSmart CPU module RAM are written to the EEPROM.

When uploading the user program after confirming, the user program with changed preset values is uploaded from the MicroSmart CPU module EEPROM to WindLDR.



Data movement when clearing changed preset values to restore original values

Changing preset values for timers and counters in the MicroSmart CPU module RAM does not automatically update preset values in the user memory, EEPROM. This is useful for restoring original preset values. When the Clear button is pressed before pressing the Confirm button, the changed timer/counter preset values are cleared from the RAM and the original preset values are loaded from the EEPROM to the RAM.



CC= and CC≥ (Counter Comparison)

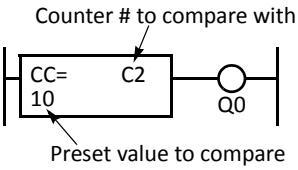
The CC= instruction is an equivalent comparison instruction for counter current values. This instruction will constantly compare current values to the value that has been programmed in. When the counter value equals the given value, the desired output will be initiated.

The CC≥ instruction is an equal to or greater than comparison instruction for counter current values. This instruction will constantly compare current values to the value that has been programmed in. When the counter value is equal to or greater than the given value, the desired output will be initiated.

When a counter comparison instruction is programmed, two addresses are required. The circuit for a counter comparison instruction must be programmed in the following order: the CC= or CC≥ instruction; a counter number C0 through C255, followed by a preset value to compare from 0 to 65535.

The preset value can be designated using a decimal constant or a data register D0 through D1999 (all CPU modules) or D2000 through D7999 and D10000 through D49999 (slim type CPU modules). When a data register is used, the data of the data register becomes the preset value.

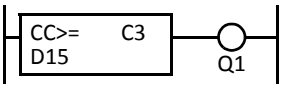
Ladder Diagram (CC=)



Program List

Instruction	Data
CC=	C2
	10
OUT	Q0

Ladder Diagram (CC≥)

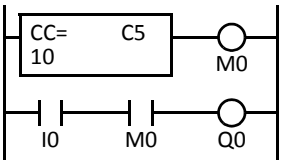


Program List

Instruction	Data
CC>=	C3
	D15
OUT	Q1

- The CC= and CC≥ instructions can be used repeatedly for different preset values.
- The comparison instructions only compare the current value. The status of the counter does not affect this function.
- The comparison instructions also serve as an implicit LOD instruction.
- The comparison instructions can be used with internal relays, which are ANDed or ORed at a separate program address.
- Like the LOD instruction, the comparison instructions can be followed by the AND and OR instructions.

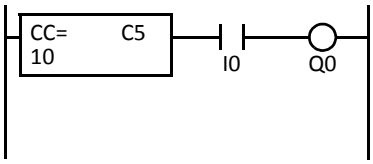
Ladder Diagram



Program List

Instruction	Data
CC=	C5
	10
OUT	M0
LOD	I0
AND	M0
OUT	Q0

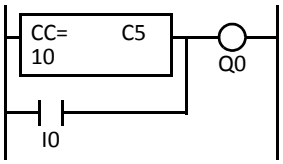
Ladder Diagram



Program List

Instruction	Data
CC=	C5
	10
AND	I0
OUT	Q0

Ladder Diagram

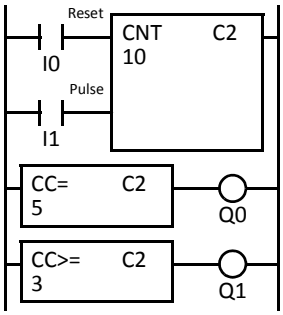


Program List

Instruction	Data
CC=	C5
	10
OR	I0
OUT	Q0

Examples: CC= and CC≥ (Counter Comparison)

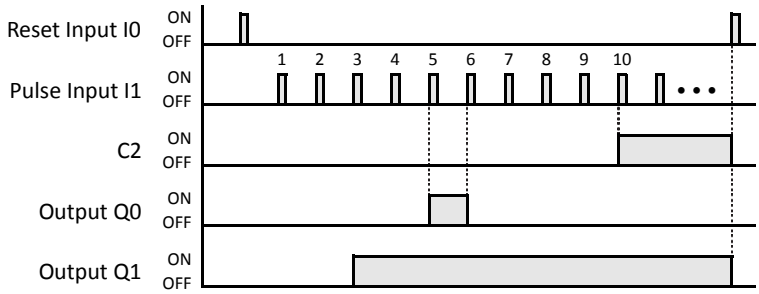
Ladder Diagram 1



Program List

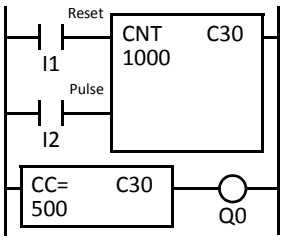
Instruction	Data
LOD	I0
LOD	I1
CNT	C2
	10
CC=	C2
	5
OUT	Q0
CC≥	C2
	3
OUT	Q1

Timing Chart



Output Q0 is on when counter C2 current value is 5.
Output Q1 is turned on when counter C2 current value reaches 3 and remains on until counter C2 is reset.

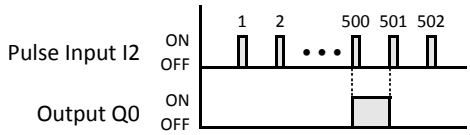
Ladder Diagram 2



Program List

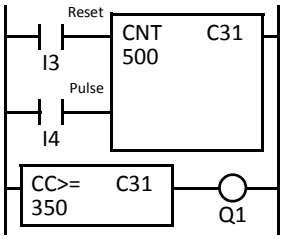
Instruction	Data
LOD	I1
LOD	I2
CNT	C30
	1000
CC=	C30
	500
OUT	Q0

Timing Chart



Output Q0 is on when counter C30 current value is 500.

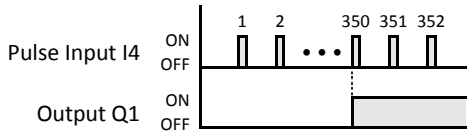
Ladder Diagram 3



Program List

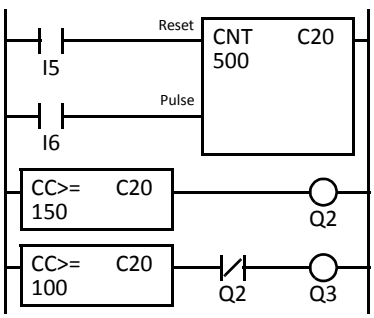
Instruction	Data
LOD	I3
LOD	I4
CNT	C31
	500
CC>=	C31
	350
OUT	Q1

Timing Chart



Output Q1 is turned on when counter C31 current value reaches 350 and remains on until counter C31 is reset.

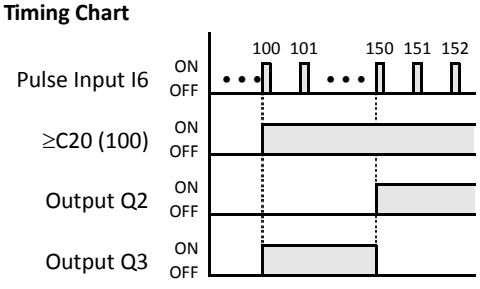
Ladder Diagram 4



Program List

Instruction	Data
LOD	I5
LOD	I6
CNT	C20
	500
CC>=	C20
	150
OUT	Q2
CC>=	C20
	100
ANDN	Q2
OUT	Q3

Timing Chart



Output Q3 is on when counter C20 current value is between 100 and 149.

DC= and DC≥ (Data Register Comparison)

The DC= instruction is an equivalent comparison instruction for data register values. This instruction will constantly compare data register values to the value that has been programmed in. When the data register value equals the given value, the desired output will be initiated.

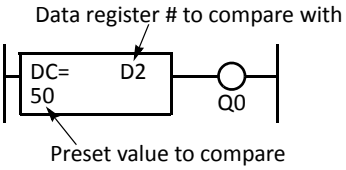
The DC≥ instruction is an equal to or greater than comparison instruction for data register values. This instruction will constantly compare data register values to the value that has been programmed in. When the data register value is equal to or greater than the given value, the desired output will be initiated.

When a data register comparison instruction is programmed, two addresses are required. The circuit for a data register comparison instruction must be programmed in the following order: the DC= or DC≥ instruction, a data register number D0 through D1999 (all CPU modules) or D2000 through D7999 and D10000 through D49999 (slim type CPU modules), followed by a preset value to compare from 0 to 65535.

The preset value can be designated using a decimal constant or a data register D0 through D1999 (all CPU modules) or D2000 through D7999 and D10000 through D49999 (slim type CPU modules). When a data register is used, the data of the data register becomes the preset value.

For LC (Load Compare) instructions, see page 4-8 (Advanced Vol.).

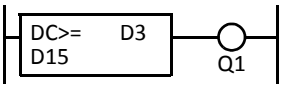
Ladder Diagram (DC=)



Program List

Instruction	Data
DC=	D2
	50
OUT	Q0

Ladder Diagram (DC≥)

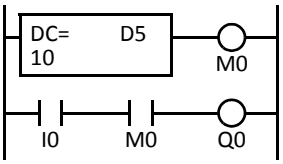


Program List

Instruction	Data
DC>=	D3
	D15
OUT	Q1

- The DC= and DC≥ instructions can be used repeatedly for different preset values.
- The comparison instructions also serve as an implicit LOD instruction.
- The comparison instructions can be used with internal relays, which are ANDed or ORed at a separate program address.
- Like the LOD instruction, the comparison instructions can be followed by the AND and OR instructions.

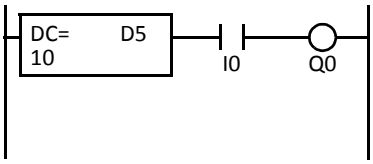
Ladder Diagram



Program List

Instruction	Data
DC=	D5
	10
OUT	M0
LOD	I0
AND	M0
OUT	Q0

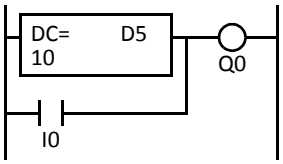
Ladder Diagram



Program List

Instruction	Data
DC=	D5
	10
AND	I0
OUT	Q0

Ladder Diagram

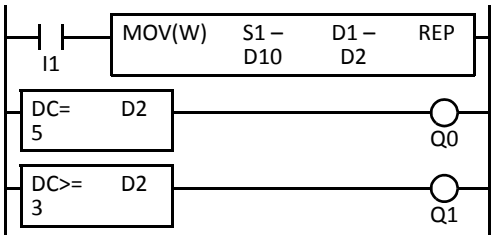


Program List

Instruction	Data
DC=	D5
	10
OR	I0
OUT	Q0

Examples: DC= and DC≥ (Data Register Comparison)

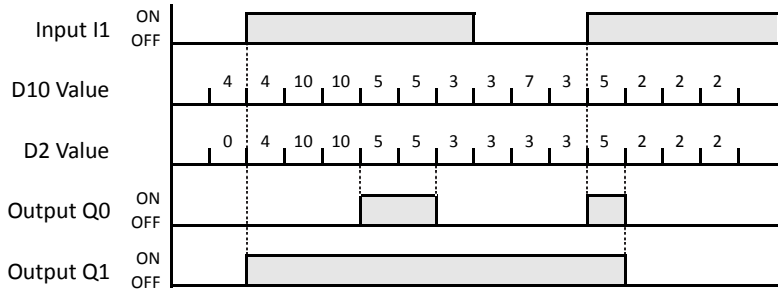
Ladder Diagram 1



Program List

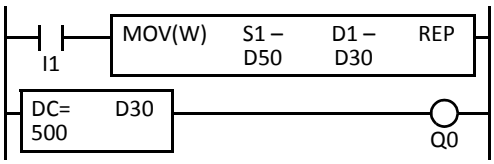
Instruction	Data
LOD	I1
MOV(W)	
	D10 –
	D2 –
DC=	D2
	5
OUT	Q0
DC≥	D2
	3
OUT	Q1

Timing Chart

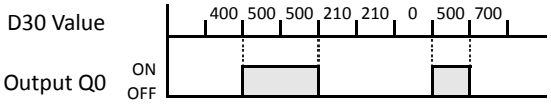


Output Q0 is on when data register D2 value is 5.
Output Q1 is on when data register D2 value is 3 or more.

Ladder Diagram 2

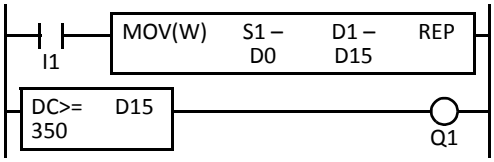


Timing Chart

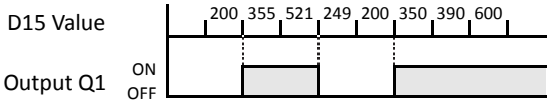


Output Q0 is on when data register D30 value is 500.

Ladder Diagram 3

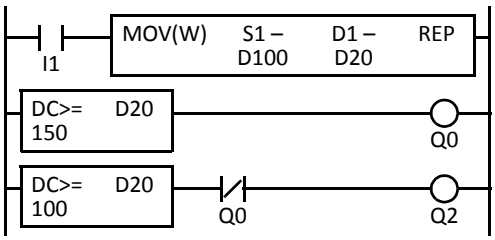


Timing Chart

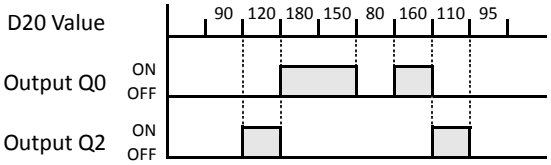


Output Q1 is on when data register D15 value is 350 or more.

Ladder Diagram 4



Timing Chart



Output Q2 is on while data register D20 value is between 149 and 100.

SFR and SFRN (Forward and Reverse Shift Register)

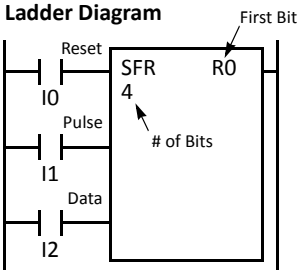
All-in-one type CPU modules have a shift register consisting of 128 bits which are allocated to R0 through R127. Slim type CPU modules have a shift register consisting of 256 bits which are allocated to R0 through R255. Any number of available bits can be selected to form a train of bits which store on or off status. The on/off data of constituent bits is shifted in the forward direction (forward shift register) or in the reverse direction (reverse shift register) when a pulse input is turned on.

Forward Shift Register (SFR)

When SFR instructions are programmed, two addresses are always required. The SFR instruction is entered, followed by a shift register number selected from appropriate device addresses. The shift register number corresponds to the first, or head bit. The number of bits is the second required address after the SFR instruction.

The SFR instruction requires three inputs. The forward shift register circuit must be programmed in the following order: reset input, pulse input, data input, and the SFR instruction, followed by the first bit and the number of bits.

Ladder Diagram

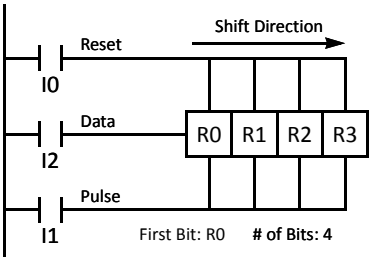


CPU Type	All-in-One CPU	Slim CPU
First Bit	R0 to R127	R0 to R255
# of Bits	1 to 128	1 to 256

Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
SFR	R0
	4

Structural Diagram



Reset Input

The reset input will cause the value of each bit of the shift register to return to zero. Initialize pulse special internal relay, M8120, may be used to initialize the shift register at start-up.

Pulse Input

The pulse input triggers the data to shift. The shift is in the forward direction for a forward shift register and in reverse for a reverse shift register. A data shift will occur upon the leading edge of a pulse; that is, when the pulse *turns on*. If the pulse has been on and stays on, no data shift will occur.

Data Input

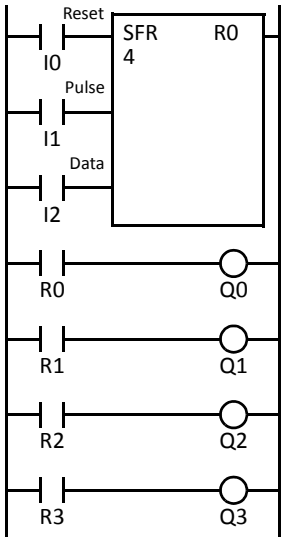
The data input is the information which is shifted into the first bit when a forward data shift occurs, or into the last bit when a reverse data shift occurs.

Note: When power is turned off, the statuses of all shift register bits are normally cleared. It is also possible to maintain the statuses of shift register bits by using the Function Area Settings as required. See page 5-5.

Caution • For restrictions on ladder programming of shift register instructions, see page 7-32.

Forward Shift Register (SFR), continued

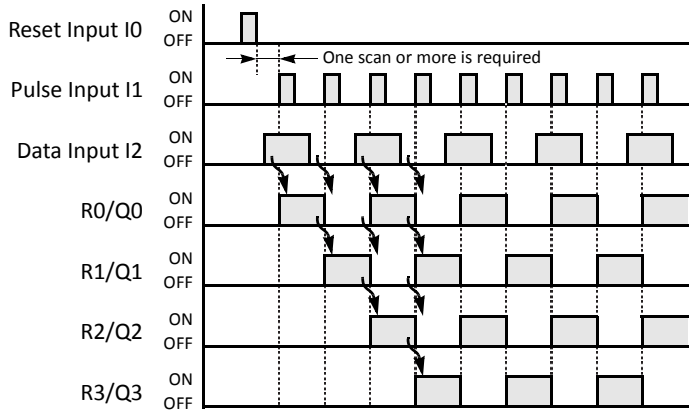
Ladder Diagram



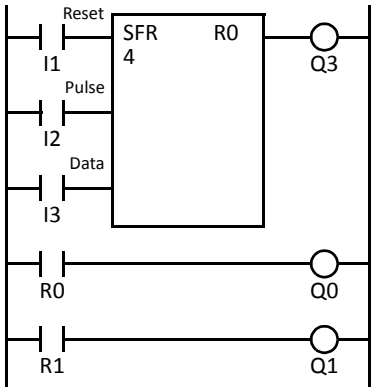
Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
SFR	R0
	4
LOD	R0
OUT	Q0
LOD	R1
OUT	Q1
LOD	R2
OUT	Q2
LOD	R3
OUT	Q3

Timing Chart



Ladder Diagram

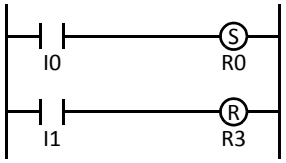


Program List

Instruction	Data
LOD	I1
LOD	I2
LOD	I3
SFR	R0
	4
OUT	Q3
LOD	R0
OUT	Q0
LOD	R1
OUT	Q1

- The last bit status output can be programmed directly after the SFR instruction. In this example, the status of bit R3 is read to output Q3.
- Each bit can be loaded using the LOD R# instruction.

Setting and Resetting Shift Register Bits



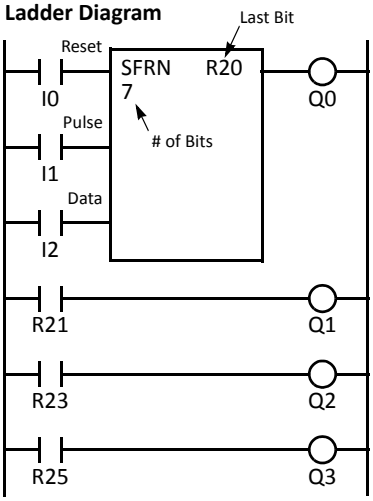
- Any shift register bit can be turned on using the SET instruction.
- Any shift register bit can be turned off using the RST instruction.
- The SET or RST instruction is actuated by any input condition.

Reverse Shift Register (SFRN)

For reverse shifting, use the SFRN instruction. When SFRN instructions are programmed, two addresses are always required. The SFRN instructions are entered, followed by a shift register number selected from appropriate device addresses. The shift register number corresponds to the lowest bit number in a string. The number of bits is the second required address after the SFRN instructions.

The SFRN instruction requires three inputs. The reverse shift register circuit must be programmed in the following order: reset input, pulse input, data input, and the SFRN instruction, followed by the last bit and the number of bits.

Ladder Diagram



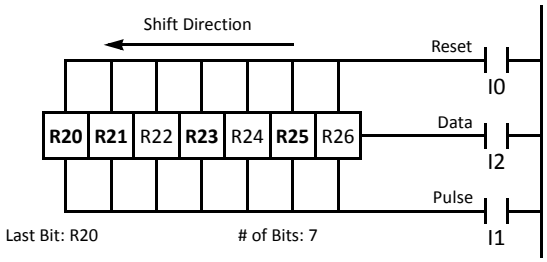
CPU Type	All-in-One CPU	Slim CPU
Last Bit	R0 to R127	R0 to R255
# of Bits	1 to 128	1 to 256

Program List

Instruction	Data
LOD	I0
LOD	I1
LOD	I2
SFRN	R20
	7
OUT	Q0
LOD	R21
OUT	Q1
LOD	R23
OUT	Q2
LOD	R25
OUT	Q3

- The last bit status output can be programmed directly after the SFRN instruction. In this example, the status of bit R20 is read to output Q0.
- Each bit can be loaded using the LOD R# instructions.
- For details of reset, pulse, and data inputs, see page 7-23.

Structural Diagram



Note: Output is initiated only for those bits highlighted in bold print.

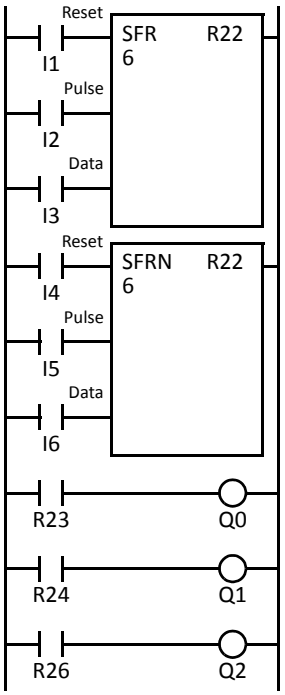
Note: When power is turned off, the statuses of all shift register bits are normally cleared. It is also possible to maintain the statuses of shift register bits by using the Function Area Settings as required. See page 5-5.

Caution • For restrictions on ladder programming of shift register instructions, see page 7-32.

Bidirectional Shift Register

A bidirectional shift register can be created by first programming the SFR instruction as detailed in the Forward Shift Register section on page 7-23. Next, the SFRN instruction is programed as detailed in the Reverse Shift Register section on page 7-25.

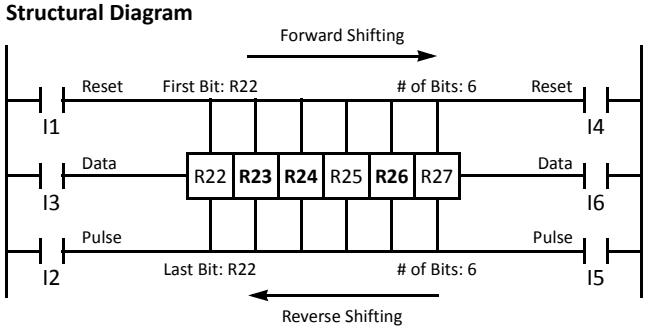
Ladder Diagram



Program List

Instruction	Data
LOD	I1
LOD	I2
LOD	I3
SFR	R22
	6
LOD	I4
LOD	I5
LOD	I6
SFRN	R22
	6
LOD	R23
OUT	Q0
LOD	R24
OUT	Q1
LOD	R26
OUT	Q2

Structural Diagram



Note: Output is initiated only for those bits highlighted in bold print.

SOTU and SOTD (Single Output Up and Down)

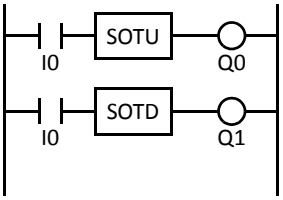
The SOTU instruction "looks for" the transition of a given input from off to on. The SOTD instruction looks for the transition of a given input from on to off. When this transition occurs, the desired output will turn on for the length of one scan. The SOTU or SOTD instruction converts an input signal to a "one-shot" pulse signal.

A total of 3072 SOTU and SOTD instructions can be used in a user program.

If operation is started while the given input is already on, the SOTU output will not turn on. The transition from off to on is what triggers the SOTU instruction.

When a relay of the CPU or relay output module is defined as the SOTU or SOTD output, it may not operate if the scan time is not compatible with relay requirements.

Ladder Diagram



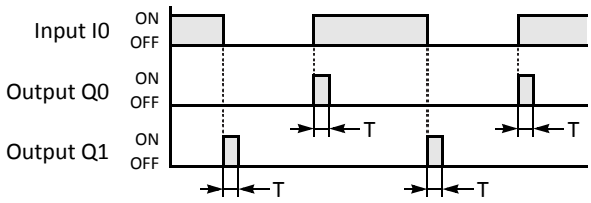
Program List

Instruction	Data
LOD	I0
SOTU	
OUT	Q0
LOD	I0
SOTD	
OUT	Q1

Caution

- For restrictions on ladder programming of SOTU and SOTD instructions, see page 7-32.

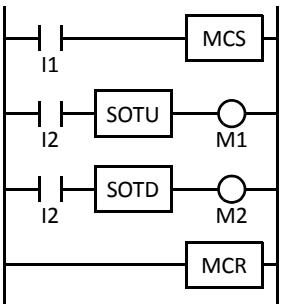
Timing Chart



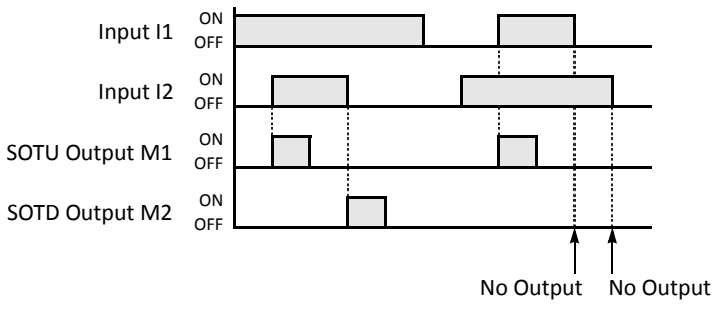
Note: "T" equals one scan time (one-shot pulse).

There is a special case when the SOTU and SOTD instructions are used between the MCS and MCR instructions (which are detailed on page 7-28). If input I2 to the SOTU instruction turns on while input I1 to the MCS instruction is on, then the SOTU output turns on. If input I2 to the SOTD instruction turns off while input I1 is on, then the SOTD output turns on. If input I1 turns on while input I2 is on, then the SOTU output turns on. However, if input I1 turns off while input I2 is on, then the SOTD output does not turn on as shown below.

Ladder Diagram



Timing Chart



MCS and MCR (Master Control Set and Reset)

The MCS (master control set) instruction is usually used in combination with the MCR (master control reset) instruction. The MCS instruction can also be used with the END instruction, instead of the MCR instruction.

When the input preceding the MCS instruction is off, the MCS is executed so that all inputs to the portion between the MCS and the MCR are forced off. When the input preceding the MCS instruction is on, the MCS is not executed so that the program following it is executed according to the actual input statuses.

When the input condition to the MCS instruction is off and the MCS is executed, other instructions between the MCS and MCR are executed as follows:

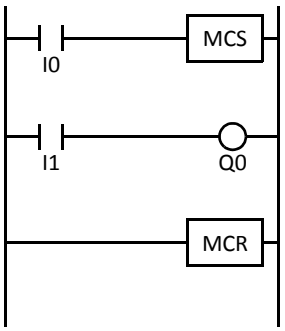
Instruction	Status
SOTU	Rising edges (ON pulses) are not detected.
SOTD	Falling edges (OFF pulses) are not detected.
OUT	All are turned off.
OUTN	All are turned on.
SET and RST	All are held in current status.
TML, TIM, TMH, and TMS	Current values are reset to zero. Timeout statuses are turned off.
CNT, CDP, and CUD	Current values are held. Pulse inputs are turned off. Countout statuses are turned off.
SFR and SFRN	Shift register bit statuses are held. Pulse inputs are turned off. The output from the last bit is turned off.

Input conditions cannot be set for the MCR instruction.

More than one MCS instruction can be used with one MCR instruction.

Corresponding MCS/MCR instructions cannot be nested within another pair of corresponding MCS/MCR instructions.

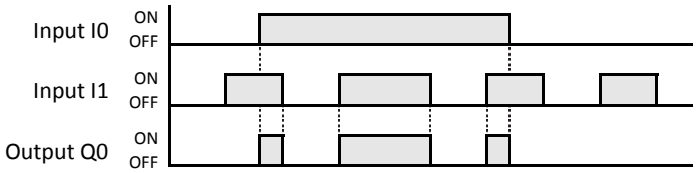
Ladder Diagram



Program List

Instruction	Data
LOD	I0
MCS	
LOD	I1
OUT	Q0
MCR	

Timing Chart



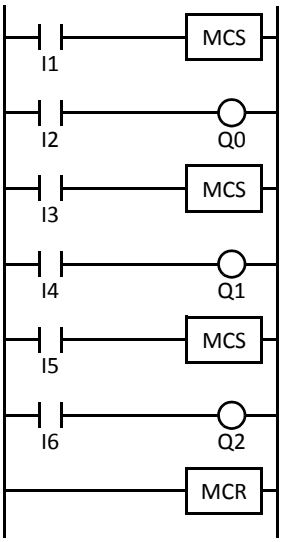
When input I0 is off, MCS is executed so that the subsequent input is forced off.

When input I0 is on, MCS is not executed so that the following program is executed according to the actual input statuses.

MCS and MCR (Master Control Set and Reset), continued

Multiple Usage of MCS instructions

Ladder Diagram



Program List

Instruction	Data
LOD	I1
MCS	
LOD	I2
OUT	Q0
LOD	I3
MCS	
LOD	I4
OUT	Q1
LOD	I5
MCS	
LOD	I6
OUT	Q2
MCR	

This master control circuit will give priority to I1, I3, and I5, in that order.

When input I1 is off, the first MCS is executed so that subsequent inputs I2 through I6 are forced off.

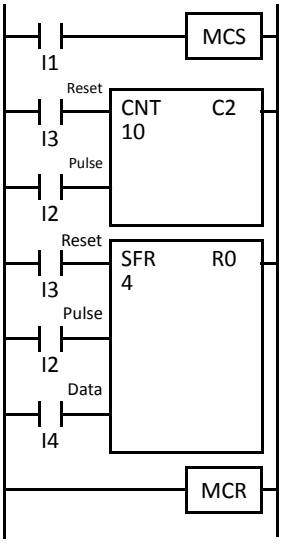
When input I1 is on, the first MCS is not executed so that the following program is executed according to the actual input statuses of I2 through I6.

When I1 is on and I3 is off, the second MCS is executed so that subsequent inputs I4 through I6 are forced off.

When both I1 and I3 are on, the first and second MCSs are not executed so that the following program is executed according to the actual input statuses of I4 through I6.

Counter and Shift Register in Master Control Circuit

Ladder Diagram

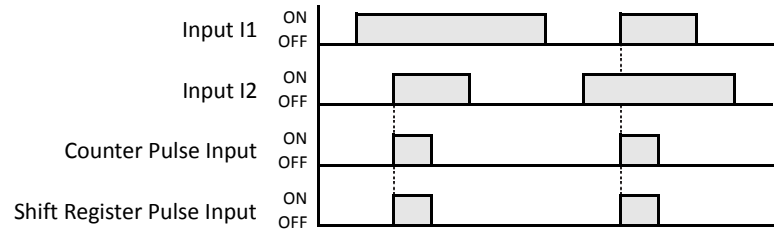


When input I1 is on, the MCS is not executed so that the counter and shift register are executed according to actual statuses of subsequent inputs I2 through I4.

When input I1 is off, the MCS is executed so that subsequent inputs I2 through I4 are forced off.

When input I1 is turned on while input I2 is on, the counter and shift register pulse inputs are turned on as shown below.

Timing Chart



JMP (Jump) and JEND (Jump End)

The JMP (jump) instruction is usually used in combination with the JEND (jump end) instruction. At the end of a program, the JMP instruction can also be used with the END instruction, instead of the JEND instruction.

These instructions are used to proceed through the portion of the program between the JMP and the JEND *without* processing. This is similar to the MCS/MCR instructions, except that the portion of the program between the MCS and MCR instruction *is* executed.

When the operation result immediately before the JMP instruction is on, the JMP is valid and the program is *not* executed. When the operation result immediately before the JMP instruction is off, the JMP is invalid and the program is executed.

When the input condition to the JMP instruction is on and the JMP is executed, other instructions between the JMP and JEND are executed as follows:

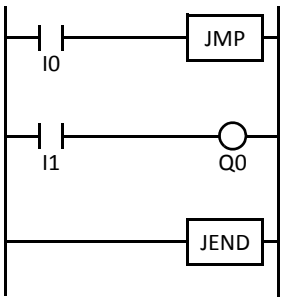
Instruction	Status
SOTU	Rising edges (ON pulses) are not detected.
SOTD	Falling edges (OFF pulses) are not detected.
OUT and OUTN	All are held in current status.
SET and RST	All are held in current status.
TML, TIM, TMH, and TMS	Current values are held. Timeout statuses are held.
CNT, CDP, and CUD	Current values are held. Pulse inputs are turned off. Countout statuses are held.
SFR and SFRN	Shift register bit statuses are held. Pulse inputs are turned off. The output from the last bit is held.

Input conditions cannot be set for the JEND instruction.

More than one JMP instruction can be used with one JEND instruction.

Corresponding JMP/JEND instructions cannot be nested within another pair of corresponding JMP/JEND instructions.

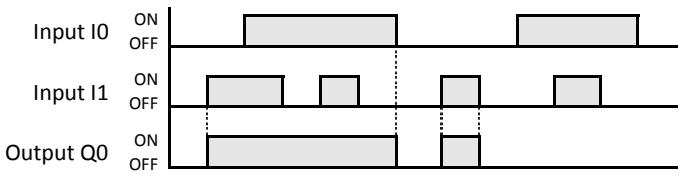
Ladder Diagram



Program List

Instruction	Data
LOD	I0
JMP	
LOD	I1
OUT	Q0
JEND	

Timing Chart

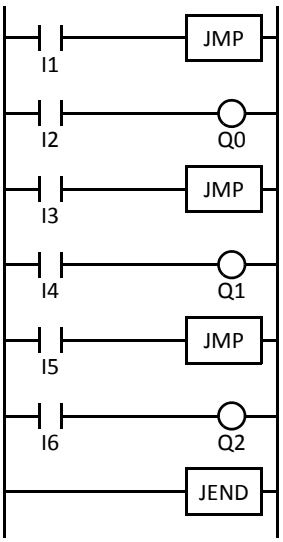


When input I0 is on, JMP is executed so that the subsequent output status is held.

When input I0 is off, JMP is not executed so that the following program is executed according to the actual input statuses.

JMP (Jump) and JEND (Jump End), continued

Ladder Diagram



Program List

Instruction	Data
LOD	I1
JMP	
LOD	I2
OUT	Q0
LOD	I3
JMP	
LOD	I4
OUT	Q1
LOD	I5
JMP	
LOD	I6
OUT	Q2
JEND	

This jump circuit will give priority to I1, I3, and I5, in that order.

When input I1 is on, the first JMP is executed so that subsequent output statuses of Q0 through Q2 are held.

When input I1 is off, the first JMP is not executed so that the following program is executed according to the actual input statuses of I2 through I6.

When I1 is off and I3 is on, the second JMP is executed so that subsequent output statuses of Q1 and Q2 are held.

When both I1 and I3 are off, the first and second JMPs are not executed so that the following program is executed according to the actual input statuses of I4 through I6.

END

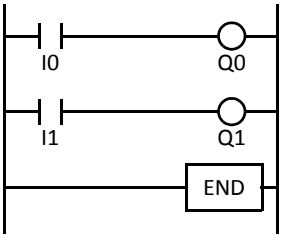
The END instruction is always required at the end of a program; however, it is not necessary to program the END instruction after the last programmed instruction. The END instruction already exists at every unused address. (When an address is used for programming, the END instruction is removed.)

A *scan* is the execution of all instructions from address zero to the END instruction. The time required for this execution is referred to as one *scan time*. The scan time varies with respect to program length, which corresponds to the address where the END instruction is found.

During the scan time, program instructions are processed sequentially. This is why the output instruction closest to the END instruction has priority over a previous instruction for the same output. No output is initiated until all logic within a scan is processed.

Output occurs simultaneously, and this is the first part of the END instruction execution. The second part of the END instruction execution is to monitor all inputs, also done simultaneously. Then program instructions are ready to be processed sequentially once again.

Ladder Diagram

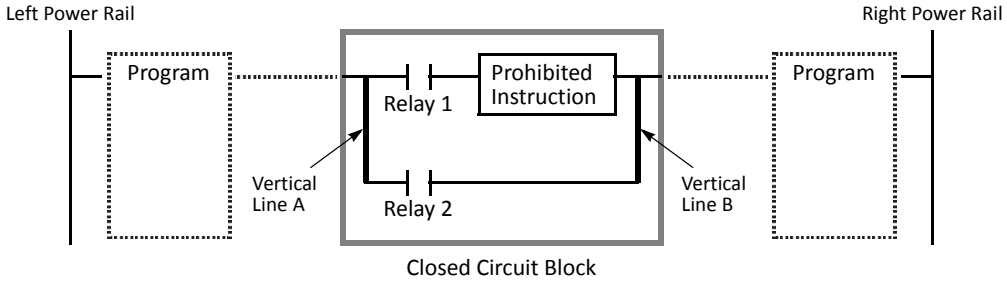


Program List

Instruction	Data
LOD	I0
OUT	Q0
LOD	I1
OUT	Q1
END	

Restriction on Ladder Programming

Due to the structure of WindLDR, the following ladder diagram cannot be programmed — a closed circuit block is formed by vertical lines, except for right and left power rails, and the closed circuit block contains one or more prohibited instructions shown in the table below.

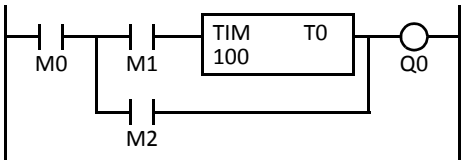


Prohibited Instructions	OUT, OUTN, SET, RST, TML, TIM, TMH, TMS, CNT, CDP, CUD, SFR, SFRN, SOTU, SOTD
Error Detection	When converting the ladder program, an error message is shown, such as "TIM follows an invalid device." Conversion fails to create mnemonics and the program is not downloaded to the CPU module.

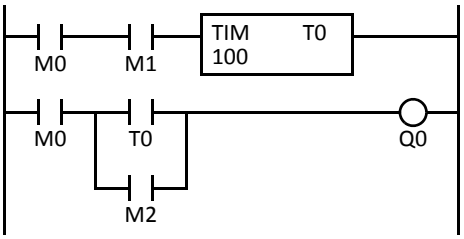
Modifying Prohibited Ladder Programs

Intended operation can be performed by modifying the prohibited ladder program as shown in the examples below:

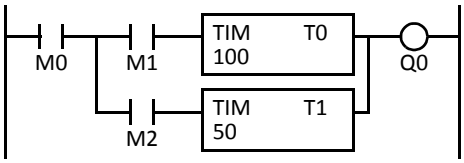
Prohibited Ladder Program 1



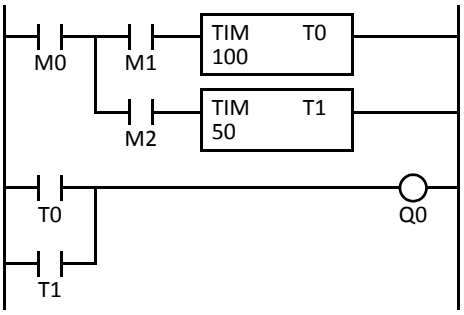
Modified Ladder Program 1



Prohibited Ladder Program 2



Modified Ladder Program 2



8: ADVANCED INSTRUCTIONS REFERENCE

Introduction

This chapter describes general rules of using advanced instructions, terms, data types, and formats used for advanced instructions.

Advanced Instruction List

Group	Symbol	Name	Valid Data Type					See Page
			W	I	D	L	F	
NOP	NOP	No Operation						8-10
Move	MOV	Move	X	X	X	X	X	Advanced Vol. 3-1
	MOVN	Move Not	X	X	X	X		Advanced Vol. 3-5
	IMOV	Indirect Move	X		X		X	Advanced Vol. 3-6
	IMOVN	Indirect Move Not	X		X			Advanced Vol. 3-8
	BMOV	Block Move	X					Advanced Vol. 3-9
	IBMV	Indirect Bit Move	X					Advanced Vol. 3-10
	IBMVN	Indirect Bit Move Not	X					Advanced Vol. 3-12
	NSET	N Data Set	X	X	X	X	X	Advanced Vol. 3-13
	NRS	N Data Repeat Set	X	X	X	X	X	Advanced Vol. 3-14
	XCHG	Exchange	X		X			Advanced Vol. 3-15
	TCCST	Timer/Counter Current Value Store	X		X			Advanced Vol. 3-16
Data Comparison	CMP=	Compare Equal To	X	X	X	X	X	Advanced Vol. 4-1
	CMP<>	Compare Unequal To	X	X	X	X	X	Advanced Vol. 4-1
	CMP<	Compare Less Than	X	X	X	X	X	Advanced Vol. 4-1
	CMP>	Compare Greater Than	X	X	X	X	X	Advanced Vol. 4-1
	CMP<=	Compare Less Than or Equal To	X	X	X	X	X	Advanced Vol. 4-1
	CMP>=	Compare Greater Than or Equal To	X	X	X	X	X	Advanced Vol. 4-2
	ICMP>=	Interval Compare Greater Than or Equal To	X	X	X	X	X	Advanced Vol. 4-6
	LC=	Load Compare Equal To	X	X	X	X	X	Advanced Vol. 4-8
	LC<>	Load Compare Unequal To	X	X	X	X	X	Advanced Vol. 4-8
	LC<	Load Compare Less Than	X	X	X	X	X	Advanced Vol. 4-8
	LC>	Load Compare Greater Than	X	X	X	X	X	Advanced Vol. 4-8
	LC<=	Load Compare Less Than or Equal To	X	X	X	X	X	Advanced Vol. 4-8
	LC>=	Load Compare Greater Than or Equal To	X	X	X	X	X	Advanced Vol. 4-8
Binary Arithmetic	ADD	Addition	X	X	X	X	X	Advanced Vol. 5-1
	SUB	Subtraction	X	X	X	X	X	Advanced Vol. 5-1
	MUL	Multiplication	X	X	X	X	X	Advanced Vol. 5-1
	DIV	Division	X	X	X	X	X	Advanced Vol. 5-1
	INC	Increment	X	X	X	X		Advanced Vol. 5-13
	DEC	Decrement	X	X	X	X		Advanced Vol. 5-13
	ROOT	Root	X		X		X	Advanced Vol. 5-15
	SUM	Sum (ADD)	X	X	X	X	X	Advanced Vol. 5-16
		Sum (XOR)	X					
	RNDM	Random	X					Advanced Vol. 5-19
Boolean Computation	ANDW	AND Word	X		X			Advanced Vol. 6-1
	ORW	OR Word	X		X			Advanced Vol. 6-1
	XORW	Exclusive OR Word	X		X			Advanced Vol. 6-1

Group	Symbol	Name	Valid Data Type					See Page
			W	I	D	L	F	
Shift and Rotate	SFTL	Shift Left						Advanced Vol. 7-1
	SFTR	Shift Right						Advanced Vol. 7-3
	BCDLS	BCD Left Shift			X			Advanced Vol. 7-5
	WSFT	Word Shift	X					Advanced Vol. 7-7
	ROTL	Rotate Left	X		X			Advanced Vol. 7-8
	ROTR	Rotate Right	X		X			Advanced Vol. 7-10
Data Conversion	HTOB	Hex to BCD	X		X			Advanced Vol. 8-1
	BTOH	BCD to Hex	X		X			Advanced Vol. 8-3
	HTOA	Hex to ASCII	X					Advanced Vol. 8-5
	ATOH	ASCII to Hex	X					Advanced Vol. 8-7
	BTOA	BCD to ASCII	X		X			Advanced Vol. 8-9
	ATOB	ASCII to BCD	X		X			Advanced Vol. 8-12
	ENCO	Encode						Advanced Vol. 8-15
	DECO	Decode						Advanced Vol. 8-16
	BCNT	Bit Count						Advanced Vol. 8-17
	ALT	Alternate Output						Advanced Vol. 8-18
	CVDT	Convert Data Type	X	X	X	X	X	Advanced Vol. 8-19
	DTDV	Data Divide	X					Advanced Vol. 8-21
	DTCB	Data Combine	X					Advanced Vol. 8-22
	SWAP	Data Swap	X		X			Advanced Vol. 8-23
Week Programmer	WKTIM	Week Timer						Advanced Vol. 9-1
	WKTBL	Week Table						Advanced Vol. 9-2
Interface	DISP	Display						Advanced Vol. 10-1
	DGRD	Digital Read						Advanced Vol. 10-3
User Communication	TXD1	Transmit 1						10-6
	TXD2	Transmit 2						10-6
	TXD3	Transmit 3						10-6
	TXD4	Transmit 4						10-6
	TXD5	Transmit 5						10-6
	TXD6	Transmit 6						10-6
	TXD7	Transmit 7						10-6
	RXD1	Receive 1						10-15
	RXD2	Receive 2						10-15
	RXD3	Receive 3						10-15
	RXD4	Receive 4						10-15
	RXD5	Receive 5						10-15
	RXD6	Receive 6						10-15
	RXD7	Receive 7						10-15
Program Branching	LABEL	Label						Advanced Vol. 11-1
	LJMP	Label Jump						Advanced Vol. 11-1
	LCAL	Label Call						Advanced Vol. 11-3
	LRET	Label Return						Advanced Vol. 11-3
	DJNZ	Decrement Jump Non-zero						Advanced Vol. 11-5
	DI	Disable Interrupt						Advanced Vol. 11-7
	EI	Enable Interrupt						Advanced Vol. 11-7
	IOREF	I/O Refresh						Advanced Vol. 11-9
	HSCRF	High-speed Counter Refresh						Advanced Vol. 11-11
	FRQRF	Frequency Measurement Refresh						Advanced Vol. 11-12
	COMRF	Communication Refresh						Advanced Vol. 11-13

Group	Symbol	Name	Valid Data Type					See Page
			W	I	D	L	F	
Coordinate Conversion	XYFS	XY Format Set	X	X				Advanced Vol. 12-1
	CVXTY	Convert X to Y	X	X				Advanced Vol. 12-2
	CVYTX	Convert Y to X	X	X				Advanced Vol. 12-3
	AVRG	Average	X	X	X	X	X	Advanced Vol. 12-7
Pulse	PULS1	Pulse Output 1						Advanced Vol. 13-2
	PULS2	Pulse Output 2						Advanced Vol. 13-2
	PULS3	Pulse Output 3						Advanced Vol. 13-2
	PWM1	Pulse Width Modulation 1						Advanced Vol. 13-8
	PWM2	Pulse Width Modulation 2						Advanced Vol. 13-8
	PWM3	Pulse Width Modulation 3						Advanced Vol. 13-8
	RAMP1	Ramp Pulse Output 1						Advanced Vol. 13-14
	RAMP2	Ramp Pulse Output 2						Advanced Vol. 13-14
	ZRN1	Zero Return 1						Advanced Vol. 13-26
	ZRN2	Zero Return 2						Advanced Vol. 13-26
	ZRN3	Zero Return 3						Advanced Vol. 13-26
PID Instruction	PID	PID Control	X	X				Advanced Vol. 14-1
Dual / Teaching Timer	DTML	1-sec Dual Timer						Advanced Vol. 15-1
	DTIM	100-ms Dual Timer						Advanced Vol. 15-1
	DTMH	10-ms Dual Timer						Advanced Vol. 15-1
	DTMS	1-ms Dual Timer						Advanced Vol. 15-1
	TTIM	Teaching Timer						Advanced Vol. 15-3
Intelligent Module Access	RUNA	Run Access	X	X				Advanced Vol. 16-2
	STPA	Stop Access	X	X				Advanced Vol. 16-4
Trigonometric Function	RAD	Degree to Radian					X	Advanced Vol. 17-1
	DEG	Radian to Degree					X	Advanced Vol. 17-2
	SIN	Sine					X	Advanced Vol. 17-3
	COS	Cosine					X	Advanced Vol. 17-4
	TAN	Tangent					X	Advanced Vol. 17-5
	ASIN	Arc Sine					X	Advanced Vol. 17-6
	ACOS	Arc Cosine					X	Advanced Vol. 17-7
	ATAN	Arc Tangent					X	Advanced Vol. 17-8
Logarithm / Power	LOGE	Natural Logarithm					X	Advanced Vol. 18-1
	LOG10	Common Logarithm					X	Advanced Vol. 18-2
	EXP	Exponent					X	Advanced Vol. 18-3
	POW	Power					X	Advanced Vol. 18-4
File Data Processing	FIFOF	FIFO Format	X					Advanced Vol. 19-1
	FIEX	First-In Execute	X					Advanced Vol. 19-3
	FOEX	First-Out Execute	X					Advanced Vol. 19-3
	NDSRC	N Data Search	X	X	X	X	X	Advanced Vol. 19-5
Clock	TADD	Time Addition						Advanced Vol. 20-1
	TSUB	Time Subtraction						Advanced Vol. 20-5
	HTOS	HMS to Sec						Advanced Vol. 20-9
	STOH	Sec to HMS						Advanced Vol. 20-10
	HOUR	Hour Meter						Advanced Vol. 20-11
Ethernet Instructions	EMAIL	Send E-mail						
	PING	Ping						
	ETXD	Transmit over Ethernet						
	ERXD	Receive over Ethernet						

Advanced Instruction Applicable CPU Modules

Applicable advanced instructions depend on the type of CPU modules as listed in the table below.

Group	Symbol	All-in-One Type CPU Modules			Slim Type CPU Modules	
		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E
NOP	NOP	X	X	X	X	X
Move	MOV	X	X	X	X	X
	MOVN	X	X	X	X	X
	IMOV	X	X	X	X	X
	IMOVN	X	X	X	X	X
	BMOV	X	X	X	X	X
	IBMV	X	X	X	X	X
	IBMVN	X	X	X	X	X
	NSET	X	X	X	X	X
	NRS	X	X	X	X	X
	XCHG	X	X	X	X	X
	TCCST	X	X	X	X	X
Data Comparison	CMP=	X	X	X	X	X
	CMP<>	X	X	X	X	X
	CMP<	X	X	X	X	X
	CMP>	X	X	X	X	X
	CMP<=	X	X	X	X	X
	CMP>=	X	X	X	X	X
	ICMP>=	X	X	X	X	X
	LC=	X	X	X	X	X
	LC<>	X	X	X	X	X
	LC<	X	X	X	X	X
	LC>	X	X	X	X	X
	LC<=	X	X	X	X	X
	LC>=	X	X	X	X	X
Binary Arithmetic	ADD	X	X	X	X	X
	SUB	X	X	X	X	X
	MUL	X	X	X	X	X
	DIV	X	X	X	X	X
	INC	X	X	X	X	X
	DEC	X	X	X	X	X
	ROOT	X	X	X	X	X
	SUM	X	X	X	X	X
	RNDM	X	X	X	X	X
Boolean Computation	ANDW	X	X	X	X	X
	ORW	X	X	X	X	X
	XORW	X	X	X	X	X
Shift and Rotate	SFTL	X	X	X	X	X
	SFTR	X	X	X	X	X
	BCDLS	X	X	X	X	X
	WSFT	X	X	X	X	X
	ROTL	X	X	X	X	X
	ROTR	X	X	X	X	X

Group	Symbol	All-in-One Type CPU Modules			Slim Type CPU Modules	
		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E
Data Conversion	HTOB	X	X	X	X	X
	BTOH	X	X	X	X	X
	HTOA	X	X	X	X	X
	ATOH	X	X	X	X	X
	BTOA	X	X	X	X	X
	ATOB	X	X	X	X	X
	ENCO	X	X	X	X	X
	DECO	X	X	X	X	X
	BCNT	X	X	X	X	X
	ALT	X	X	X	X	X
	CVDT	X	X	X	X	X
	DTDV	X	X	X	X	X
	DTCB	X	X	X	X	X
	SWAP	X	X	X	X	X
Week Programmer	WKTIM	X	X	X	X	X
	WKTBL	X	X	X	X	X
Interface	DISP			X	X	X
	DGRD			X	X	X
User Communication	TXD1	X	X	X	X	X (Note 1)
	TXD2	X	X	X	X	X
	TXD3			X (Note 2)	X	X
	TXD4			X (Note 2)	X	X
	TXD5			X (Note 2)	X	X
	TXD6				X	X
	TXD7				X	X
	RXD1	X	X	X	X	X (Note 1)
	RXD2	X	X	X	X	X
	RXD3			X (Note 2)	X	X
	RXD4			X (Note 2)	X	X
	RXD5			X (Note 2)	X	X
	RXD6				X	X
	RXD7				X	X
Program Branching	LABEL	X	X	X	X	X
	LJMP	X	X	X	X	X
	LCAL	X	X	X	X	X
	LRET	X	X	X	X	X
	DJNZ	X	X	X	X	X
	DI	X	X	X	X	X
	EI	X	X	X	X	X
	IOREF	X	X	X	X	X
	HSCRF	X	X	X	X	X
	FRQRF	X	X	X	X	X
	COMRF			X (Note 2)	X	X
Coordinate Conversion	XYFS	X	X	X	X	X
	CVXTY	X	X	X	X	X
	CVYTX	X	X	X	X	X
	AVRG	X	X	X	X	X

Note 1: Not available on FC5A-D12K1E/S1E.

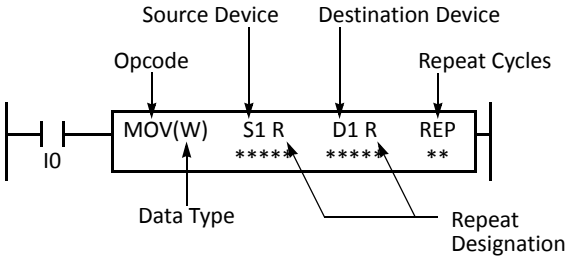
Note 2: Not available on FC5A-C24R2D.

Group	Symbol	All-in-One Type CPU Modules			Slim Type CPU Modules	
		FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D	FC5A-C24R2 FC5A-C24R2C FC5A-C24R2D	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E
Pulse	PULS1				X	X
	PULS2				X	X
	PULS3					X
	PWM1				X	X
	PWM2				X	X
	PWM3					X
	RAMP1				X	X
	RAMP2					X
	ZRN1				X	X
	ZRN2				X	X
	ZRN3					X
PID Instruction	PID			X	X	X
Dual / Teaching Timer	DTML	X	X	X	X	X
	DTIM	X	X	X	X	X
	DTMH	X	X	X	X	X
	DTMS	X	X	X	X	X
	TTIM	X	X	X	X	X
Intelligent Module Access	RUNA			X (Note 1)	X	X
	STPA			X (Note 1)	X	X
Trigonometric Function	RAD	X	X	X	X	X
	DEG	X	X	X	X	X
	SIN	X	X	X	X	X
	COS	X	X	X	X	X
	TAN	X	X	X	X	X
	ASIN	X	X	X	X	X
	ACOS	X	X	X	X	X
	ATAN	X	X	X	X	X
Logarithm / Power	LOGE	X	X	X	X	X
	LOG10	X	X	X	X	X
	EXP	X	X	X	X	X
	POW	X	X	X	X	X
File Data Processing	FIFOF	X	X	X	X	X
	FIEX	X	X	X	X	X
	FOEX	X	X	X	X	X
	NDSRC	X	X	X	X	X
Clock	TADD	X	X	X	X	X
	TSUB	X	X	X	X	X
	HTOS	X	X	X	X	X
	STOH	X	X	X	X	X
	HOUR	X	X	X	X	X
Ethernet Instructions	EMAIL					X (Note 2)
	PING					X (Note 2)
	ETXD					X (Note 2)
	ERXD					X (Note 2)

Note 1: Not available on FC5A-C24R2D.

Note 2: Ethernet instructions can only be used with FC5A-D12K1E and FC5A-D12S1E.

Structure of an Advanced Instruction



Repeat Designation
Specifies whether repeat is used for the device or not.

Repeat Cycles
Specifies the quantity of repeat cycles: 1 through 99.

Opcode
The opcode is a symbol to identify the advanced instruction.

Data Type
Specifies the word (W), integer (I), double word (D), long (L), or float (F) data type.

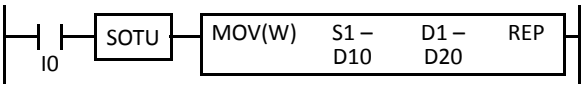
Source Device
The source device specifies the 16- or 32-bit data to be processed by the advanced instruction. Some advanced instructions require two source devices.

Destination Device
The destination device specifies the 16- or 32-bit data to store the result of the advanced instruction. Some advanced instructions require two destination devices.

Input Condition for Advanced Instructions

Almost all advanced instructions must be preceded by a contact, except NOP (no operation), LABEL (label), LRET (label return), and STPA (stop access) instructions. The input condition can be programmed using a bit device such as input, output, internal relay, or shift register. Timer and counter can also be used as an input condition to turn on the contact when the timer times out or the counter counts out.

While the input condition is on, the advanced instruction is executed in each scan. To execute the advanced instruction only at the rising or falling edge of the input, use the SOTU or SOTD instruction.



While the input condition is off, the advanced instruction is not executed and device statuses are held.

Source and Destination Devices

The source and destination devices specify 16- or 32-bit data, depending on the selected data type. When a bit device such as input, output, internal relay, or shift register is designated as a source or destination device, 16 or 32 points starting with the designated number are processed as source or destination data. When a word device such as timer or counter is designated as a source device, the current value is read as source data. When a timer or counter is designated as a destination device, the result of the advanced instruction is set to the preset value for the timer or counter. When a data register is designated as a source or destination device, the data is read from or written to the designated data register.

Using Timer or Counter as Source Device

Since all timer instructions — TML (1-sec timer), TIM (100-ms timer), TMH (10-ms timer), and TMS (1-ms timer) — subtract from the preset value, the current value is decremented from the preset value and indicates the remaining time. As described above, when a timer is designated as a source device of an advanced instruction, the current value, or the remaining time, of the timer is read as source data. Adding counters CNT start counting at 0, and the current value is incremented up to the preset value. Reversible counters CDP and CUD start counting at the preset value and the current value is incremented or decremented from the preset value. When any counter is designated as a source device of an advanced instruction, the current value is read as source data.

Using Timer or Counter as Destination Device

As described above, when a timer or counter is designated as a destination device of an advanced instruction, the result of the advanced instruction is set to the preset value of the timer or counter. Timer and counter preset values can be 0 through 65535.

When a timer or counter preset value is designated using a data register, the timer or counter cannot be designated as a destination of an advanced instruction. When executing such an advanced instruction, a user program execution error will result. For details of user program execution error, see page 13-6.

Note: When a user program execution error occurs, the result is not set to the destination.

Data Types for Advanced Instructions (Integer Type)

When using move, data comparison, binary arithmetic, Boolean computation, bit shift/rotate, data conversion, and coordinate conversion instructions, data types can be selected from word (W), integer (I), double word (D), long (L), or float (F). For other advanced instructions, the data is processed in units of 16-bit word.

Data Type	Symbol	Bits	Quantity of Data Registers Used	Range of Decimal Values
Word (Unsigned 16 bits)	**W**	16 bits	1	0 to 65,535
Integer (Signed 15 bits)	**I**	16 bits	1	–32,768 to 32,767
Double Word (Unsigned 32 bits)	**D**	32 bits	2	0 to 4,294,967,295
Long (Signed 31 bits)	**L**	32 bits	2	–2,147,483,648 to 2,147,483,647
Float (Floating point)	**F**	32 bits	2	-3.402823×10^{38} to 3.402823×10^{38}

Decimal Values and Hexadecimal Storage (Word, Integer, Double, and Long Data Types)

The following table shows hexadecimal equivalents which are stored in the CPU, as a result of addition and subtraction of the decimal values shown:

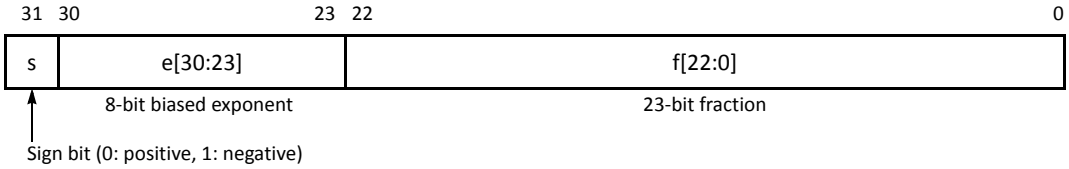
Data Type	Result of Addition	Hexadecimal Storage	Result of Subtraction	Hexadecimal Storage
Word	0	0000	65535	FFFF
	65535	FFFF	0	0000
	131071	(CY) FFFF	–1	(BW) FFFF
			–65535	(BW) 0001
			–65536	(BW) 0000
Integer	65534	(CY) 7FFE	65534	(BW) 7FFE
	32768	(CY) 0000	32768	(BW) 0000
	32767	7FFF	32767	7FFF
	0	0000	0	0000
	–1	FFFF	–1	FFFF
	–32767	8001	–32767	8001
	–32768	8000	–32768	8000
	–32769	(CY) FFFF	–32769	(BW) FFFF
	–65535	(CY) 8001	–65535	(BW) 8001
Double Word	0	00000000	4294967295	FFFFFFFF
	4294967295	FFFFFFFF	0	00000000
	8589934591	(CY) FFFFFFFF	–1	(BW) FFFFFFFF
			–4294967295	(BW) 00000001
			–4294967296	(BW) 00000000
Long	4294967294	(CY) 7FFFFFFE	4294967294	(BW) 7FFFFFFE
	2147483648	(CY) 00000000	2147483648	(BW) 00000000
	2147483647	7FFFFFFF	2147483647	7FFFFFFF
	0	00000000	0	00000000
	–1	FFFFFFFF	–1	FFFFFFFF
	–2147483647	80000001	–2147483647	80000001
	–2147483648	80000000	–2147483648	80000000
	–2147483649	(CY) FFFFFFFF	–2147483649	(BW) FFFFFFFF
	–4294967295	(CY) 80000001	–4294967295	(BW) 80000001

Floating-Point Data Format

The FC5A MicroSmart can specify the floating-point data type (F) for advanced instructions. Like the double word (D) and long integer (L) data types, the floating-point data type also uses two consecutive data registers to execute advanced instructions. The FC5A MicroSmart supports the floating-point data based on the single storage format of the IEEE (The Institute of Electrical and Electronics Engineers) Standard 754.

Single Storage Format

The IEEE single format consists of three fields: a 23-bit fraction, f; an 8-bit biased exponent, e; and 1-bit sign, s. These fields are stored contiguously in one 32-bit word, as shown in the figure below. Bits 0:22 contain the 23-bit fraction, f, with bit 0 being the least significant bit of the fraction and bit 22 being the most significant; bits 23:30 contain the 8-bit biased exponent, e, with bit 23 being the least significant bit of the biased exponent and bit 30 being the most significant; and the highest-order bit 31 contains the sign bit, s.



Single Storage Format

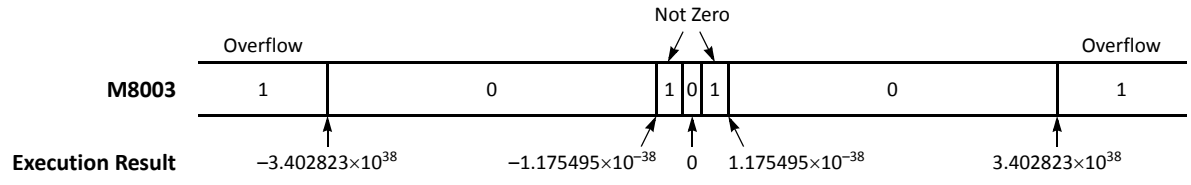
The table below shows the correspondence between the values of the three constituent fields s, e, and f and the value represented by the single format bit pattern. When any value out of the bit pattern is entered to the advanced instruction or when execution of advanced instructions, such as division by zero, has produced any value out of the bit pattern, a user program execution error will result, turning on special internal relay M8004 and the ERR LED on the CPU module.

Single Format Bit Patters	Value
0 < e < 255	$(-1)^s \times 2^{e-127} \times 1.f$ (normal numbers)
e = 0; f = 0 (all bits in f are zero)	$(-1)^s \times 2^{e-127} \times 0.0$ (signed zero)

Carry and Borrow in Floating-Point Data Processing

When advanced instructions involving floating-point data are executed, special internal relay M8003 (carry and borrow) is updated.

M8003	Execution Result	Value
1	≠ 0	Overflow (out of the range between -3.402823×10^{38} and 3.402823×10^{38})
1	0	Not zero (within the range between -1.175495×10^{-38} and 1.175495×10^{-38})
0	0	Zero

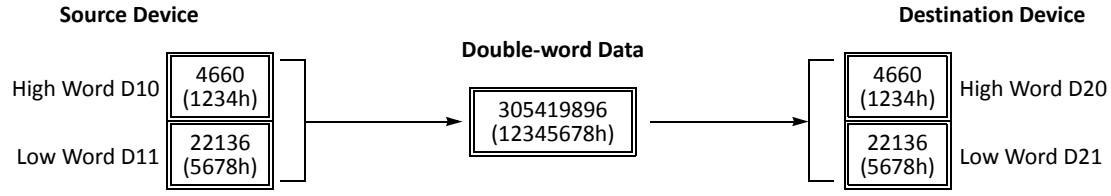


Double-word Devices in Data Registers

When the double-word data type is selected for the source or destination device, the data is loaded from or stored to two consecutive data registers. The order of the two devices depends on the device type.

When a data register, timer, or counter is selected as a double-word device, the high-word data is loaded from or stored to the first device selected. The low-word data is loaded from or stored to the subsequent device.

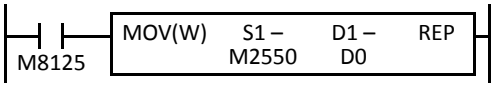
Example: When data register D10 is designated as a double-word source device and data register D20 is designated as a double-word destination device, the data is loaded from or stored to two consecutive data registers as illustrated below.



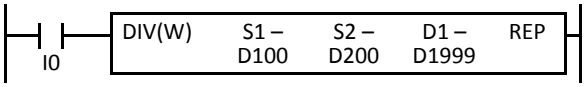
Note: The above example is the default setting of the FC5A MicroSmart. The order of two devices can be selected on CPU modules with system program version 110 or higher. See page 5-46.

Discontinuity of Device Areas

Each device area is discrete and does not continue, for example, from input to output or from output to internal relay. In addition, special internal relays M8000 through M8157 (all-in-one type CPU) or M8317 (slim type CPU) are in a separate area from internal relays M0 through M2557. Data registers D0 through D1999, expansion data registers D2000 through D7999 (slim type CPU only), and special data registers D8000 through D8199 (all-in-one type CPU) or D8499 (slim type CPU) are in separate areas and do not continue with each other.

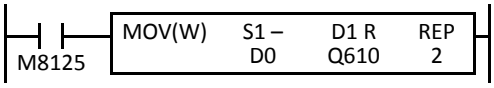


The internal relay ends at M2557. Since the MOV (move) instruction reads 16 internal relays, the last internal relay exceeds the valid range, resulting in a user program syntax error.



This program results in a user program syntax error. The destination of the DIV (division) instruction requires two data registers D1999 and D2000. Since D2000 exceeds the valid range, a user program syntax error occurs.

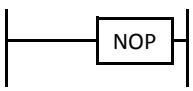
Advanced instructions execute operation only on the available devices in the valid area. If a user program syntax error is found during programming, WindLDR rejects the program instruction and shows an error message.



The MOV (move) instruction sets data of data register D0 to 16 outputs Q610 through Q627 in the first repeat cycle. The destination of the second cycle is the next 16 outputs Q630 through Q647, which are invalid, resulting in a user program syntax error.

For details about repeat operations of each advanced instruction, see the following chapters.

NOP (No Operation)



No operation is executed by the NOP instruction.

The NOP instruction may serve as a place holder. Another use would be to add a delay to the CPU scan time, in order to simulate communication with a machine or application, for debugging purposes.

The NOP instruction does not require an input and device.

Details of all other advanced instructions are described in the following chapters.

9: ANALOG I/O CONTROL

Introduction

The MicroSmart provides analog I/O control capabilities of 12- through 16-bit resolution using analog I/O modules.

This chapter describes the system setup for using analog I/O modules, WindLDR programming procedures, data register device addresses for analog I/O modules, and application examples.

For hardware specifications of analog I/O modules, see page 2-55.

System Setup

The MicroSmart CPU module can be used with a maximum of seven expansion I/O modules, which include digital I/O modules and analog I/O modules.

Quantity of Applicable Analog I/O Modules

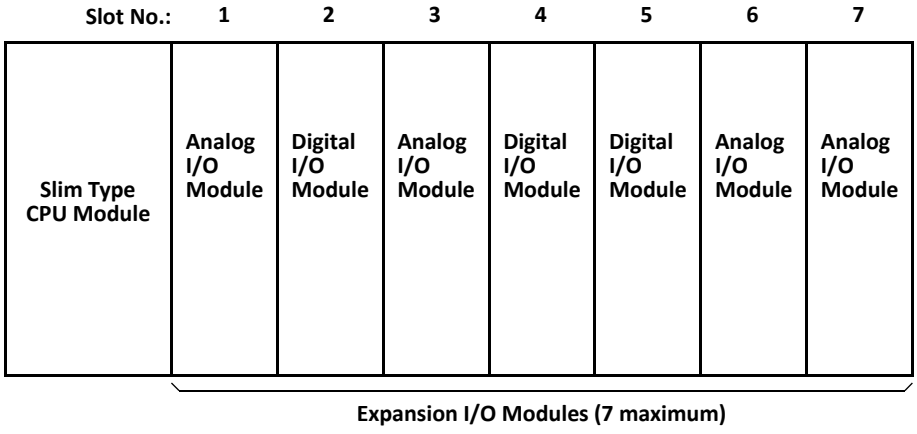
The quantity of the analog I/O modules that can be connected to the MicroSmart CPU module depends on the model of the MicroSmart CPU modules as listed below:

CPU Module	All-in-One Type CPU Module			Slim Type CPU Module	
	FC5A-C10R2 FC5A-C10R2C FC5A-C10R2D	FC5A-C16R2 FC5A-C16R2C FC5A-C16R2D FC5A-C24R2D	FC5A-C24R2 FC5A-C24R2C	FC5A-D16RK1 FC5A-D16RS1	FC5A-D32K3 FC5A-D32S3 FC5A-D12K1E FC5A-D12S1E
Quantity of Analog I/O Modules	—	—	4	7	7

Note: FC5A all-in-one 24-I/O type CPU modules cannot use analog I/O modules in combination with the AS-Interface master module (FC4A-AS62M) and/or expansion RS232C/RS485 communication module (FC5A-SIF2 or FC5A-SIF4). When using these modules in combination with analog I/O modules, use the slim type CPU module.

The all-in-one 24-I/O 12V DC type CPU module cannot use analog I/O modules.

System Setup Example



• **Slot No.**

Indicates the position where the expansion module is mounted. The slot number starts with 1 next to the CPU module up to a maximum of 7.

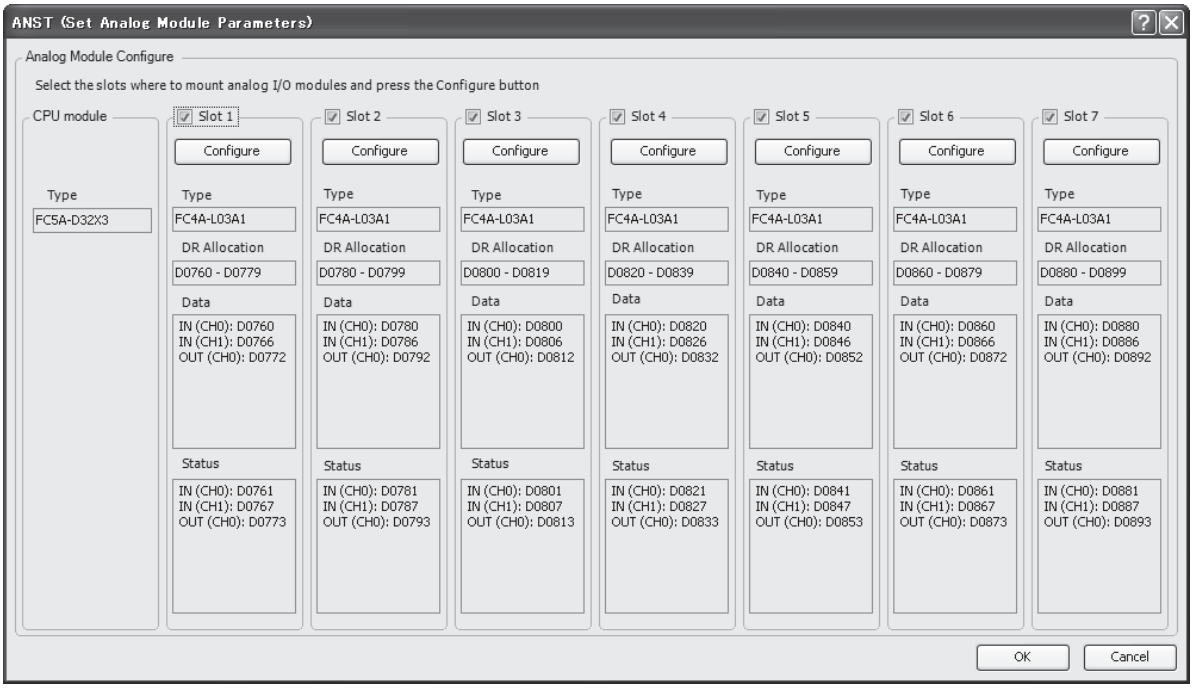
Note: Analog I/O modules cannot be mounted to the right of the expansion interface module.

Programming WindLDR

WindLDR ver. 5.0 or later has the ANST (Set Analog Module Parameters) macro for easy programming of analog I/O modules.

1. Place the cursor where you want to insert the ANST instruction on the ladder editing screen, type **ANST** and press the Enter key.

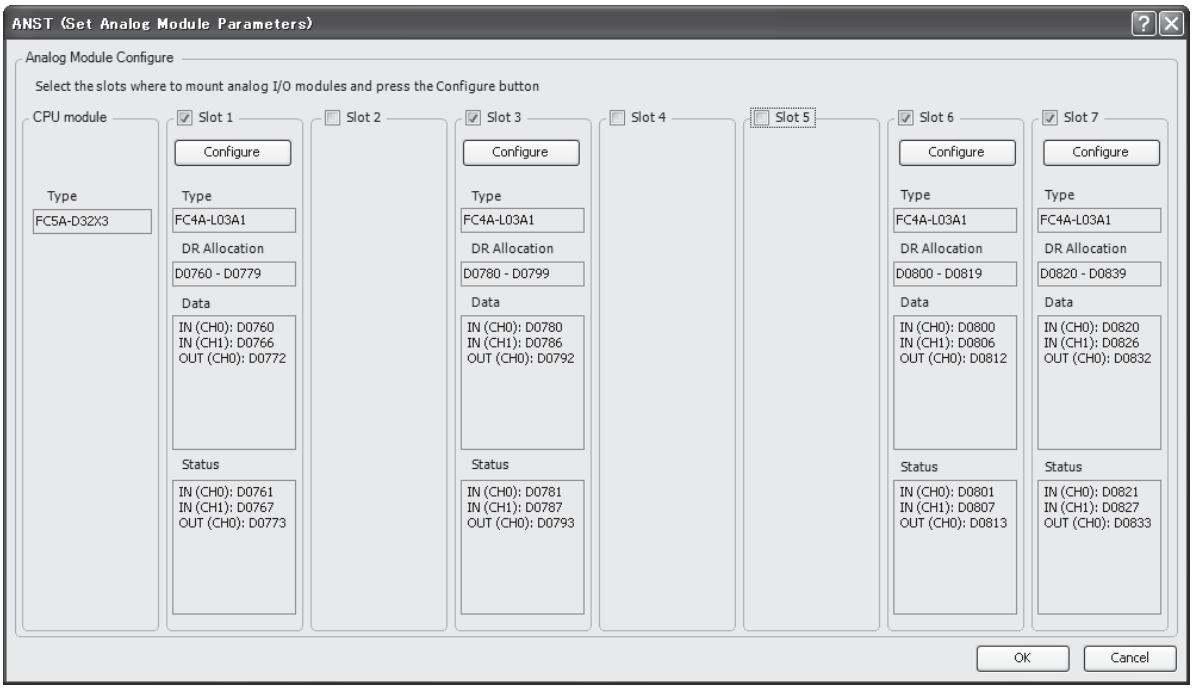
The Set Analog Module Parameters dialog box appears.



2. Select the slots where analog I/O modules are mounted.

All slots are selected to use seven analog I/O modules as default. Click the check box to deselect slots where analog I/O modules are *not* mounted.

When using analog I/O modules on Slots 1, 3, 6, and 7, deselect Slots 2, 4, and 5 as shown below.

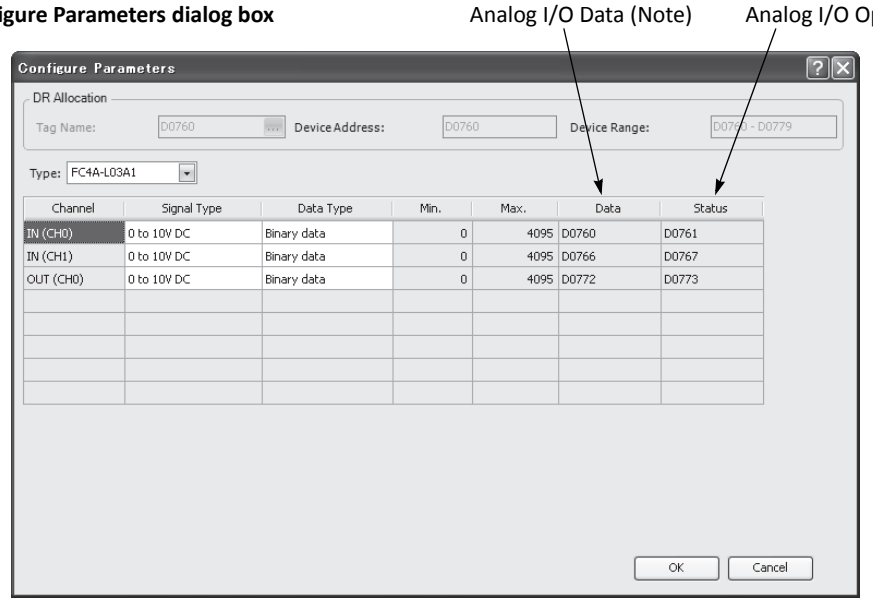


3. Click the **Configure** button under the selected slots.

The Configure Parameters dialog box appears. All parameters for analog I/O control can be set in this dialog box. Available parameters vary with the type of the analog I/O module.

END Refresh Type Configure Parameters dialog box

FC4A-L03A1
FC4A-L03AP1
FC4A-J2A1
FC4A-K1A1



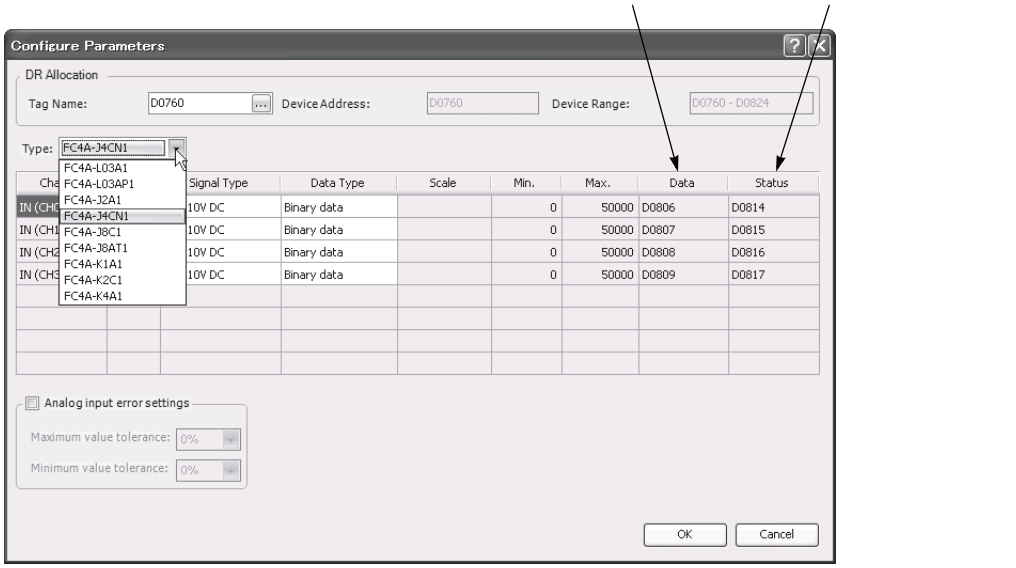
4. Select the type of the analog I/O module.

Click on the right of the analog I/O module Type No., then a pull-down list shows eight available modules.

Depending on the selected analog I/O module, other parameters available for the selected module are shown.

Ladder Refresh Type Configure Parameters dialog box

FC4A-J4CN1
FC4A-J8C1
FC4A-J8AT1
FC4A-K2C1
FC4A-K4A1



In the Configure Parameters dialog box, parameters in white cells are selectable while gray cells indicate default parameters. In the white cells, optional values can be selected from a pull-down list or entered by typing required values.

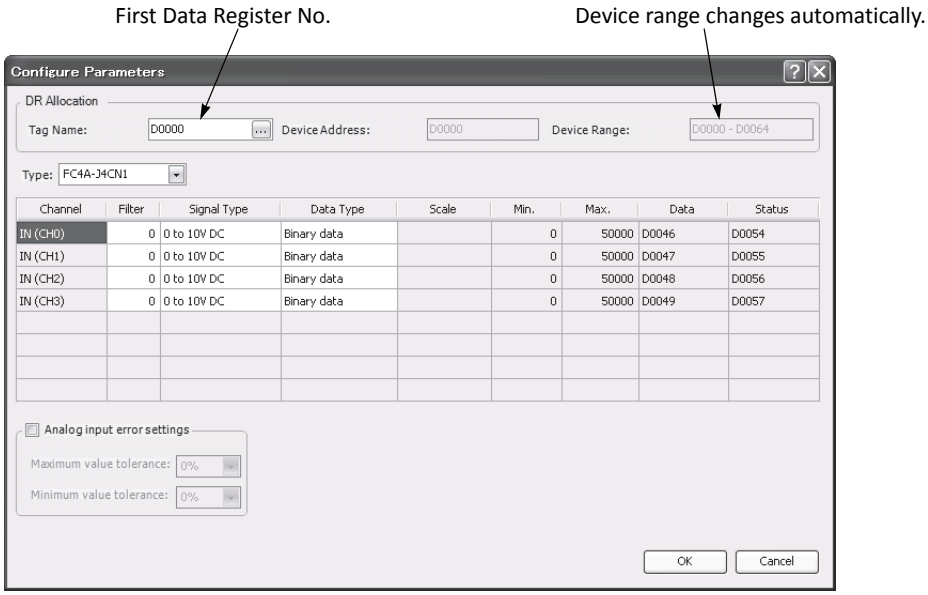
Note for PID Instruction Source Device S4 (process variable)

When using the PID instruction, specify the data register number shown under Data in the Configure Parameters dialog box as source device S4 (process variable) of the PID instruction. The analog input data in the selected data register is used as the process variable of the PID instruction.

5. Select a DR device address (Ladder refresh type only).

CPU Module	DR Allocation
END Refresh Type FC4A-L03A1 FC4A-L03AP1 FC4A-J2A1 FC4A-K1A1	DR allocation starts with D760 as default, and the first DR number cannot be changed. One analog I/O module occupies 20 data registers. When a maximum of seven analog I/O modules are used, data registers D760 through D899 are used for analog I/O control.
Ladder Refresh Type FC4A-J4CN1 FC4A-J8C1 FC4A-J8AT1 FC4A-K2C1 FC4A-K4A1	The first data register can be selected as required. Enter the first DR number used for analog I/O control. One analog input module occupies a maximum of 65 data registers. One analog output module occupies a maximum of 27 data registers.

Ladder Refresh Type Configure Parameters dialog box



6. Enter a filter value (Ladder refresh type analog input modules only).

The filter function is available for the FC4A-J4CN1, FC4A-J8C1, and FC4A-J8AT1 only. Filtering ensures smooth input of analog data into the CPU module.

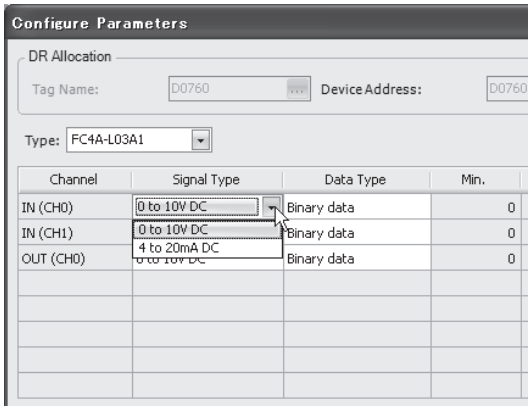
Filter Value	Description
0	Without filter function
1 to 255	The average of N pieces of analog input data is read as analog input data, where N is the designated filter value. $\text{Analog input data} = \frac{(\text{Previous analog input data}) \times (\text{Filter value}) + (\text{Current analog input data})}{(\text{Filter value}) + 1}$

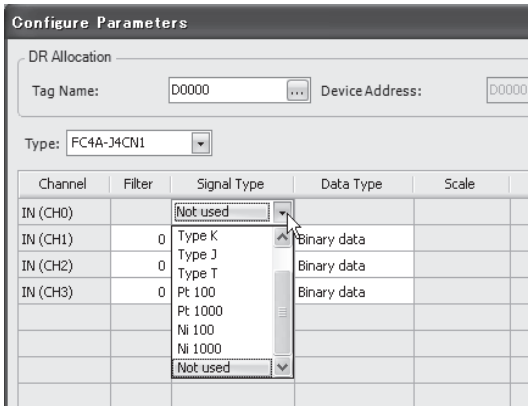
7. Select a signal type for each channel.

Click on the right of the Signal Type field, then a pull-down list appears to show all available input or output signal types.

When you do not use any input or output signal, select the default value or **Not used** for the channel.

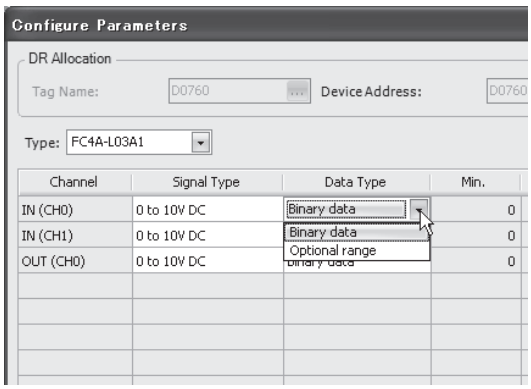
Analog I/O Module		For unused channel, select
END Refresh Type	FC4A-L03A1, FC4A-J2A1	0 to 10V DC
	FC4A-L03AP1	Type K
Ladder Refresh Type	FC4A-J4CN1, FC4A-J8C1, FC4A-J8AT1, FC4A-K2C1, FC4A-K4A1	Not used

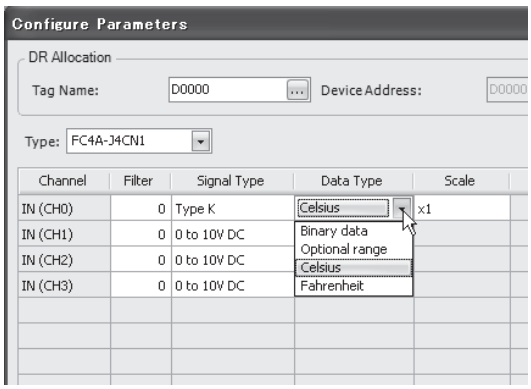




8. Select a data type for each channel.

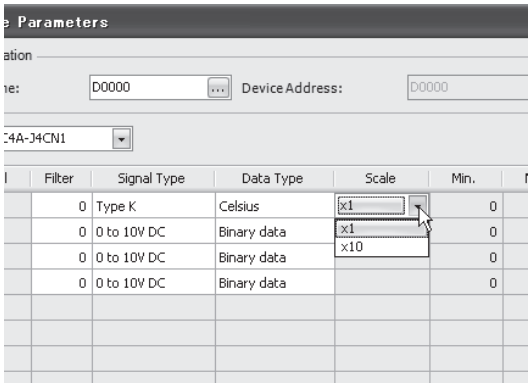
Click on the right of the Data Type field, then a pull-down list appears to show all available input or output data types.

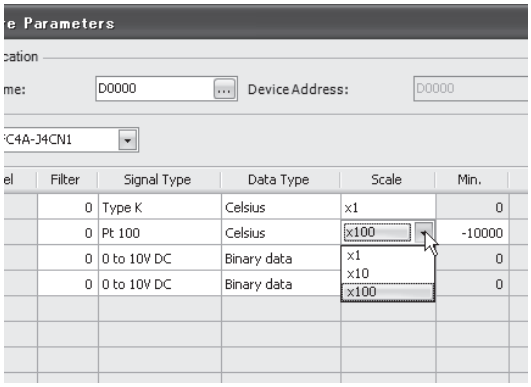




9. Select a scale value (Ladder refresh type analog input modules only).

When Celsius or Fahrenheit is selected for thermocouple, resistance thermometer, or thermistor signal types on ladder refresh type analog input modules, the scale value can be selected from ×1, ×10, or ×100 depending on the selected signal type. Using this function, the analog input data can be multiplied to ensure precise control.



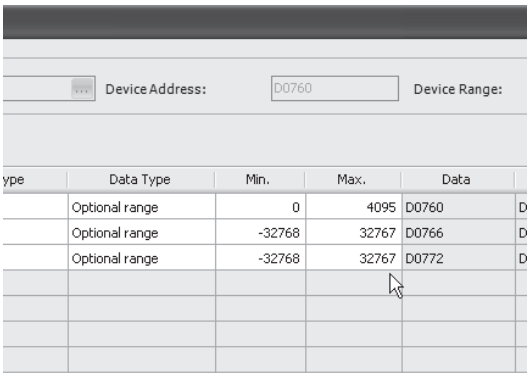


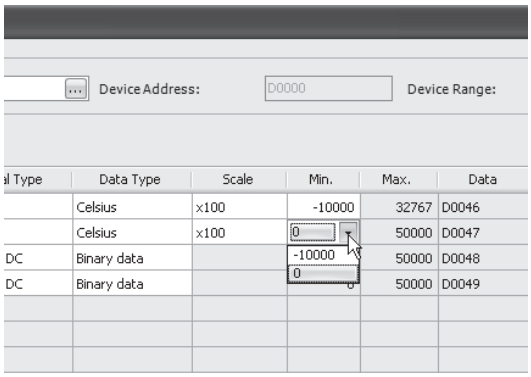
10. Select maximum and minimum values.

For analog input values, when Optional range is selected for the Data Type, designate the analog input data minimum and maximum values which can be –32,768 through 32,767.

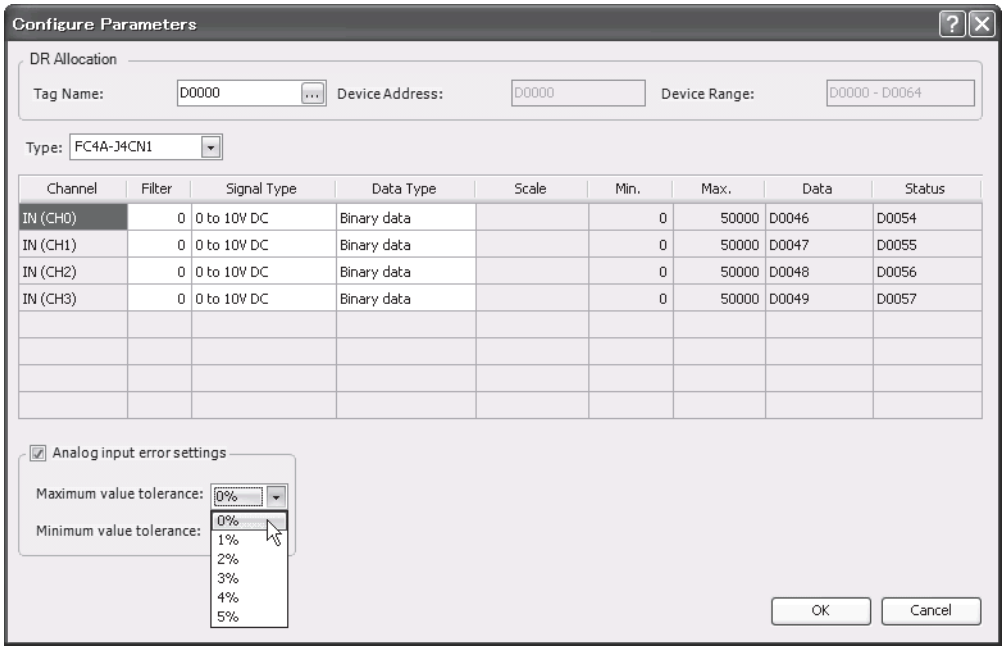
In addition, when using resistance thermometers (Pt100, Pt1000, Ni100, or Ni1000) with the Celsius or Fahrenheit Data Type and the ×100 scale, select the analog input data minimum value from 0 or another value in the pull-down list. The maximum value is changed automatically according to the selected minimum value.

For analog output values, when Optional range is selected for the Data Type, designate the analog output data minimum and maximum values which can be –32,768 through 32,767.





11. Configure analog input error settings. (FC4A-J4CN1 and FC4A-J8C1 only.)



To use analog input error settings, CPU modules with system program version 230 or higher and an analog module (version 200 or higher) are required.

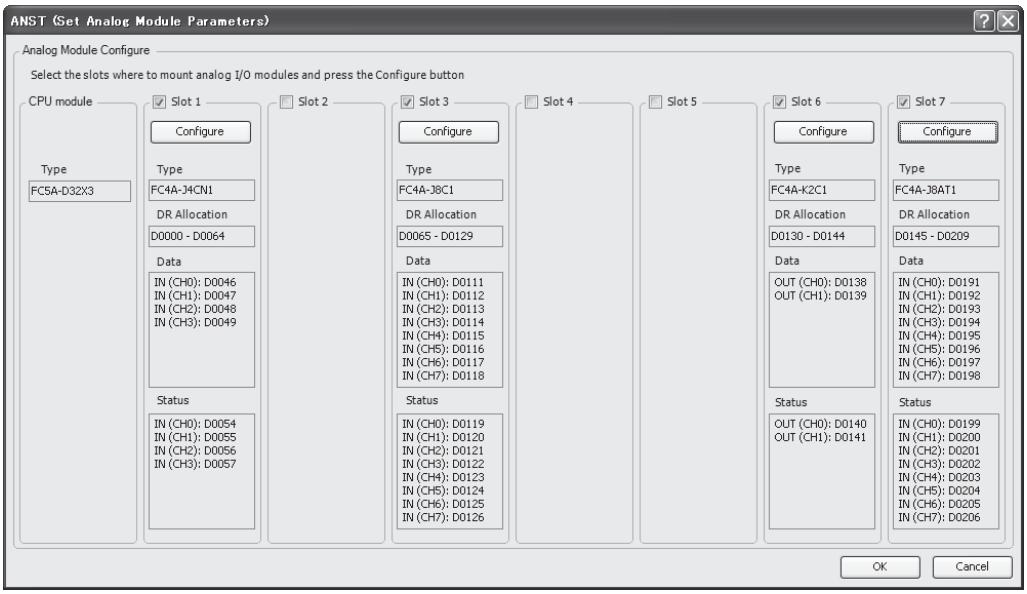
12. View the data register numbers allocated to Data and Status.

Parameter		DR Allocation
Data	**Analog I/O Data** Stores the digital data converted from an analog input signal or converted into an analog output signal. Designated as source device S4 (process variable) of the PID instruction.	**END Refresh Type** Data registers are automatically allocated depending on the slot where the analog I/O module is mounted. **Ladder Refresh Type** Data registers are automatically allocated depending on the number designated in the DR Device Address field.
Status	**Analog I/O Operating Status** Stores an analog I/O operating status code. See pages 9-14 and 9-17.	

13. Click the **OK** button to save changes and exit the Configure Parameter dialog box.

14. Repeat the same steps for other slots.

15. When finished, click the **OK** button to save changes and exit the Set Analog Module Parameters dialog box.



Analog I/O Control Parameters

Available parameters for analog I/O control depend on the type of analog I/O modules as summarized in the following table. Designate the parameters in the Configure Parameters dialog box of the ANST macro as required by your application.

Parameter	Analog I/O Module		Analog Input Module				Analog Output Module		
	END Refresh Type		Ladder Refresh Type				END	Ladder	
	FC4A-L03A1	FC4A-L03AP1	FC4A-J2A1	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1	FC4A-K1A1	FC4A-K2C1	FC4A-K4A1
Analog Input Signal Type	X	X	X	X	X	X	—	—	—
	Page 9-12		Page 9-12				—		
Analog Input Data Type	X	X	X	X	X	X	—	—	—
	Page 9-12		Page 9-12				—		
Analog Input Data Minimum/Maximum Values	X	X	X	X	X	X	—	—	—
	Page 9-14		Page 9-14				—		
Filter Value	—	—	—	X	X	X	—	—	—
	—		—	Page 9-14			—		
Thermistor Parameter	—	—	—	—	—	X	—	—	—
	—		—			9-14	—		
Analog Input Data	X	X	X	X	X	X	—	—	—
	Page 9-14		Page 9-14				—		
Analog Input Operating Status	X	X	X	X	X	X	—	—	—
	Page 9-14		Page 9-14				—		
Analog Output Signal Type	X	X	—	—	—	—	X	X	X
	Page 9-16		—				Page 9-16		
Analog Output Data Type	X	X	—	—	—	—	X	X	X
	Page 9-16		—				Page 9-16		
Analog Output Data Minimum/Maximum Values	X	X	—	—	—	—	X	X	X
	Page 9-16		—				Page 9-16		
Analog Output Data	X	X	—	—	—	—	X	X	X
	Page 9-17		—				Page 9-17		
Analog Output Operating Status	X	X	—	—	—	—	X	X	X
	Page 9-17		—				Page 9-17		

Data Register Device Addresses for Analog I/O Modules

Analog I/O modules are numbered from 1 through 7, in the order of increasing distance from the CPU module. Data registers are allocated to each analog I/O module depending on the analog I/O module number. END refresh type analog I/O modules and ladder refresh type analog I/O modules have different data register allocation.

END Refresh Type Analog I/O Modules

Each END refresh type analog I/O module is automatically allocated 20 data registers to store parameters for controlling analog I/O operation, starting with D760 through D779 for analog I/O module No. 1, up to D880 through D899 for analog I/O module No. 7. When a maximum of seven analog I/O modules are *not* used, data registers allocated to the unused analog I/O module numbers can be used as ordinary data registers.

When a maximum of seven END refresh type analog I/O modules are mounted, data registers D760 through D899 are allocated to analog modules 1 through 7 as shown below. The ANST macro is used to program data registers for the analog I/O module configuration. The CPU module checks the analog I/O configuration only once when the CPU starts to run. If you have changed the parameter while the CPU is running, stop and restart the CPU to enable the new parameter.

The END refresh type analog I/O module number starts with 1 next to the CPU module up to a maximum of 7.

The run-time program download and test program download cannot be used to change analog I/O parameters.

Channel	Function	END Refresh Type Analog I/O Module No.							R/W
		1	2	3	4	5	6	7	
Analog Input Ch 0	Analog input data	D760	D780	D800	D820	D840	D860	D880	R
	Analog input operating status	D761	D781	D801	D821	D841	D861	D881	R
	Analog input signal type	D762	D782	D802	D822	D842	D862	D882	R/W
	Analog input data type	D763	D783	D803	D823	D843	D863	D883	R/W
	Analog input data minimum value	D764	D784	D804	D824	D844	D864	D884	R/W
	Analog input data maximum value	D765	D785	D805	D825	D845	D865	D885	R/W
Analog Input Ch 1	Analog input data	D766	D786	D806	D826	D846	D866	D886	R
	Analog input operating status	D767	D787	D807	D827	D847	D867	D887	R
	Analog input signal type	D768	D788	D808	D828	D848	D868	D888	R/W
	Analog input data type	D769	D789	D809	D829	D849	D869	D889	R/W
	Analog input data minimum value	D770	D790	D810	D830	D850	D870	D890	R/W
	Analog input data maximum value	D771	D791	D811	D831	D851	D871	D891	R/W
Analog Output	Analog output data	D772	D792	D812	D832	D852	D872	D892	R/W
	Analog output operating status	D773	D793	D813	D833	D853	D873	D893	R
	Analog output signal type	D774	D794	D814	D834	D854	D874	D894	R/W
	Analog output data type	D775	D795	D815	D835	D855	D875	D895	R/W
	Analog output data minimum value	D776	D796	D816	D836	D856	D876	D896	R/W
	Analog output data maximum value	D777	D797	D817	D837	D857	D877	D897	R/W
– Reserved –		D778	D798	D818	D838	D858	D878	D898	R/W
		D779	D799	D819	D839	D859	D879	D899	R/W

Note: Data registers allocated to the unused analog I/O module numbers can be used as ordinary data registers.

Ladder Refresh Type Analog I/O Modules

When using a ladder refresh type analog input or output module, the first data register number can be designated in the ASNT macro dialog box. The quantity of required data registers depends on the model of the ladder refresh type analog input or output module.

Analog I/O Module	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1	FC4A-K2C1	FC4A-K4A1
Quantity of Data Registers for Analog I/O Operation	65	65	65	15	27

Data register numbers and parameters are shown in the table below.

Ladder Refresh Type Analog Input Module Data Register Allocation (FC4A-J4CN1, FC4A-J8C1, and FC4A-J8AT1)

Data Register Number Offset	Data Size (word)	Parameter	Channel	Default	R/W
+0 (Low Byte)	1	Analog input signal type	CH0	FFh	R/W
+0 (High Byte)		— Reserved —	All channels	00h	
+1	4	Analog input data configuration	CH0	0	R/W
+5	1	Analog input signal type	CH1	00FFh	R/W
+6	4	Analog input data configuration		0	R/W
+10	1	Analog input signal type	CH2	00FFh	R/W
+11	4	Analog input data configuration		0	R/W
+15	1	Analog input signal type	CH3	00FFh	R/W
+16	4	Analog input data configuration		0	R/W
+20	1	Analog input signal type	CH4 *	00FFh	R/W
+21	4	Analog input data configuration		0	R/W
+25	1	Analog input signal type	CH5 *	00FFh	R/W
+26	4	Analog input data configuration		0	R/W
+30	1	Analog input signal type	CH6 *	00FFh	R/W
+31	4	Analog input data configuration		0	R/W
+35	1	Analog input signal type	CH7 *	00FFh	R/W
+36	4	Analog input data configuration		0	R/W
+40	3	Thermistor parameters (FC4A-J8AT1 only)	CH0 to CH3	0	R/W
+43	3		CH4 to CH7 *	0	R/W
+46	1	Analog input data	CH0	—	R
+47	1		CH1	—	R
+48	1		CH2	—	R
+49	1		CH3	—	R
+50	1		CH4 *	—	R
+51	1		CH5 *	—	R
+52	1		CH6 *	—	R
+53	1		CH7 *	—	R
+54	1	Analog input operating status	CH0	—	R
+55	1		CH1	—	R
+56	1		CH2	—	R
+57	1		CH3	—	R
+58	1		CH4 *	—	R
+59	1		CH5 *	—	R
+60	1		CH6 *	—	R
+61	1		CH7 *	—	R
+62	3	— Reserved —	All channels	—	R

* Data registers for channels 4 through 7 are reserved on the FC4A-J4CN1.

Ladder Refresh Type Analog Output Module Data Register Allocation (FC4A-K2C1)

Data Register Number Offset	Data Size (word)	Parameter	Channel	Default	R/W
+0 (Low Byte)	1	Analog output signal type	CH0	FFh	R/W
+0 (High Byte)		— Reserved —	All channels	00h	
+1	3	Analog output data configuration	CH0	0	R/W
+4	1	Analog output signal type	CH1	00FFh	R/W
+5	3	Analog output data configuration		0	R/W
+8	1	Analog output data	CH0	0	R/W
+9	1		CH1	0	R/W
+10	1	Analog output operating status	CH0	—	R
+11	1		CH1	—	R
+12	3	— Reserved —	All channels	—	R

Ladder Refresh Type Analog Output Module Data Register Allocation (FC4A-K4A1)

Data Register Number Offset	Data Size (word)	Parameter	Channel	Default	R/W
+0 (Low Byte)	1	Analog output signal type	CH0	00h	R/W
+0 (High Byte)		— Reserved —	All channels	00h	R/W
+1	3	Analog output data configuration	CH0	0	R/W
+4	1	Analog output signal type	CH1	0	R/W
+5	3	Analog output data configuration		0	R/W
+8	1	Analog output signal type	CH2	0	R/W
+9	3	Analog output data configuration		0	R/W
+12	1	Analog output signal type	CH3	0	R/W
+13	3	Analog output data configuration		0	R/W
+16	1	Analog output data	CH0	0	R/W
+17	1		CH1	0	R/W
+18	1		CH2	0	R/W
+19	1		CH3	0	R/W
+20	1	Analog output operating status	CH0	—	R
+21	1		CH1	—	R
+22	1		CH2	—	R
+23	1		CH3	—	R
+24	3	— Reserved —	All channels	—	R

Analog Input Parameters

Analog input parameters include the analog input signal type, analog input data type, analog input minimum and maximum values, filter value, thermistor parameter, analog input data, and analog input operating status. This section describes these parameters in detail.

Analog Input Signal Type

A total of 11 analog input signal types are available, depending on the analog I/O or analog input module. Select an analog input signal type for each analog input channel. When a channel is not used, select the default value or **Not used** for the channel.

Parameter		FC4A-L03A1	FC4A-L03AP1	FC4A-J2A1	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1
0	Voltage input (0 to 10V DC)	X	—	X	X	X	—
1	Current input (4 to 20 mA DC)	X	—	X	X	X	—
2	Type K thermocouple	—	X	—	X	—	—
3	Type J thermocouple	—	X	—	X	—	—
4	Type T thermocouple	—	X	—	X	—	—
5	Pt 100 resistance thermometer	—	X	—	X	—	—
6	Pt 1000 resistance thermometer	—	—	—	X	—	—
7	Ni 100 resistance thermometer	—	—	—	X	—	—
8	Ni 1000 resistance thermometer	—	—	—	X	—	—
9	NTC type thermistor	—	—	—	—	—	X
10	PTC type thermistor	—	—	—	—	—	X
255	Not used	—	—	—	X	X	X

Analog Input Data Type

A total of five analog input data types are available, depending on the analog I/O or analog input module. Select an analog input data type for each analog input channel.

Parameter		FC4A-L03A1	FC4A-L03AP1	FC4A-J2A1	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1
0	Binary data	X	X	X	X	X	X
1	Optional range	X	X	X	X	X	X
2	Celsius	—	X	—	X	—	NTC only
3	Fahrenheit	—	X	—	X	—	NTC only
4	Resistance	—	—	—	—	—	X

Binary Data

When Binary data is selected as an analog input data type, the analog input is linearly converted into digital data in the range described in the table below.

Type No.	FC4A-L03A1 FC4A-L03AP1 FC4A-J2A1	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1
Analog Input Data	0 to 4095	Analog Input Signal Type — Analog Input Data Voltage/Current: 0 to 50,000 Thermocouple: 0 to 50,000 Pt100, Ni100: 0 to 6,000 Pt1000, Ni1000: 0 to 60,000	0 to 50000	0 to 4000

Optional Range

When Optional range is selected as an analog input data type, the analog input is linearly converted into digital data in the range between the minimum and maximum values designated in the Configure Parameters dialog box.

Type No.	FC4A-L03A1	FC4A-L03AP1	FC4A-J2A1	FC4A-J4CN1	FC4A-J8C1	FC4A-J8AT1
Analog Input Data	Analog input data minimum value to maximum value (–32768 to 32767)					

Celsius and Fahrenheit

When Celsius or Fahrenheit is selected as an analog input data type, the analog input data range depends on the analog input signal type, scale value, and the type of the analog input module, FC4A-L03AP1, FC4A-J4CN1, and FC4A-J8AT1.

- **FC4A-L03AP1**

Analog Input Signal Type	Celsius		Fahrenheit	
	Temperature (°C)	Analog Input Data	Temperature (°F)	Analog Input Data
Type K thermocouple	0 to 1300	0 to 13000	32 to 2372	320 to 23720
Type J thermocouple	0 to 1200	0 to 12000	32 to 2192	320 to 21920
Type T thermocouple	0 to 400	0 to 4000	32 to 752	320 to 7520
Pt100 resistance thermometer	–100.0 to 500.0	–1000 to 5000	–148.0 to 932.0	–1480 to 9320

- **FC4A-J4CN1**

Analog Input Signal Type	Scale	Celsius		Fahrenheit	
		Temperature (°C)	Analog Input Data	Temperature (°F)	Analog Input Data
Type K thermocouple	×1	0 to 1300	0 to 1300	32 to 2372	32 to 2372
	×10	0.0 to 1300.0	0 to 13000	32.0 to 2372.0	320 to 23720
Type J thermocouple	×1	0 to 1200	0 to 1200	32 to 2192	32 to 2192
	×10	0.0 to 1200.0	0 to 12000	32.0 to 2192.0	320 to 21920
Type T thermocouple	×1	0 to 400	0 to 400	32 to 752	32 to 752
	×10	0.0 to 400.0	0 to 4000	32.0 to 752.0	320 to 7520
Pt100, Pt1000 resistance thermometer	×1	–100 to 500	–100 to 500	–148 to 932	–148 to 932
	×10	–100.0 to 500.0	–1000 to 5000	–148.0 to 932.0	–1480 to 9320
	×100	0.00 to 500.00 –100.00 to 327.67	0 to 50000 –10000 to 32767	0.00 to 655.35 –148.00 to 327.67	0 to 65535 –14800 to 32767
Ni100, Ni1000 resistance thermometer	×1	–60 to 180	–60 to 180	–76 to 356	–76 to 356
	×10	–60.0 to 180.0	–600 to 1800	–76.0 to 356.0	–760 to 3560
	×100	–60.00 to 180.00	–6000 to 18000	0.00 to 356.00 –76.00 to 327.67	0 to 35600 –7600 to 32767

- **FC4A-J8AT1**

Analog Input Signal Type	Scale	Celsius		Fahrenheit	
		Temperature (°C)	Analog Input Data	Temperature (°F)	Analog Input Data
NTC thermistor	×1	–50 to 150	–50 to 150	–58 to 302	–58 to 302
	×10	–50.0 to 150.0	–500 to 1500	–58.0 to 302.0	–580 to 3020

Resistance

When Resistance is selected as an analog input data type, the analog input is linearly converted into digital data in the range described in the table below. This option is available only when NTC or PTC type thermistor is selected for the FC4A-J8AT1.

- **FC4A-J8AT1**

Analog Input Signal Type	Resistance	
	Resistance (Ω)	Analog Input Data
NTC/PTC thermistor	0 to 100000	0 to 10000

Analog Input Minimum/Maximum Values

For analog input values, when Optional range is selected for the Data Type, designate the analog input data minimum and maximum values which can be –32,768 through 32,767.

In addition, when using resistance thermometers (Pt100, Pt1000, Ni100, or Ni1000) with the Celsius or Fahrenheit Data Type and the ×100 scale, select the analog input data minimum value from 0 or another value in the pull-down list. The maximum value is changed automatically according to the selected minimum value.

Filter Value

The filter function is available for the ladder input type FC4A-J4CN1, FC4A-J8C1, and FC4A-J8AT1 only. Filtering ensures smooth input of analog data into the CPU module. For the filtering function of analog input signals, see page 9-4.

Valid values are 0 through 255.

Thermistor Parameter

Thermistor parameters are enabled when selecting NTC thermistor for the analog input type of the FC4A-J8AT1. The same parameters are specified for four channels: CH0 to CH3 and CH4 to CH7.

Channel	NTC Thermistor Parameters (Values indicated on the thermistor)		Valid Range
CH0 to CH3 CH4 to CH7	R0:	Thermistor resistance value at the temperature (°C)	0 to 65535
	T0:	Temperature (°C)	–32768 to 32767
	B:	Thermistor B parameter	0 to 65535

For NTC type thermistors, analog input data can be calculated from the following formula:

$$\text{Analog Input Data} = \frac{B \times T0}{B + T0 \times \log(r/R0)}$$

where, r = thermistor resistance (Ω)

For PTC type thermistors, linearize the analog input data using the XYFS instruction.

Analog Input Data

The analog input signal is converted into a digital value within the range specified by the analog input data type and applicable parameters, and is stored to a data register allocated to analog input data. The analog input data register number is shown under Data in the Configure Parameters dialog box.

END Refresh Type

The analog input signal is converted into a digital value and stored to a data register, such as D760 or D766, allocated to analog input channel 1 or 2 on analog module number 1 through 7 depending on the mounting position.

The analog input data stored in the allocated data register is updated whether the CPU module is running or stopped. When the CPU module is running, the update occurs at the END processing of every scan or 10 ms, whichever is longer. When the CPU module is stopped, the update occurs every 10 ms.

Ladder Refresh Type

The analog input signal is converted into a digital value and stored to a data register determined by the data register number selected in the Configure Parameters dialog box of the ANST macro. The analog input data stored in the allocated data register is updated when the RUNA instruction contained in the ANST macro is executed.

When a certain channel of a ladder refresh type analog input module is not used, data registers allocated to the unused channel will store indefinite values if the values are read out of the analog input module. Do not use the allocated data registers for other purposes.

Only when the analog input status code is 0, the analog input data is assured. Make sure that a user program reads analog input data only when the analog input status code is 0.

Analog Input Operating Status

The operating status of each analog input channel is stored to a data register allocated to analog input operating status. While the analog input is operating normally, the data register stores 0. The analog input operating status data register number is shown under Status in the Configure Parameters dialog box.

END Refresh Type

The operating status of each analog input channel is stored to a data register, such as D761 or D767, allocated to analog input channel 1 or 2 on analog module number 1 through 7 depending on the mounting position.

The analog input operating status data is updated whether the CPU module is running or stopped. When the CPU module is running, the update occurs at the END processing of every scan or 10 ms, whichever is longer. When the CPU module is stopped, the update occurs every 10 ms.

Status Code	Analog Input Operating Status (END refresh type)
0	Normal operation
1	Converting data (during the first data conversion after power-up)
2	Initializing
3	Invalid parameter or analog input channel not available on the installed analog module
4	Hardware failure (external power supply failure)
5	Incorrect wiring (input data over valid range)
6	Incorrect wiring (input data below valid range or current loop open)

Ladder Refresh Type

The operating status of each analog input channel is stored to a data register determined by the data register number selected in the Configure Parameters dialog box of the ANST macro.

Operating Status Bit		Analog Input Operating Status (Ladder refresh type)	
Bit 0	0	Operating status bit	Normal operation
	1		Initializing, changing configuration, hardware initialization error
Bit 1	0	Parameter bit	Parameter configuration normal
	1		Parameter configuration error
Bit 2	0	External power supply bit	External power supply normal
	1		External power supply error
Bit 3	0	Maximum value over bit	Within the maximum value
	1		Maximum value over error
Bit 4	0	Minimum value over bit	Within the minimum value
	1		Minimum value under error
Bit 5 to Bit 15	0	Reserved	Normal operation

Analog Input Error Settings

When using analog voltage or current input, the boundary values that trigger the maximum value over error and minimum value over error can be configured. Preset values are specified as a percentage of full scale. While the analog input value is within the boundary range specified by the settings, the maximum value over error and minimum value over error are not turned on. The settings are applied to all analog input channels.

This function can only be used on FC4A-J4CN1/-J8C1 with version 110 or higher.

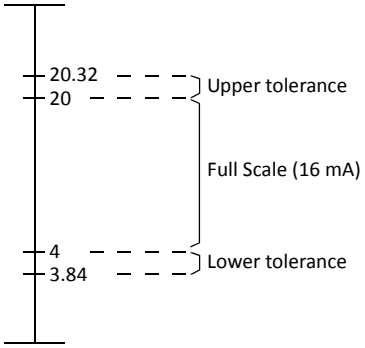
Error Range Settings		Analog Input Error Settings
Current	**Voltage**	**Description**
0 to 5%	0 to 3% (Note 1)	Analog Input maximum value tolerance
0 to 5%	0% (Note 2)	Analog Input minimum value tolerance

Note 1: When set to 4 or 5 %, the maximum voltage value of 3 % is applied.

Note 2: The minimum voltage error is always 0 regardless of the configured minimum voltage value.

Analog Input Error Settings:

Analog Output Operation Mode: 4 to 20 mA
Maximum value tolerance: 2%
Minimum value tolerance: 1%



Analog Output Parameters

Analog output parameters include the analog output signal type, analog output data type, analog output minimum and maximum values, analog output data, and analog output operating status. This section describes these parameters in detail.

Analog Output Signal Type

A total of three analog output signal types are available, depending on the analog I/O or analog output module. Select an analog output signal type for each analog output channel. When a channel is not used, select the default value or **Not used** for the channel.

Parameter		FC4A-L03A1	FC4A-L03AP1	FC4A-K1A1	FC4A-K2C1	FC4A-K4A1
0	Voltage output	0 to 10V DC			–10 to +10V DC	0 to 10V DC
1	Current output	4 to 20 mA DC				
255	Not used	—	—	—	X	X

Analog Output Data Type

A total of two analog output data types are available, depending on the analog I/O or analog output module. Select an analog output data type for each analog output channel.

Parameter			FC4A-L03A1	FC4A-L03AP1	FC4A-K1A1	FC4A-K2C1	FC4A-K4A1
0	Binary data	Voltage	0 to 4095			–25000 to 25000	0 to 4095
		Current				0 to 50000	
1	Optional range	Voltage	Analog output data minimum value to maximum value (–32768 to 32767)				
		Current					

Analog Output Minimum/Maximum Values

For analog output values, when Optional range is selected for the Data Type, designate the analog output data minimum and maximum values which can be –32,768 through 32,767.

Analog Output Data

The analog output data is converted into an analog output signal within the range specified by the analog output data type and applicable parameters. The analog output data register number is shown under Data in the Configure Parameters dialog box.

END Refresh Type

The analog output data stored in a data register, such as D772, is converted into an analog output signal of voltage output (0 to 10V DC) or current output (4 to 20 mA) as designated by the value stored in the data register allocated to analog output signal type, such as D774.

While the CPU module is running, the analog output data stored in the allocated data register is updated at the END processing of every scan or 10 ms, whichever is longer. While the CPU module is stopped, the analog output data remains at 0 or the designated analog output data minimum value, so the generated analog output signal remains at the minimum value of 0V DC or 4 mA DC.

Ladder Refresh Type

While the CPU module is running, the analog output data stored in the allocated data register is updated when the RUNA instruction contained in the ANST macro is executed. While the CPU module is stopped, the analog output data is not updated. But the analog output signal can be changed by using the STPA instruction. For details, see page 9-22.

Analog Output Operating Status

The operating status of each analog output channel is stored to a data register allocated to analog output operating status. While the analog output is operating normally, the data register stores 0. The analog output operating status data register number is shown under Status in the Configure Parameters dialog box.

END Refresh Type

The operating status of each analog output is stored to a data register, such as D773. While the analog output is operating normally, the data register stores 0. The analog output operating status data is updated whether the CPU module is running or stopped. The update occurs at the END processing of every scan or 10 ms, whichever is longer.

Status Code	Analog Output Operating Status (END refresh type)
0	Normal operation
1	(reserved)
2	Initializing
3	Invalid parameter or analog output channel not available on the installed analog module
4	Hardware failure (external power supply failure)

Ladder Refresh Type

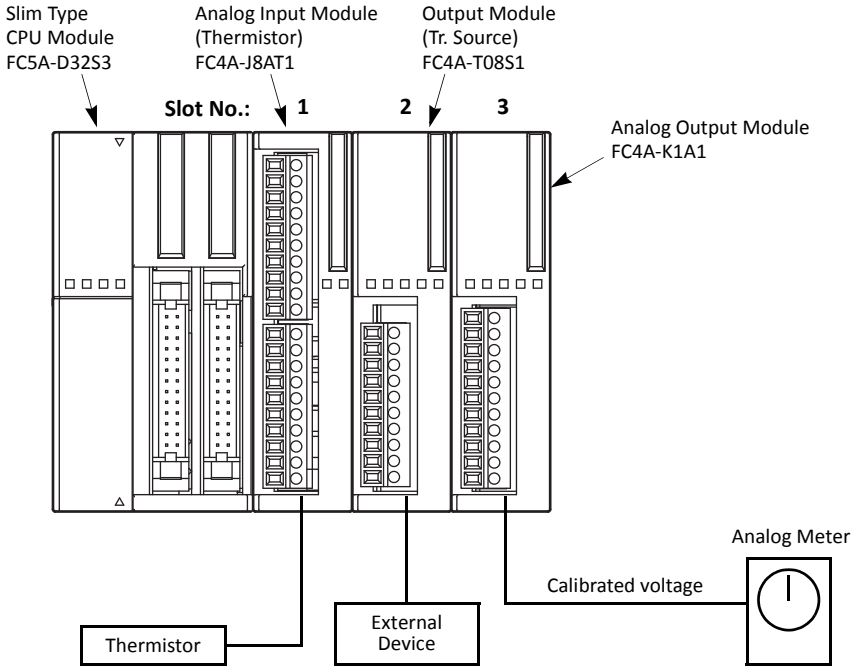
The operating status of each analog output channel is stored to a data register determined by the data register number selected in the Configure Parameters dialog box of the ANST macro.

Operating Status Bit		Analog Output Operating Status (Ladder refresh type)	
Bit 0	0	Operating status bit	Normal operation
	1		Initializing, changing configuration, hardware initialization error
Bit 1	0	Parameter bit	Parameter configuration normal
	1		Parameter configuration error
Bit 2	0	External power supply bit	External power supply normal
	1		External power supply error
Bit 3	0	Output data error bit	Output data normal
	1		Output data range error
Bit 4 to Bit 15	0	Reserved	Normal operation

Example: Analog I/O

The following example demonstrates a program of analog I/O control using an NTC thermistor. Two analog I/O modules are mounted in the slots shown below.

System Setup

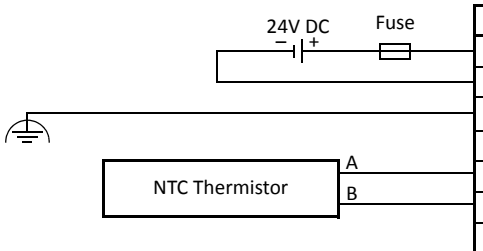


Operation

In this example, the input value from the NTC thermistor is calibrated. When the temperature reaches the preset value, the output is turned off. The thermistor temperature is monitored on an analog meter.

Wiring Diagram

FC4A-J8AT1 (Analog Input Module)

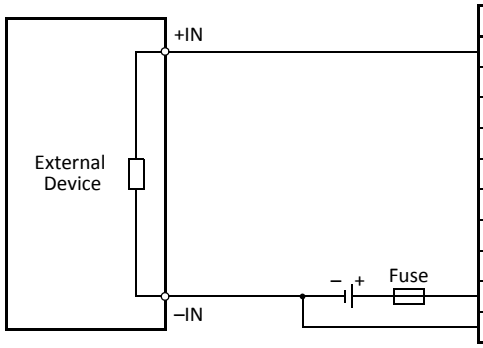


Terminal No.	Channel
24V	24V DC
0V	
⏚	
NC	—
A	IN0
B	
A	IN1
B	
A	IN2
B	
A	IN3
B	
A	IN4
B	
A	IN5
B	
A	IN6
B	
A	IN7
B	

• **Thermistor Specifications**

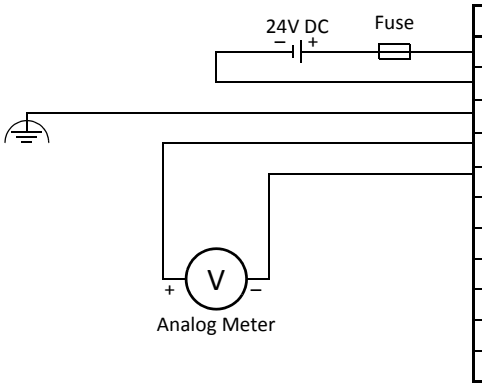
Type No.	NT731ATTD103K38J (KOA)
Type	NTC
RO	10,000Ω
T0	25°C
B Parameter	3,800K

FC4A-T08S1 (8-point Transistor Source Output Module)



Terminal No.	Output
0	Q0
1	Q1
2	Q2
3	Q3
4	Q4
5	Q5
6	Q6
7	Q7
COM(+)	COM(+)
–V	–V

FC4A-K1A1 (Analog Output Module)

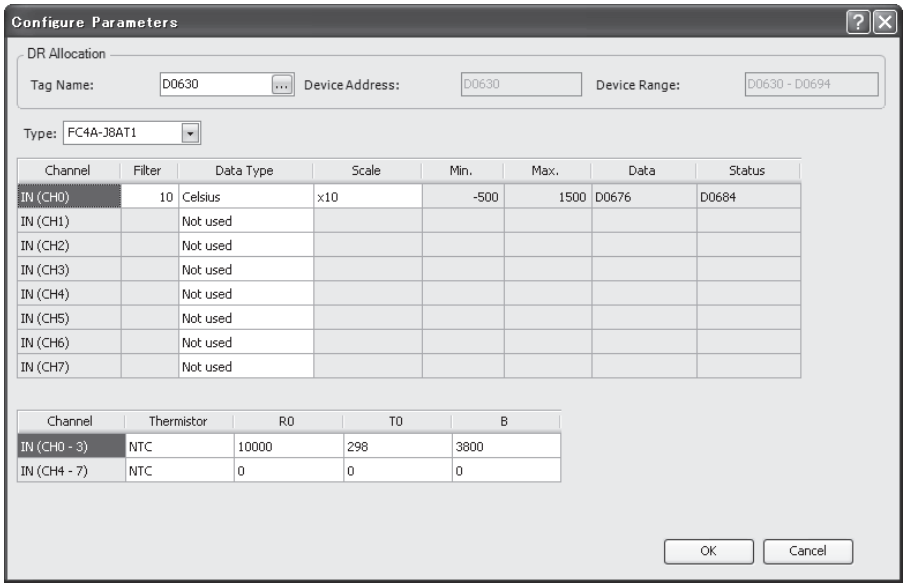


Terminal No.	Channel
+	24V DC
–	
⏚	
+	OUT
–	
NC	—
NC	
NC	
NC	—
NC	
NC	

WindLDR Programming

Analog I/O modules are programmed using the ANST macro in WindLDR. Program the ANST macro as shown below.

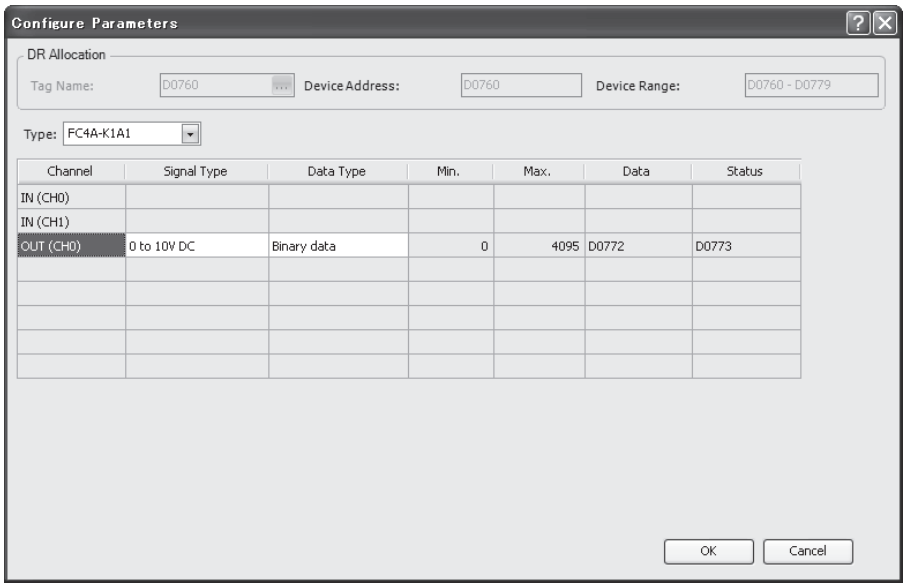
- **Analog Input Module FC4A-J8AT1 on Slot 1**



DR Allocation Range			Designation	Description
D630 - D694			D630	Optional range allocation, 65 words
I/O	**Channel**	**Item**	**Designation**	**Description**
IN	CH0	Filter	10	Averages input values
		Data Type	Celsius	Analog input range –50 to 150°C
		Scale	×10	Analog input data –500 to 1500
	CH1	Data Type	Not used	Unused channel
	CH2	Data Type	Not used	Unused channel
	CH3	Data Type	Not used	Unused channel
	CH4	Data Type	Not used	Unused channel
	CH5	Data Type	Not used	Unused channel
	CH6	Data Type	Not used	Unused channel
	CH7	Data Type	Not used	Unused channel
	CH0 - CH3	Thermistor Type	NTC	NTC thermistor
		R0	10,000	Resistance value at the absolute temperature = 10 kΩ
		T0	25	Temperature = 25°C
		B	3,800	B parameter = 3,800K

Note: When CH4 through CH7 are not used, thermistor settings are not required.

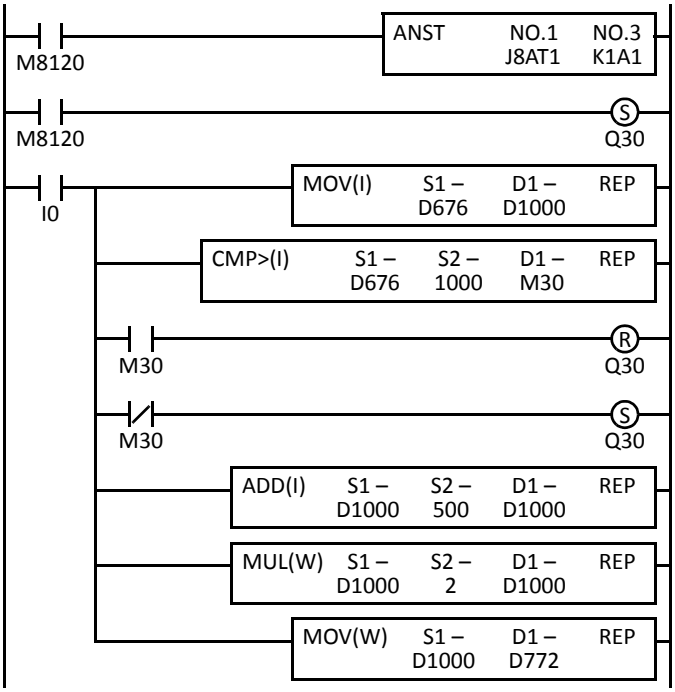
- **Analog Output Module FC4A-K1A1 on Slot 3**



DR Allocation Range			Designation	Description
D760 - D779			—	Automatic range allocation, 20 words
I/O	**Channel**	**Item**	**Designation**	**Description**
OUT	CH0	Signal Type	0 to 10V DC	Voltage output
		Data Type	Binary data	0 to 4095

Ladder Diagram

As shown in the ladder diagram below, when initialize pulse special internal relay M8120 is used for the ANST macro in parallel with another instruction, load M8120 again for the other instruction.



M8120 is the initialize pulse special internal relay.

When the CPU starts to run, ANST stores parameters to data registers to configure analog I/O modules and Q30 is turned on.

When I0 is turned on, analog input data is moved from D676 to D1000.

The temperature is compared with the alarm temperature of 100°C.

When the temperature is higher than 100°C, Q30 is turned off.

When the temperature is not higher than 100°C, Q30 is turned on.

Analog input data of –500 to +1500 is converted to 0 to 2000.

Analog input data of 0 to 2000 is converted to 0 to 4000.

Analog input data of 0 to 4000 is moved to D772 (analog output data) of the analog output module.

Note: The above ladder diagram is only an example and should be modified as required.

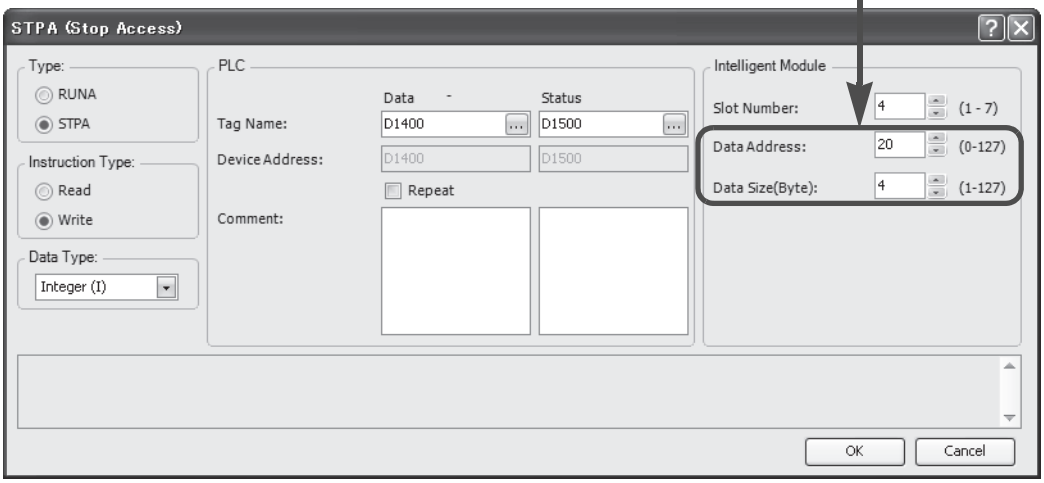
Changing Analog Output While CPU is Stopped

When using the FC4A-K2C1 analog output module, the analog output value can be changed while the CPU module is stopped. To change the analog output value, store a required output value to the memory addresses allocated to the analog output data.

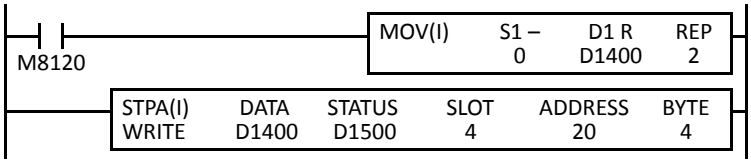
Example: Memory Allocation of Ladder Refresh Type Analog Output Module FC4A-K2C1

Memory Address (data address used for STPA)	Data Size (bytes)	R/W	Parameter	
+20	2	R/W	Analog Output Data	CH0
+22	2	R/W		CH1

STPA instruction when FC4A-K2C1 is mounted on slot 4



Ladder Diagram



M8120 is the initialize pulse special internal relay.

MOV stores output values at the OFF state.

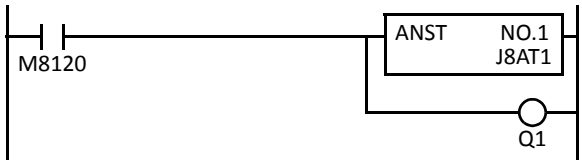
When the CPU stops, STPA updates the analog output value of the analog output module.

Note: The above ladder diagram is only an example and should be modified as required.

Precautions for Programming ANST Macro

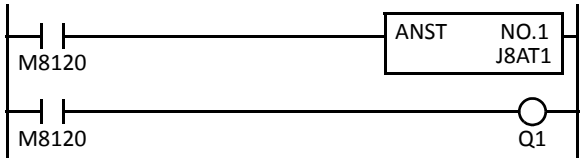
When using the ANST macro, do not make a branch from the ladder line of the ANST macro.

Incorrect



Delete the branch from the ANST macro, and start another line by inserting a LOD instruction.

Correct



10: USER COMMUNICATION INSTRUCTIONS

Introduction

This chapter describes the user communication function for communication between the MicroSmart and external devices with an RS232C or RS485 port, such as a computer, modem, printer, or barcode reader. The MicroSmart uses user communication instructions for transmitting and receiving communication to and from external devices.

For details about expansion RS232C/RS485 communication on port 3 to port 7, see page 25-1 (Advanced Vl.).

User Communication Overview

Every all-in-one CPU module has one RS232C port and port 2 connector as standard. By installing an optional RS232C communication adapter (FC4A-PC1) to the port 2 connector, the CPU module can communicate with two external devices simultaneously.

Every slim type CPU module has one RS232C port. An optional RS232C communication module can be attached to any slim type CPU module to use port 2 for additional RS232C communication. When an optional HMI base module is attached to a slim type CPU module, an optional RS232C communication adapter can be installed to the port 2 connector on the HMI base module.

When using an RS485 communication adapter or RS485 communication module for port 2, both all-in-one and slim type CPU modules can communicate with a maximum of 31 RS485 devices using the user communication.

User communication transmit and receive instructions can be programmed to match the communication protocol of the equipment to communicate with. Possibility of communication using the user communication mode can be determined referring to the user communication mode specifications described below.

User Communication Mode Specifications

Type	RS232C User Communication	RS485 User Communication
CPU Module and Communication Port	All CPU modules: Port 1 and Port 2 Expansion RS232C communication module: Port 3 to Port 7	All CPU modules: Port 2 Expansion RS485 communication module: Port 3 to Port 7
Maximum Nodes	1 per port	31 maximum
Standards	EIA RS232C	EIA RS485
Baud Rate	Ports 1 and 2: 1200, 2400, 4800, 9600, 19200, 38400, 57600 bps (Default: 9600) Ports 3 to 7: 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200 bps (Default: 9600) *1	
Data Bits	7 or 8 bits (Default: 7)	
Parity	Odd, Even, None (Default: Even)	
Stop Bits	1 or 2 bits (Default: 1)	
Receive Timeout	10 to 2540 ms (10-ms increments) or none (Receive timeout is disabled when 2550 ms is selected.) The receive timeout has an effect when using RXD instructions.	
Communication Method	Start-stop synchronization system	
Maximum Cable Length	2.4m	200m/1200m (When FC5A-SIF4 is used)
Maximum Transmit Data	200 bytes	
Maximum Receive Data	200 bytes	
BCC Calculation	XOR, ADD, ADD-2comp *, Modbus ASCII *, Modbus RTU * (* For calculation examples, see page 10-42.)	

***1:** To use 57600 or 115200 bps, the CPU modules with system program version 220 or higher and FC5A-SIF4 or FC5A-SIF2 (version 200 or higher) are required.

Connecting RS232C Equipment through RS232C Port 1 or 2

When using port 2 for RS232C communication on the all-in-one type CPU module, install the RS232C communication adapter (FC4A-PC1) to the port 2 connector.

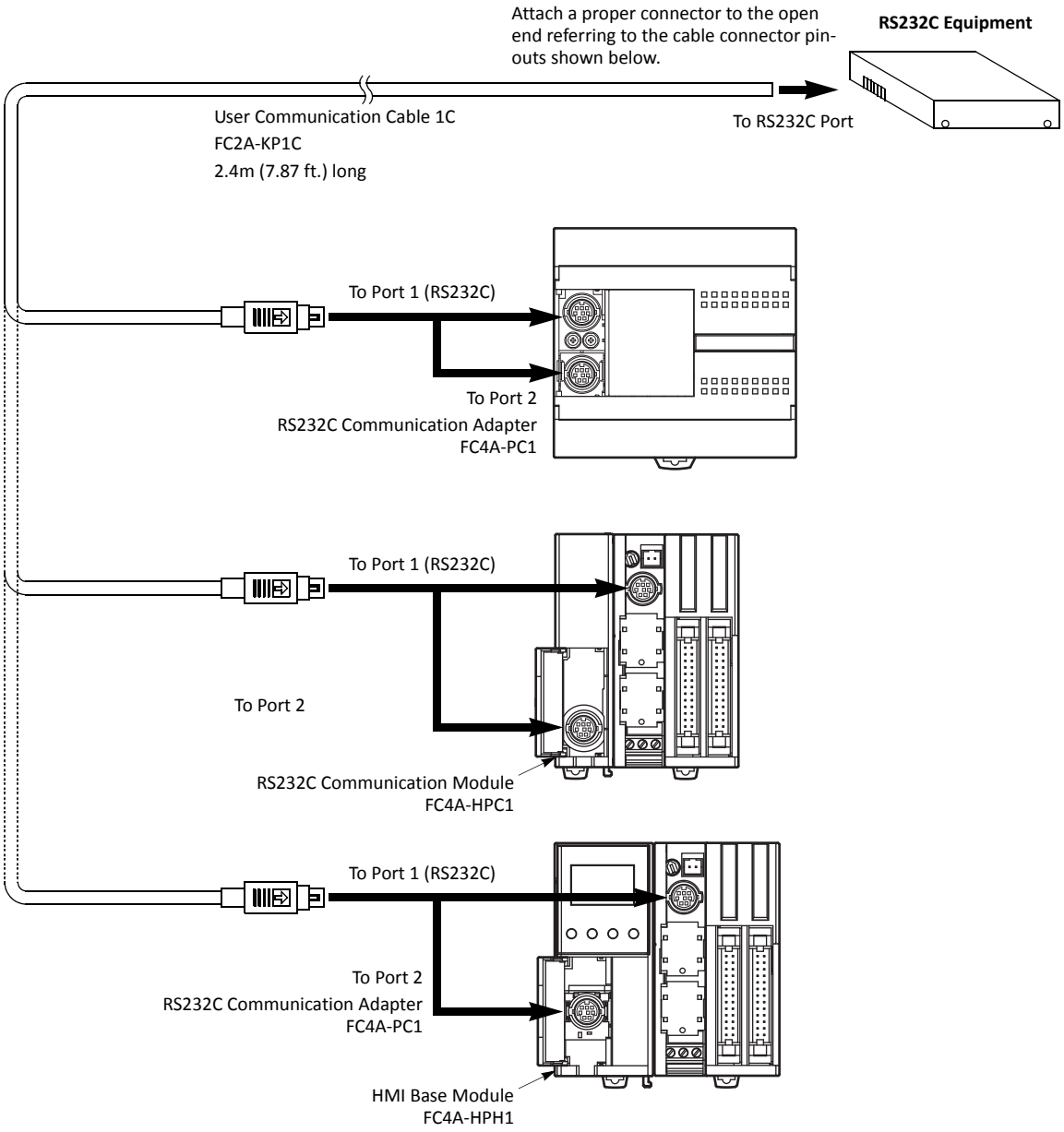
When using port 2 for RS232C communication on the slim type CPU module, mount the RS232C communication module (FC4A-HPC1) to the left of the CPU module.

When using port 2 for RS232C communication on the slim type CPU module with the optional HMI module, install the RS232C communication adapter (FC4A-PC1) to the port 2 connector on the HMI base module.

To connect an RS232C communication device to the RS232C port 1 or 2 on the MicroSmart CPU module, use the user communication cable 1C (FC2A-KP1C). One end of the user communication cable 1C is not provided with a connector, and can be terminated with a proper connector to plug in to communicate with the RS232C port. See the figure on page 10-3.

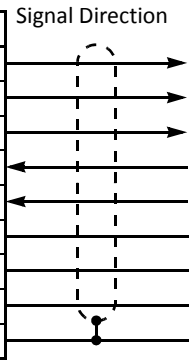
For details about expansion RS232C/RS485 communication on port 3 to port 7, see page 25-1 (Advanced Vl.).

RS232C User Communication System Setup



Cable Connector Pinouts

Pin	Port 1	Port 2	AWG#		Color
1	NC (no connection)	RTS (request to send)	28	Twisted	Black
2	NC (no connection)	DTR (data terminal ready)	28		Yellow
3	TXD (transmit data)	TXD (transmit data)	28		Blue
4	RXD (receive data)	RXD (receive data)	28		Green
5	NC (no connection)	DSR (data set ready)	28		Brown
6	CMSW (communication switch)	SG (signal ground)	28		Gray
7	SG (signal ground)	SG (signal ground)	26	Twisted	Red
8	NC (no connection)	NC (no connection)	26		White
Cover	—	—	—		Shield



Note: When preparing a cable for port 1, keep pins 6 and 7 open. If pins 6 and 7 are connected together, user communication cannot be used.

Connecting RS485 Equipment through RS485 Port 2

All MicroSmart CPU modules can use the RS485 user communication function. Using the RS485 user communication, a maximum of 31 RS485 devices can be connected to the MicroSmart CPU module.

When using port 2 for RS485 communication on the all-in-one type CPU module, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector.

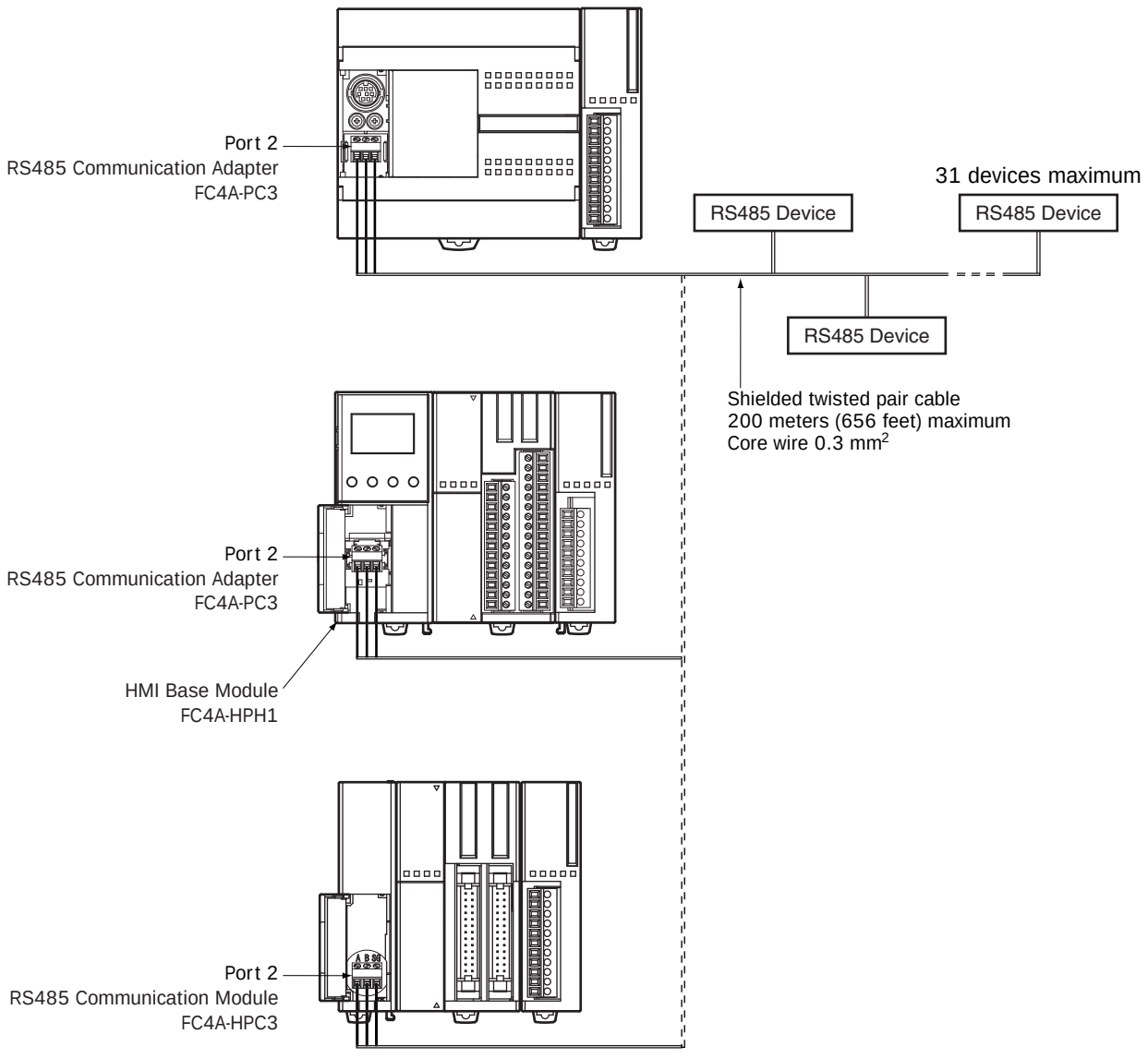
When using port 2 for RS485 communication on the slim type CPU module, mount the RS485 communication module (FC4A-HPC3) next to the CPU module.

When using port 2 for RS485 communication on the slim type CPU module with the optional HMI module, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector on the HMI base module (FC4A-HPH1).

Connect RS485 device to the RS485 terminals A, B, and SG of port 2 on the MicroSmart CPU module using a shielded twisted pair cable as shown below. The total length of the cable for the RS485 user communication can be extended up to 200 meters (656 feet).

For details about expansion RS232C/RS485 communication on port 3 to port 7, see page 25-1 (Advanced Vol.).

RS485 User Communication System Setup



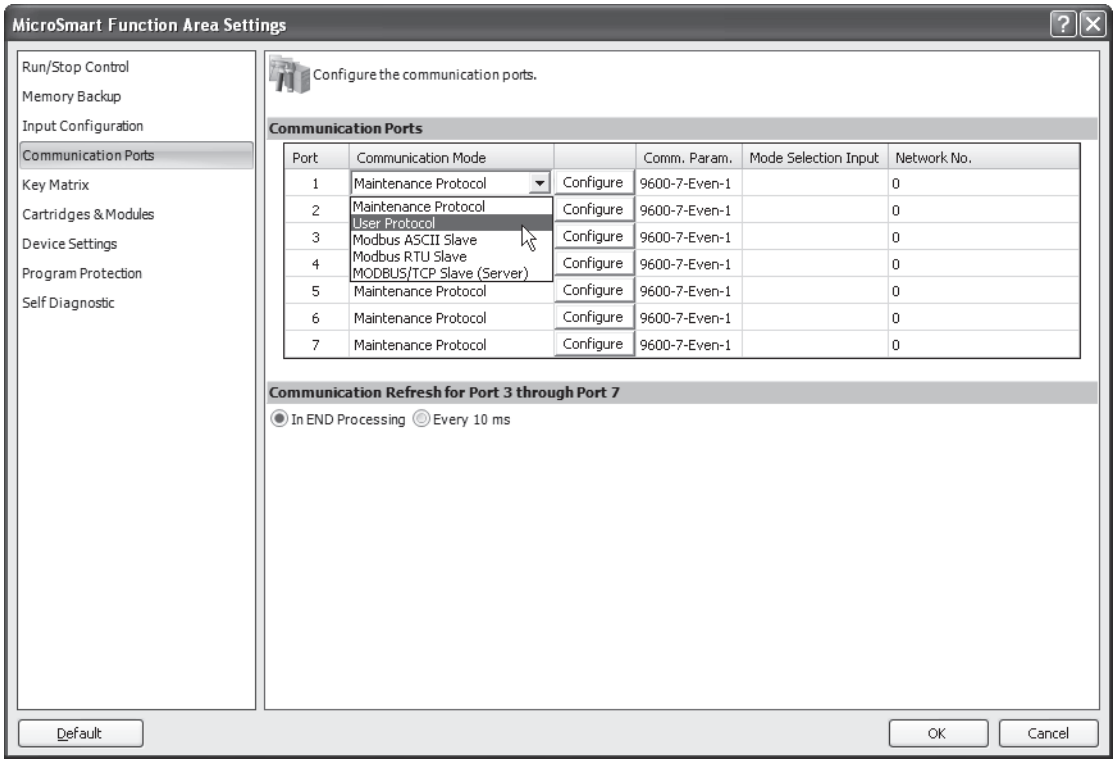
Programming WindLDR

When using the user communication function to communicate with an external RS232C or RS485 device, set the communication parameters for the MicroSmart to match those of the external device.

Note: Since communication parameters in the Function Area Settings relate to the user program, the user program must be downloaded to the MicroSmart CPU module after changing any of these settings.

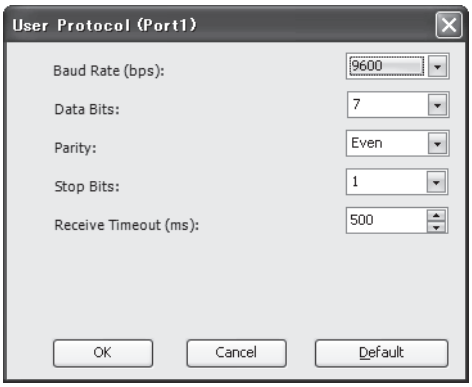
1. From the WindLDR menu bar, select **Configuration** > **Communication Ports**.

The Function Area Settings dialog box for Communication Ports appears.



2. In the Communication Mode pull-down list for Port 1 through Port 7, select **User Protocol**. (Click the **Configure** button when changing previous settings.)

The User Protocol dialog box appears.

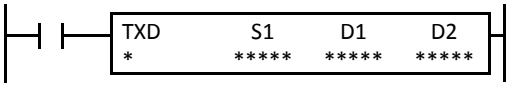


When **2550 ms** is selected in the Receive Timeout box, the receive timeout function is disabled.

3. Select communication parameters to the same values for the device to communicate with.

4. Click the **OK** button.

TXD (Transmit)



When input is on, data designated by S1 is converted into a specified format and transmitted from port 1 through port 7 to a remote terminal with an RS232C port.

TXD2 to TXD7 can be used to communicate with an RS485 remote terminal on port 2 to port 7.

TXD3 through TXD7 are available on upgraded CPU modules with system program version 110 or higher. For details about expansion RS232C/RS485 communication on port 3 to port 7, see page 25-1 (Advanced Vol.).

Applicable CPU Modules

FC5A-C10R2/C/D	FC5A-C16R2/C/D FC5A-C24R2D	FC5A-C24R2/C	FC5A-D16RK1/RS1	FC5A-D32K3/S3	FC5A-D12K1E/S1E
TXD1-TXD2	TXD1-TXD2	TXD1-TXD5	TXD1-TXD7	TXD1-TXD7	TXD2-TXD7

Valid Devices

Device	Function	I	Q	M	R	T	C	D	Constant	Repeat
S1 (Source 1)	Transmit data	—	—	—	—	—	—	X	X	—
D1 (Destination 1)	Transmit completion output	—	X	▲	—	—	—	—	—	—
D2 (Destination 2)	Transmit status register	—	—	—	—	—	—	X	—	—

For the valid device address range, see pages 6-1 and 6-2.

▲ Internal relays M0 through M2557 can be designated as D1. Special internal relays cannot be designated as D1.

Transmit data designated by device S1 can be a maximum of 200 bytes.

When transmission is complete, an output or internal relay, designated by device D1, is turned on.

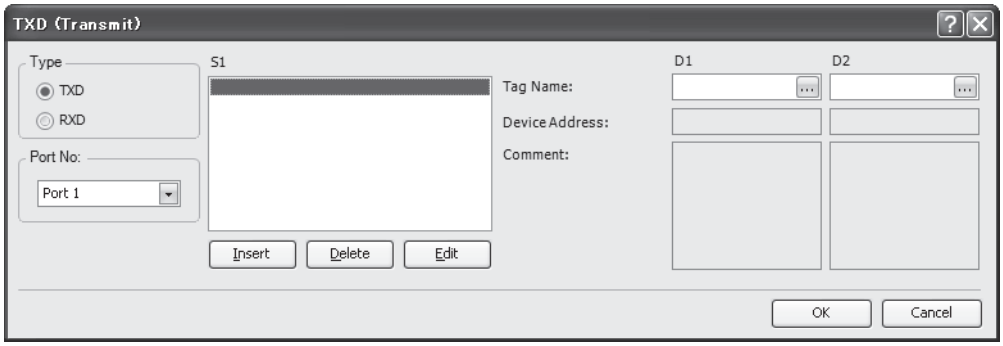
Destination 2 occupies two consecutive data registers starting with the device designated by D2. The transmit status data register, D0-D1998, D2000-D7998, or D10000-D49998, stores the status of transmission and error code. The next data register stores the byte count of transmitted data. The same data registers can not be used as transmit status registers for TXD1 through TXD7 instructions and receive status registers for RXD1 through RXD7 instructions.

The TXD instructions cannot be used in an interrupt program. If used, a user program execution error will result, turning on special internal relay M8004 and the ERR LED on the CPU module.

Precautions for Programming TXD Instruction

- The MicroSmart has five formatting areas each for executing TXD1 through TXD7 instructions, so five instructions each of TXD1 through TXD7 can be processed at the same time. If inputs to more than five of the same TXD instruction are turned on at the same time, an error code is set to the transmit status data register, designated by device D2, in the excessive TXD instructions that cannot be executed.
- If the input for a TXD instruction is turned on while another TXD instruction is executed, the subsequent TXD instruction is executed 2 scan times after the preceding TXD instruction is completed.
- Since TXD instructions are executed in each scan while input is on, a pulse input from a SOTU or SOTD instruction should be used as required.

User Communication Transmit Instruction Dialog Box in WindLDR



Selections and Devices in Transmit Instruction Dialog Box

Type	**TXD**	Transmit instruction
	RXD	Receive instruction
Port	**Port 1 - Port 7**	Transmit user communication from port 1 (TXD1) through port 7 (TXD7)
S1	**Source 1**	Enter the data to transmit in this area. Transmit data can be constant values (character or hexadecimal), data registers, or BCC.
D1	**Destination 1**	Transmit completion output can be an output or internal relay.
D2	**Destination 2**	Transmit status register can be data register D0-D1998, D2000-D7998, or D10000-D49998. The next data register stores the byte count of transmitted data.

Transmit Data

Transmit data is designated by source device S1 using constant values or data registers. BCC code can also be calculated automatically and appended to the transmit data. One TXD instruction can transmit 200 bytes of data at the maximum.

S1 (Source 1)

Transmit Data	Device	Conversion Type	Transmit Digits (Bytes)	Repeat	BCC Calculation	Calculation Start Position
Constant	00h-7Fh (FFh)	No conversion	1	—	—	—
Data Register	D0-D1999 D2000-D7999 D10000-D49999	A: Binary to ASCII B: BCD to ASCII –: No conversion	1-4 1-5 1-2	1-99	—	—
BCC	—	A: Binary to ASCII –: No conversion	1-2	—	X: XOR A: ADD C: Add-2comp M: Modbus ASCII M: Modbus RTU	1-15

Designating Constant as S1

When a constant value is designated as source device S1, one-byte data is transmitted without conversion. The valid transmit data value depends on the data bits selected in the Communication Parameters dialog box, which is called from **Configuration** > **Comm. Ports**, followed by selecting **User Protocol** in Port 1 through Port 7 list box and clicking the **Configure** button. When 7 data bits are selected as default, 00h through 7Fh is transmitted. When 8 data bits are selected, 00h through FFh is transmitted. Constant values are entered in character or hexadecimal notation into the source data.

Constant (Character)

Any character available on the computer keyboard can be entered. One character is counted as one byte.

Constant (Hexadecimal)

Use this option to enter the hexadecimal code of any ASCII character. ASCII control codes NUL (00h) through US (1Fh) can also be entered using this option.

Example:

The following example shows two methods to enter 3-byte ASCII data “1” (31h), “2” (32h), “3” (33h).

(1) Constant (Character)

(2) Constant (Hexadecimal)

Designating Data Register as S1

When a data register is designated as source device S1, conversion type and transmit digits must also be designated. The data stored in the designated data register is converted and a designated quantity of digits of the resultant data is transmitted. Conversion types are available in Binary to ASCII, BCD to ASCII, and no conversion.

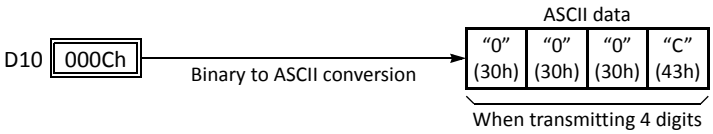
When repeat is designated, data of data registers as many as the repeat cycles are transmitted, starting with the designated data register. Repeat cycles can be up to 99.

Conversion Type

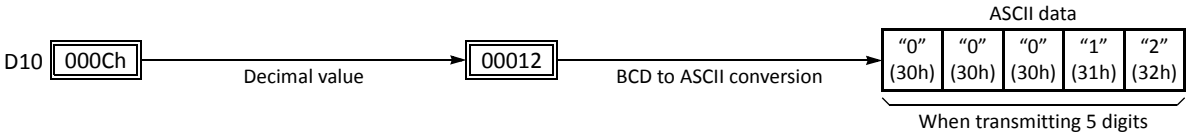
The transmit data is converted according to the designated conversion type as described below:

Example: D10 stores 000Ch (12)

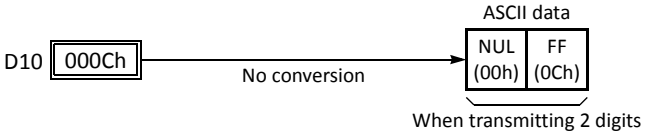
(1) Binary to ASCII conversion



(2) BCD to ASCII conversion



(3) No conversion

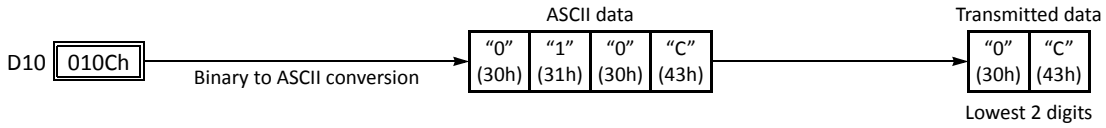


Transmit Digits (Bytes)

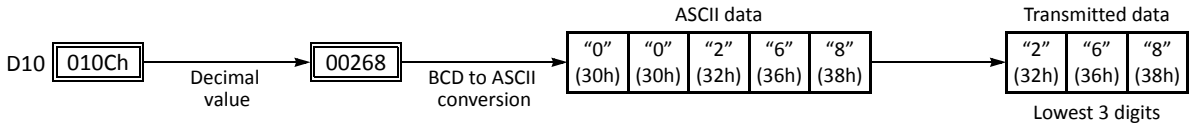
After conversion, the transmit data is taken out in specified digits. Possible digits depend on the selected conversion type.

Example: D10 stores 010Ch (268)

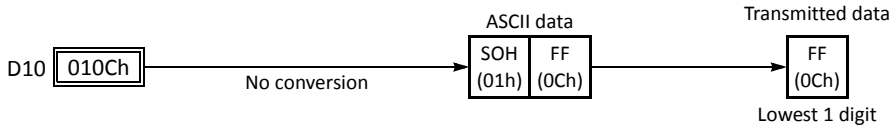
(1) Binary to ASCII conversion, Transmit digits = 2



(2) BCD to ASCII conversion, Transmit digits = 3



(3) No conversion, Transmit digits = 1



Repeat Cycles

When a data register is designated to repeat, consecutive data registers, as many as the repeat cycles, are used for transmit data in the same conversion type and transmit digits.

Example:

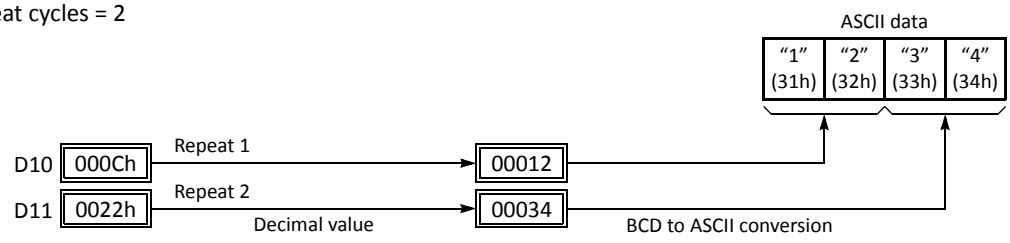
Data register No.: D10

Transmit digits: 2

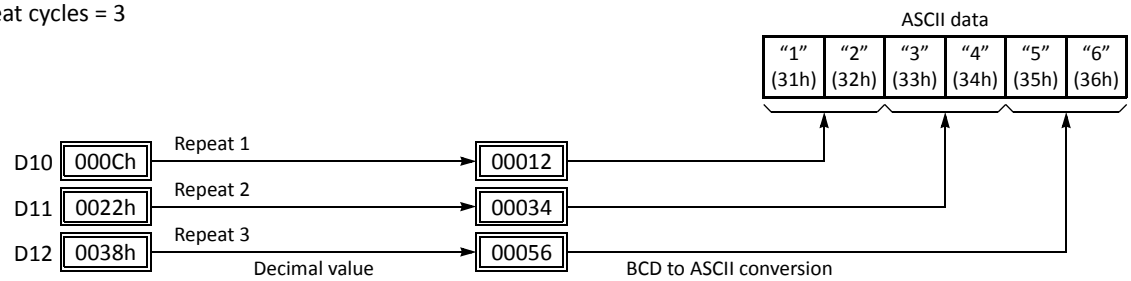
Conversion type: BCD to ASCII

Data of data registers starting with D10 is converted in BCD to ASCII and is transmitted according to the designated repeat cycles.

(1) Repeat cycles = 2

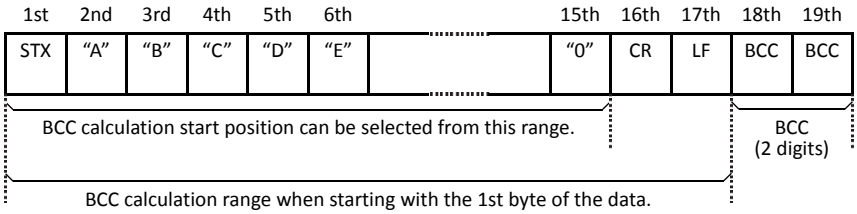


(2) Repeat cycles = 3



BCC (Block Check Character)

Block check characters can be appended to the transmit data. The start position for the BCC calculation can be selected from the first byte through the 15th byte. The BCC can be 1 or 2 digits.

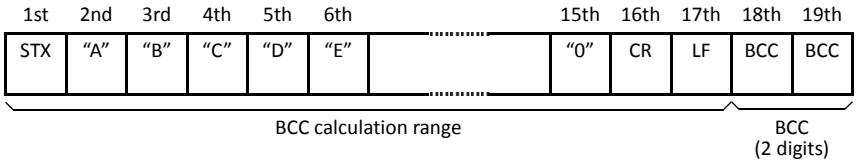


BCC Calculation Start Position

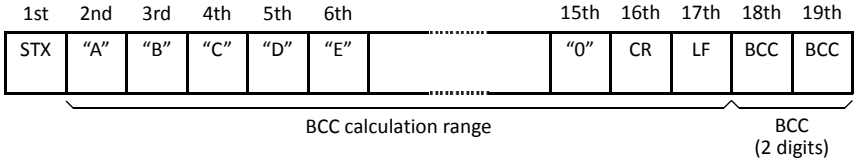
The start position for the BCC calculation can be specified from the first byte through the 15th byte. The BCC is calculated for the range starting at the designated position up to the byte immediately before the BCC of the transmit data.

Example: Transmit data consists of 17 bytes plus 2 BCC digits.

(1) Calculation start position = 1



(2) Calculation start position = 2



BCC Calculation Formula

BCC calculation formula can be selected from XOR (exclusive OR), ADD (addition), ADD-2comp, Modbus ASCII, or Modbus RTU.

Example: Conversion results of transmit data consist of 41h, 42h, 43h, and 44h.

ASCII data

"A" (41h)	"B" (42h)	"C" (43h)	"D" (44h)

(1) BCC calculation formula = XOR

Calculation result = 41h ⊕ 42h ⊕ 43h ⊕ 44h = 04h

(2) BCC calculation formula = ADD

Calculation result = 41h + 42h + 43h + 44h = 10Ah → 0Ah (Only the last 1 or 2 digits are used as BCC.)

(3) BCC calculation formula = ADD-2comp

Calculation result = FEh, F6h (2 digits without conversion)

(4) BCC calculation formula = Modbus ASCII

Calculation result = 88 (ASCII)

(5) BCC calculation formula = Modbus RTU

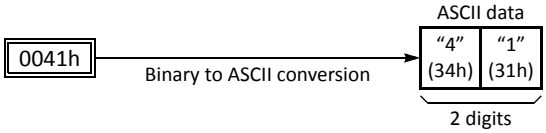
Calculation result = 85h 0Fh (binary)

Conversion Type

The BCC calculation result can be converted or not according to the designated conversion type as described below:

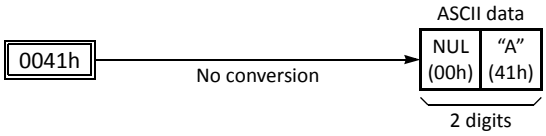
Example: BCC calculation result is 0041h.

(1) Binary to ASCII conversion



Note: On WindLDR, Modbus ASCII is defaulted to binary to ASCII conversion.

(2) No conversion

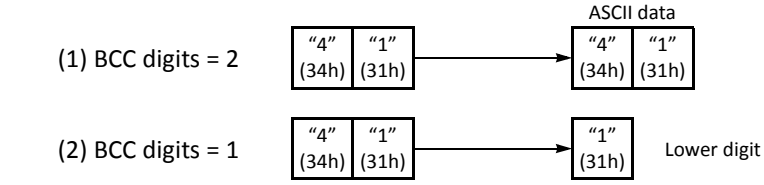


Note: On WindLDR, Modbus RTU is defaulted to no conversion.

BCC Digits (Bytes)

The quantity of digits (bytes) of the BCC code can be selected from 1 or 2.

Example:



Note: On WindLDR, Modbus ASCII and Modbus RTU are defaulted to 2 digits.

Transmit Completion Output

Designate an output, Q0 through Q627, or an internal relay, M0 through M2557, as a device for the transmit completion output. Special internal relays cannot be used.

When the start input for a TXD instruction is turned on, preparation for transmission is initiated, followed by data transmission. When a sequence of all transmission operation is complete, the designated output or internal relay is turned on.

Transmit Status

Designate a data register, D0-D1998, D2000-D7998, or D10000-D49998, as a device to store the transmit status information including a transmission status code and a user communication error code.

Transmit Status Code

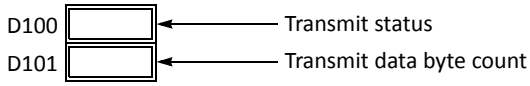
Transmit Status Code	Status	Description
16	Preparing transmission	From turning on the start input for a TXD instruction, until the transmit data is stored in the internal transmit buffer
32	Transmitting data	From enabling data transmission by an END processing, until all data transmission is completed
48	Data transmission complete	From completing all data transmission, until the END processing is completed for the TXD instruction
64	Transmit instruction complete	All transmission operation is completed and the next transmission is made possible

If the transmit status code is other than shown above, an error of transmit instruction is suspected. See User Communication Error Code on page 10-32.

Transmit Data Byte Count

The data register next to the device designated for transmit status stores the byte count of data transmitted by the TXD instruction. When BCC is included in the transmit data, the byte count of the BCC is also included in the transmit data byte count.

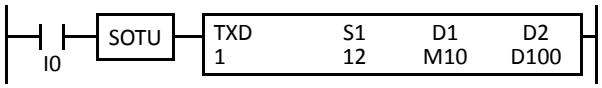
Example: Data register D100 is designated as a device for transmit status.



Programming TXD Instruction Using WindLDR

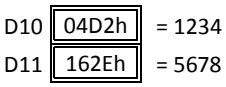
The following example demonstrates how to program a TXD instruction including a start delimiter, BCC, and end delimiter using WindLDR.

TXD sample program:

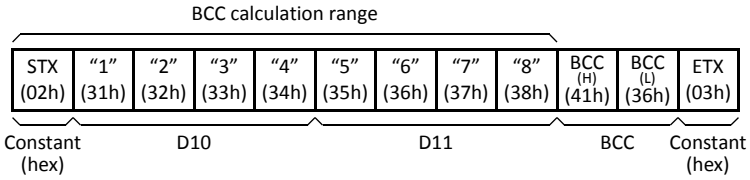


Communication port:	Port 1
Transmit completion output:	M10
Transmit status register:	D100
Transmit data byte count:	D101

Data register contents:

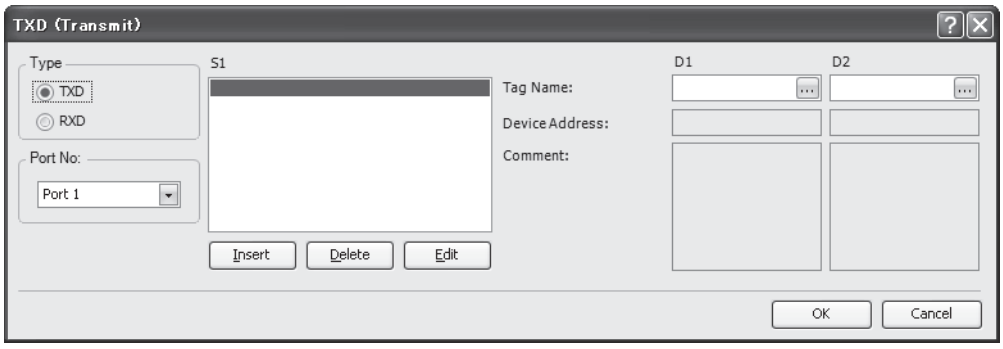


Transmit data example:



1. Start to program a TXD instruction. Move the cursor where you want to insert the TXD instruction, and type **TXD**. You can also insert the TXD instruction by clicking the User Communication icon in the menu bar and clicking where you want to insert the TXD instruction in the program edit area.

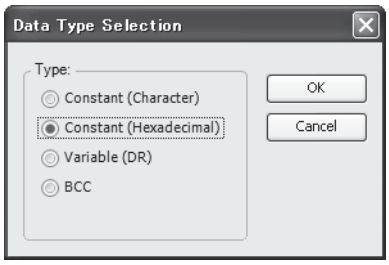
The Transmit instruction dialog box appears.

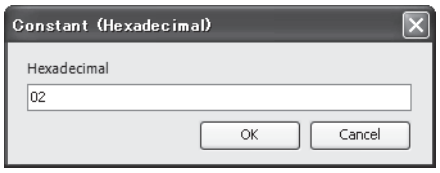


2. Check that **TXD** is selected in the Type box and select **Port 1** in the Port box. Then, click **Insert**.

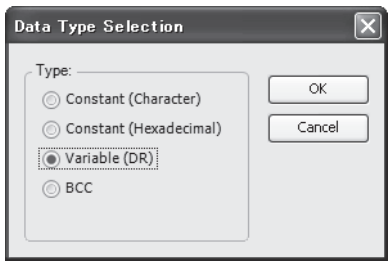
The Data Type Selection dialog box appears. You will program source device S1 using this dialog box.

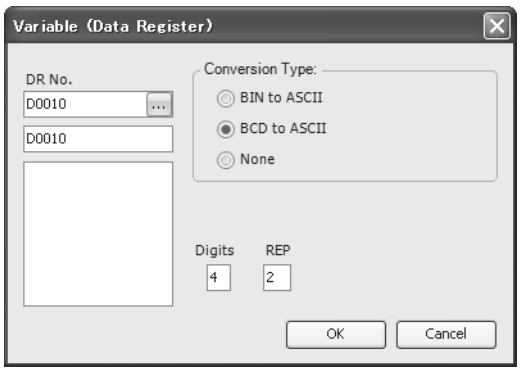
3. Click **Constant (Hexadecimal)** in the Type box and click **OK**. Next, in the Constant (Hexadecimal) dialog box, type **02** to program the start delimiter STX (02h). When finished, click **OK**.



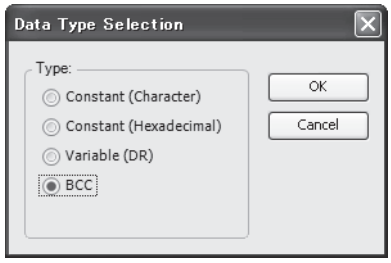


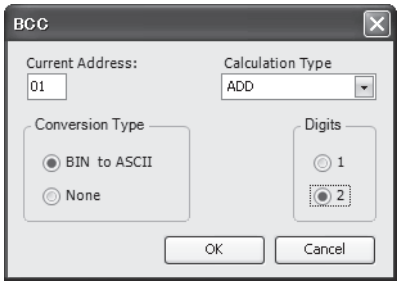
4. Since the Transmit instruction dialog box reappears, repeat the above procedure. In the Data Type Selection dialog box, click **Variable (DR)** and click **OK**. Next, in the Variable (Data Register) dialog box, type **D10** in the DR No. box and click **BCD to ASCII** to select the BCD to ASCII conversion. Enter **4** in the Digits box (4 digits) and **2** in the REP box (2 repeat cycles). When finished, click **OK**.



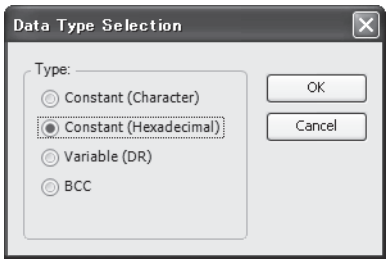


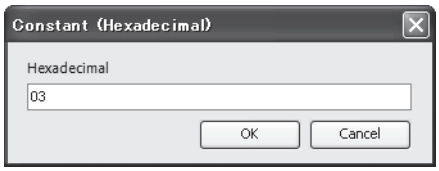
5. Again in the Data Type Selection dialog box, click **BCC** and click **OK**. Next, in the BCC dialog box, enter **1** in the Calculation Start Position box, select **ADD** for the Calculate Type, click **BIN to ASCII** for the Conversion Type, and click **2** for the Digits. When finished, click **OK**.



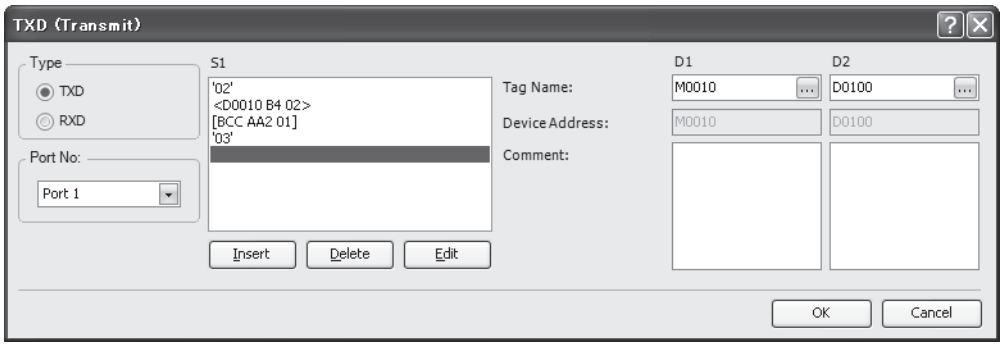


6. Once again in the Data Type Selection dialog box, click **Constant (Hexadecimal)** and click **OK**. Next, in the Constant (Hexadecimal) dialog box, type **03** to program the end delimiter ETX (03h). When finished, click **OK**.

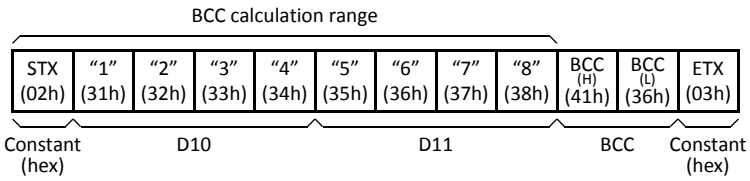




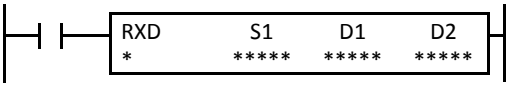
7. In the Transmit instruction dialog box, type **M10** in the destination D1 box and type **D100** in the destination D2 box. When finished, click **OK**.



Programming of the TXD1 instruction is complete and the transmit data is specified as follows:



RXD (Receive)



When input is on, data from an RS232C remote terminal received by port 1 through port 7 is converted and stored in data registers according to the receive format designated by S1.

RXD2 to RXD7 can be used to communicate with an RS485 remote terminal on port 2 to port 7.

RXD3 through RXD7 are available on upgraded CPU modules with system program version 110 or higher. For details about expansion RS232C/RS485 communication on port 3 to port 7, see page 25-1 (Advanced Vol.).

Applicable CPU Modules

FC5A-C10R2/C/D	FC5A-C16R2/C/D FC5A-C24R2D	FC5A-C24R2/C	FC5A-D16RK1/RS1	FC5A-D32K3/S3	FC5A-D12K1E/S1E
RXD1-RXD2	RXD1-RXD2	RXD1-RXD5	RXD1-RXD7	RXD1-RXD7	RXD2-RXD7

Valid Devices

Device	Function	I	Q	M	R	T	C	D	Constant	Repeat
S1 (Source 1)	Receive format	—	—	—	—	—	—	X	X	—
D1 (Destination 1)	Receive completion output	—	X	▲	—	—	—	—	—	—
D2 (Destination 2)	Receive status	—	—	—	—	—	—	X	—	—

For the valid device address range, see pages 6-1 and 6-2.

▲ Internal relays M0 through M2557 can be designated as D1. Special internal relays cannot be designated as D1.

Receive format designated by device S1 can be a maximum of 200 bytes.

When data receive is complete, an output or internal relay, designated by device D1, is turned on.

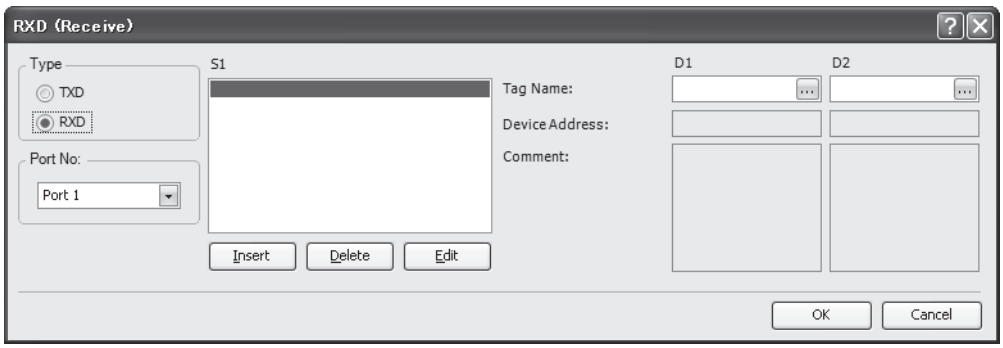
Destination 2 occupies two consecutive data registers starting with the device designated by D2. The receive status data register, D0-D1998, D2000-D7998, or D10000-D49998, stores the status of data receive and error code. The next data register stores the byte count of received data. The same data registers can not be used as transmit status registers for TXD1 through TXD7 instructions and receive status registers for RXD1 through RXD7 instructions.

The RXD instructions cannot be used in an interrupt program. If used, a user program execution error will result, turning on special internal relay M8004 and the ERR LED on the CPU module.

Precautions for Programming the RXD Instruction

- The MicroSmart can execute a maximum of five instructions each of RXD1 through RXD7 that have a start delimiter at the same time. If a start delimiter is not programmed in RXD1 through RXD7 instructions, the MicroSmart can execute only one instruction each of RXD1 through RXD7 at a time. If the start input for a RXD1 through RXD7 instruction is turned on while another RXD1 through RXD7 instruction without a start delimiter is executed, a user communication error occurs.
- Since RXD instructions are executed in each scan while input is on, a pulse input from a SOTU or SOTD instruction should be used as required.
- Once the input to the RXD instruction is turned on, the RXD is activated and ready for receiving incoming communication even after the input is turned off. When the RXD completes data receiving, the RXD is deactivated if the input to the RXD is off. Or, if the input is on, the RXD is made ready for receiving another communication. Special internal relays are available to deactivate all RXD instructions waiting for incoming communication. For user communication receive instruction cancel flags, see page 10-28.

User Communication Receive Instruction Dialog Box in WindLDR



Selections and Devices in Receive Instruction Dialog Box

Type	**TXD**	Transmit instruction
	RXD	Receive instruction
Port	**Port 1 - Port 7**	Receive user communication to port 1 (RXD1) through port 7 (RXD7)
S1	**Source 1**	Enter the receive format in this area. The receive format can include a start delimiter, data register to store incoming data, constants, end delimiter, BCC, and skip.
D1	**Destination 1**	Receive completion output can be an output or internal relay.
D2	**Destination 2**	Receive status register can be data register D0-D1998, D2000-D7998, or D10000-D49998. The next data register stores the byte count of received data.

Receive Format

Receive format, designated by source device S1, specifies data registers to store received data, data digits for storing data, data conversion type, and repeat cycles. A start delimiter and an end delimiter can be included in the receive format to discriminate valid incoming communication. When some characters in the received data are not needed, “skip” can be used to ignore a specified number of characters. BCC code can also be appended to the receive format to verify the received data. One RXD instruction can receive 200 bytes of data at the maximum.

Constants for verification can be included in the middle of the receive format when using CPU modules with system program version 200 or higher.

S1 (Source 1)

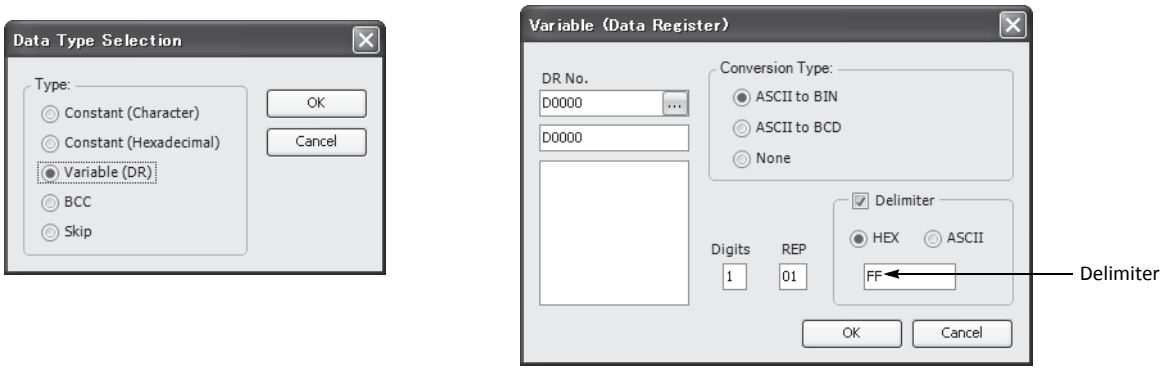
Receive Format	Device	Receive Digits (Bytes)	Conversion Type	Repeat	BCC Calculation	Calculation Start Position	Skip Bytes	Delimiter
Data Register	D0-D1999 D2000-D7999 D10000-D49999	1-4 1-5 1-2	A: ASCII to Binary B: ASCII to BCD –: No conversion	1-99	—	—	—	Hex ASCII
Start Delimiter	00h-FFh 1 to 5 bytes	—	No conversion	—	—	—	—	
End Delimiter	00h-FFh	—	No conversion	—	—	—	—	
Constant for Verification	00h-FFh	—	No conversion	—	—	—	—	
BCC	—	1-2	A: Binary to ASCII –: No conversion	—	X: XOR A: ADD C: Add-2comp M: Modbus ASCII M: Modbus RTU	1-15	—	
Skip	—	—	—	—	—	—	1-99	

Designating Data Register as S1

When a data register is designated as source device S1, receive digits and conversion type must also be designated. The received data is divided into blocks of specified receive digits, converted in a specified conversion type, and stored to the designated data registers. Conversion types are available in ASCII to Binary, ASCII to BCD, and no conversion.

When repeat is designated, received data is divided, converted, and stored into data registers as many as the repeat cycles, starting with the designated data register. Repeat cycles can be up to 99.

When a data register is designated as source device S1, a delimiter can be included in the data register designation to end receiving communication. This option is available when using CPU modules with system program version 200 or higher and WindLDR 5.2 or higher.

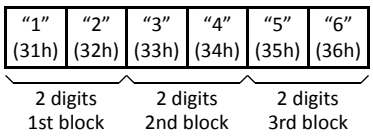


Receive Digits

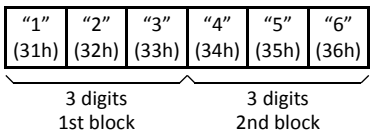
The received data is divided into blocks of specified receive digits before conversion as described below:

Example: Received data of 6 bytes are divided in different receive digits. (Repeat is also designated.)

(1) Receive digits = 2



(2) Receive digits = 3

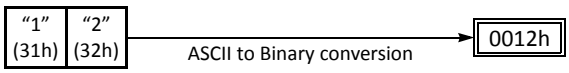


Conversion Type

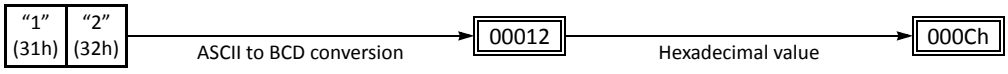
The data block of the specified receive digits is then converted according to the designated conversion type as described below:

Example: Received data has been divided into a 2-digit block.

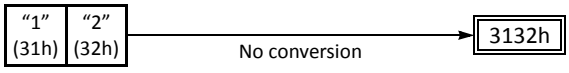
(1) ASCII to Binary conversion



(2) ASCII to BCD conversion



(3) No conversion

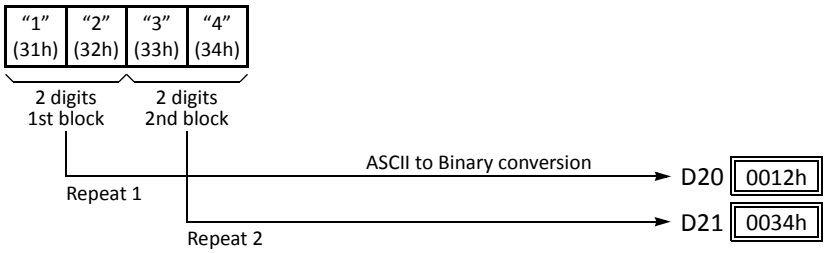


Repeat Cycles

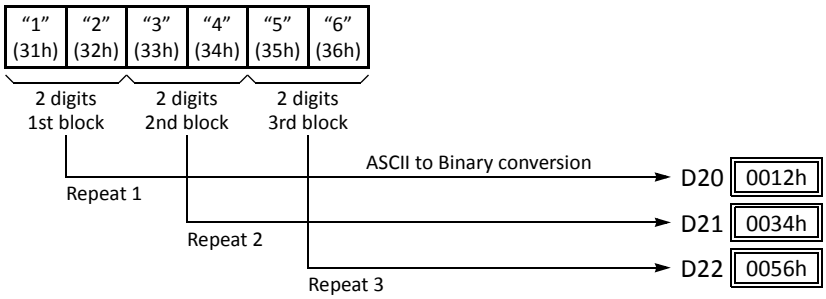
When a data register is designated to repeat, the received data is divided and converted in the same way as specified, and the converted data is stored to consecutive data registers as many as the repeat cycles.

Example: Received data of 6 bytes is divided into 2-digit blocks, converted in ASCII to Binary, and stored to data registers starting at D20.

(1) Repeat cycles = 2



(2) Repeat cycles = 3



Delimiter (System program 200 or higher)

A delimiter for the data register in the receive format can be designated. Using a delimiter, incoming data of variable length can be received and stored to data registers.

Delimiter	How the incoming data is stored to data registers
Designated	The incoming data is stored to data registers until all the data specified with receive digits, conversion type, and repeat is processed or the specified delimiter is received.
No delimiter	The incoming data is stored to data registers until all the data specified with receive digits, conversion type, and repeat is processed.

Note: Delimiters for data registers can be used in the receive format of RXD instructions only.

Delimiters can be used only when using CPU modules with system program version 200 or higher and WindLDR 5.2 or higher, and can be selected from one-byte Hex values or ASCII characters.

Designating Constant as Start Delimiter

A start delimiter can be programmed at the first byte in the receive format of a RXD instruction; the MicroSmart will recognize the beginning of valid communication, although a RXD instruction without a start delimiter can also be executed.

When a constant value is designated at the first byte of source device S1, the one-byte data serves as a start delimiter to start the processing of the received data.

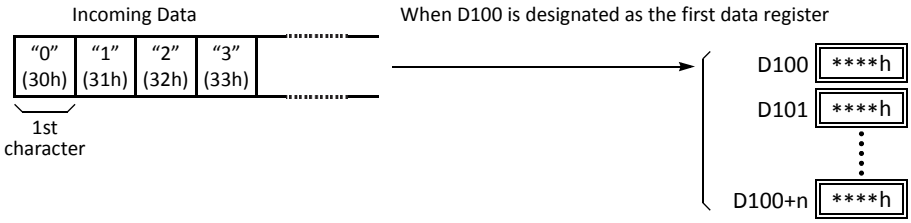
A maximum of five instructions each of RXD1 through RXD7 with different start delimiters can be executed at the same time. When the first byte of the incoming data matches the start delimiter of a RXD instruction, the received data is processed and stored according to the receive format specified in the RXD instruction. If the first byte of the incoming data does not match the start delimiter of any RXD instruction that is executed, the MicroSmart discards the incoming data and waits for the next communication.

While a RXD instruction without a start delimiter is executed, any incoming data is processed continuously according to

the receive format. Only one instruction each of RXD1 through RXD7 without a start delimiter can be executed at a time. If start inputs to two or more RXD instructions without a start delimiter are turned on simultaneously, one at the smallest address is executed and the corresponding completion output is turned on.

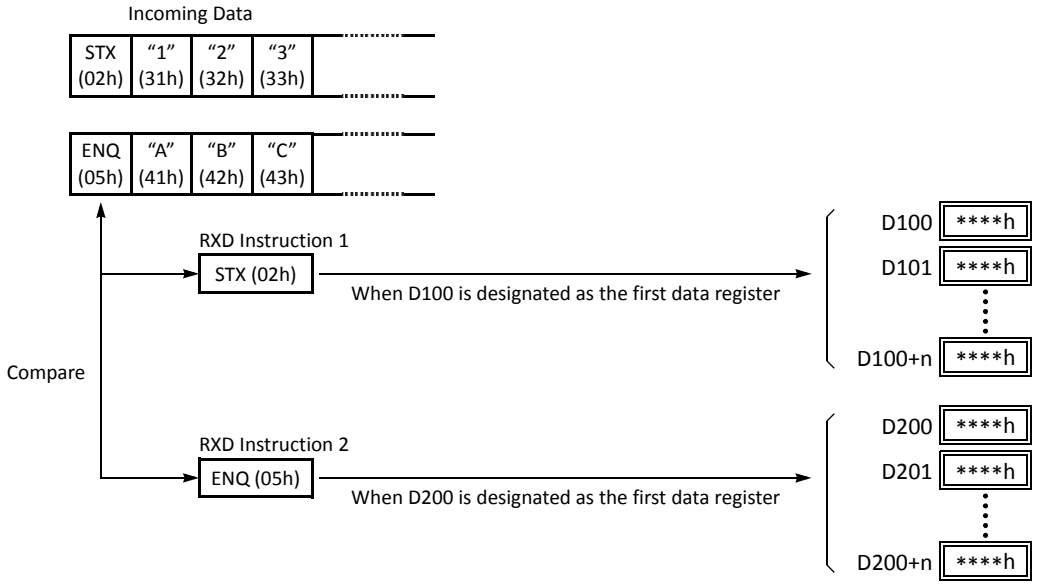
Example:

(1) When a RXD instruction without a start delimiter is executed



The incoming data is divided, converted, and stored to data registers according to the receive format.

(2) When RXD instructions with start delimiters STX (02h) and ENQ (05h) are executed



The incoming data is divided, converted, and stored to data registers according to the receive format. Start delimiters are not stored to data registers.

Multi-byte Start Delimiter (System program 200 or higher)

Multi-byte start delimiter is available on the CPU modules with system program version 200 or higher.

A start delimiter can be programmed at the first bytes in the receive format of a RXD instruction; the MicroSmart will recognize the beginning of valid communication, although a RXD instruction without a start delimiter can also be executed. A maximum of 5 consecutive constants that are either character or hexadecimal from the first byte of the receive format are considered a multi-byte start delimiter.

If a RXD instruction with a start delimiter is executed and another RXD instruction with the same start delimiter is executed, user communication error code 5 is stored in the data register designated as the receive status of the second RXD instruction. When the error occurs, the second RXD instruction is canceled, and the first RXD instruction keeps executed.

If a multi-byte start delimiter is designated, and the incoming data does not match the entire multi-byte start delimiter, the MicroSmart discards the incoming data and waits for the next communication.

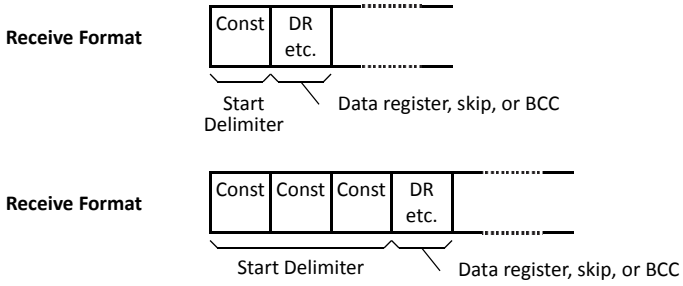
When the first one byte is received, a timer is started to monitor the interval between incoming data even when a multi-byte start delimiter is designated. If data is not received in the period specified for the receive timeout value after receiving one byte of data, a receive timeout error occurs, and user communication error code 11 is stored in the status data

register.

Examples: Multi-byte Start Delimiter

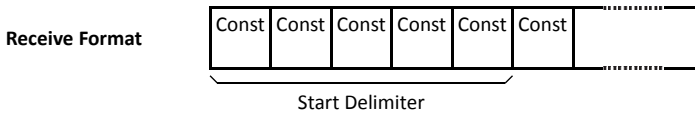
Multi-byte start delimiter is determined in the structure of the Receive Format. The following examples show how multi-byte start delimiter is determined.

• Constants are followed by data register, skip, or BCC



Note: Constants following data register, skip, or BCC are not considered start delimiter even if these are in the first five bytes of the receive format.

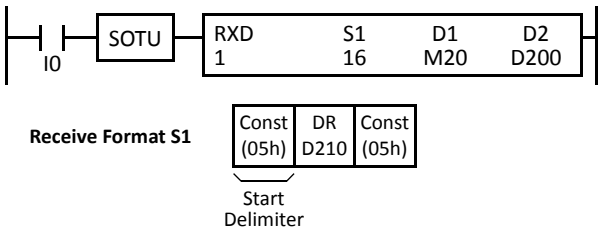
• More than 5 constants are specified from the first byte



Note: Constants that are not either start delimiters nor end delimiters are considered constants for verification. See page 10-23.

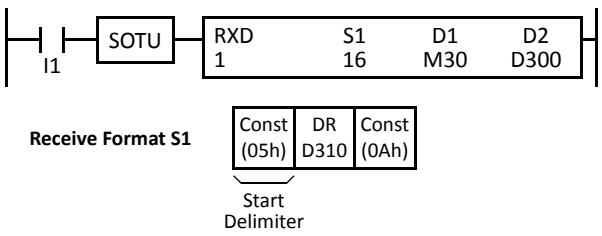
Example: Start Delimiter Duplication Error

When input I0 is turned on, the first RXD instruction is executed and status code 32 is stored in the receive status D200, indicating the RXD instruction is waiting for the incoming data. When input I1 is turned on, another RXD instruction is executed, but since two RXD instructions have the same start delimiter, the second RXD instruction is not executed, and the user communication error code 5 is stored in the receive status D300.



Communication port: Port 1
Receive completion output: M20
Receive status register: D200
Receive data byte count: D201

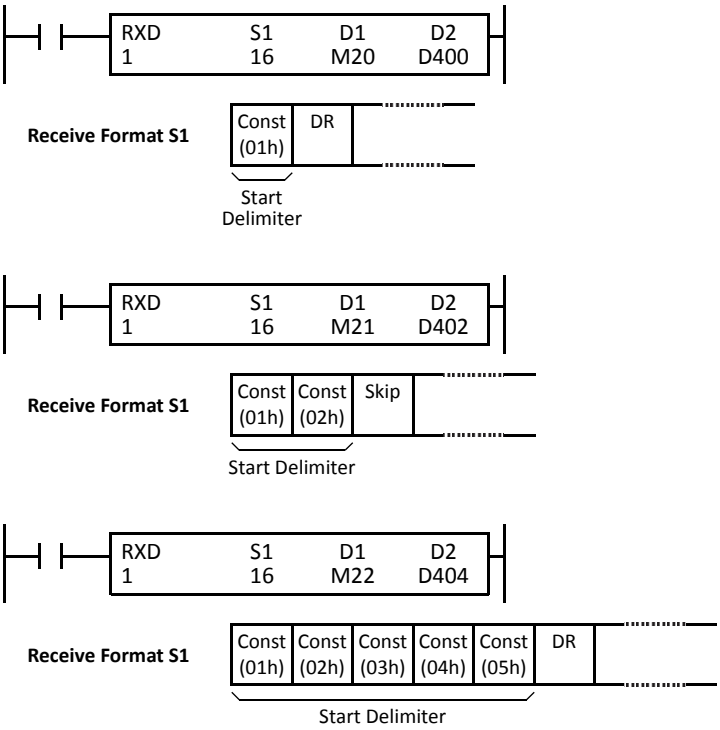
D200	32
M20	OFF



Communication port: Port 1
Receive completion output: M30
Receive status register: D300
Receive data byte count: D301

D300	5
M30	OFF

Note: If the lengths of multi-byte start delimiters of two RXD instructions executed at the same time are different, these are considered the same multi-byte start delimiter if the start delimiter constants as many as the length of the start delimiter of the RXD instruction whose start delimiter length is smaller are the same. The start delimiter of any of two RXD instructions in the following RXD instructions are considered the same.

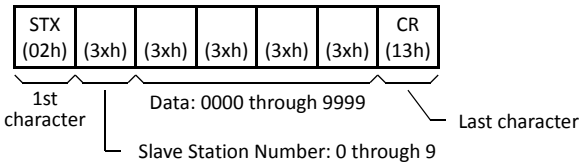


Example: Using Multi-byte Start Delimiter

The following example shows the advantages of using a multi-byte start delimiter rather than a single-byte start delimiter. A RXD instruction processes incoming data from the master station. The incoming data is sent to multiple slave stations 0 through 9, and the local slave station number is 1. Therefore, incoming data from the master station must be received only when the incoming data is sent for the slave station 1.

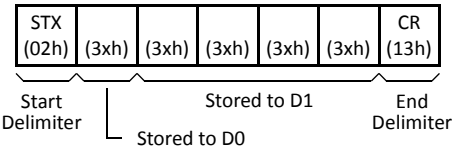
• Incoming data

Incoming data consists of start delimiter STX, a slave station number which can be 0 through 9, data 0000 through 9999, and end delimiter CR.



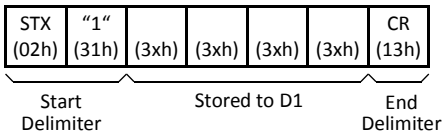
• Single-byte start delimiter

Only the first byte can be the start delimiter. The second byte of the incoming data, which is the slave station number, has to be stored to data register D0, and extra ladder programming is needed to see whether the slave station number of the incoming communication is 1 or not. Only when the slave station number is 1, received data stored in D1 is valid for the local PLC.



• Multi-byte start delimiter (system program version 200 or higher required)

First two bytes can be configured as a multi-byte start delimiter. The incoming data is processed according to the receive format only when the first two bytes of the incoming data match the start delimiter. Therefore, only the incoming data sent to slave station 1 is processed. No extra ladder programming is needed to check the slave station number.



Designating Constant as End Delimiter

An end delimiter can be programmed at the end of the receive format of a RXD instruction; the MicroSmart will recognize the end of valid communication, although RXD instructions without an end delimiter can also be executed.

When a constant value is designated at the end of source device S1, the one-byte data serves as an end delimiter to end the processing of the received data. End delimiters can be 00h through FFh. Constant values are entered in character or hexadecimal notation into the source data. When using the same RXD instruction repeatedly in a user program, designate different end delimiters for each RXD instruction.

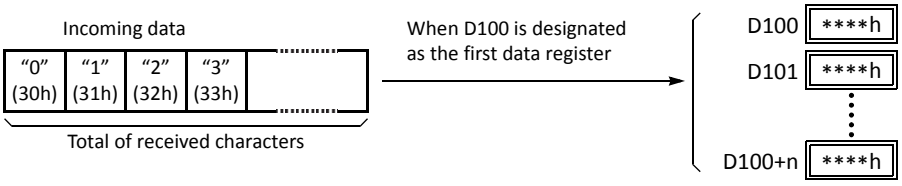
If a character in incoming data matches the end delimiter, the RXD instruction ends receiving data at this point and starts subsequent receive processing as specified. Even if a character matches the end delimiter at a position earlier than expected, the RXD instruction ends receiving data there.

If a BCC code is included in the receive format of a RXD instruction, an end delimiter can be positioned immediately before or after the BCC code. If a data register or skip is designated between the BCC and end delimiter, correct receiving is not ensured.

When a RXD instruction without an end delimiter is executed, data receiving ends when the specified bytes of data in the receive format, such as data registers and skips, have been received. In addition, data receiving also ends when the interval between incoming data characters exceeds the receive timeout value specified in the Communication Parameters dialog box whether the RXD has an end delimiter or not. The character interval timer is started when the first character of incoming communication is received and restarted each time the next character is received. When a character is not received within a predetermined period of time, timeout occurs and the RXD ends data receive operation.

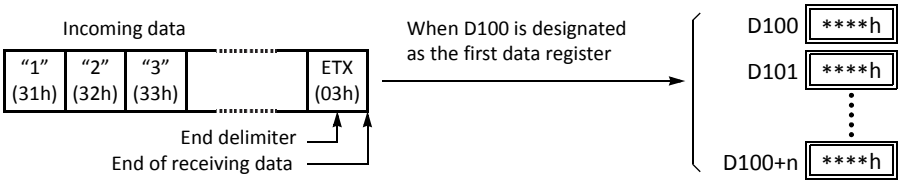
Example:

(1) When a RXD instruction without an end delimiter is executed



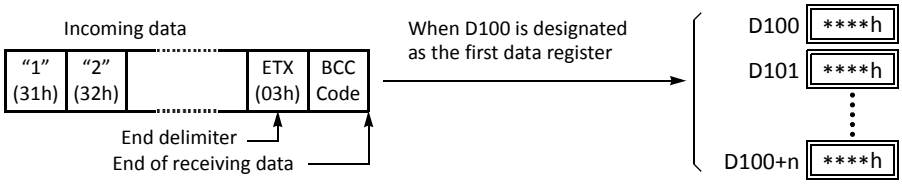
The incoming data is divided, converted, and stored to data registers according to the receive format.
Receive operation is completed when the total characters programmed in RXD are received.

(2) When a RXD instruction with end delimiter ETX (03h) and without BCC is executed



The incoming data is divided, converted, and stored to data registers according to the receive format.
The end delimiter is not stored to a data register.
Any data arriving after the end delimiter is discarded.

(3) When a RXD instruction with end delimiter ETX (03h) and one-byte BCC is executed



The incoming data is divided, converted, and stored to data registers according to the receive format.
The end delimiter and BCC code are not stored to data registers.
After receiving the end delimiter, the MicroSmart receives only the one-byte BCC code.

Constant for Verification (System program 200 or higher)

When using CPU modules with system program version 200 or higher, constants excluding start and end delimiters can be configured in the receive format to verify the incoming data with the constants, which are either characters or hexadecimal values. Constants for the verification can be configured as many as required. The verification result is stored in the receive status of the RXD instruction.

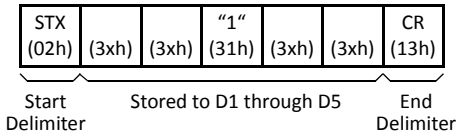
Note: Constants other than start or end delimiters cannot be configured in the receive format for the CPU modules with the system program earlier than 200. If configured, RXD instructions do not complete receiving the incoming data normally.

Example: Programming Constant for Verification

The following example shows the advantage of using constant for verification. The incoming data contains a constant value "1" in the middle, and that constant value needs to be verified to see whether the incoming data is valid.

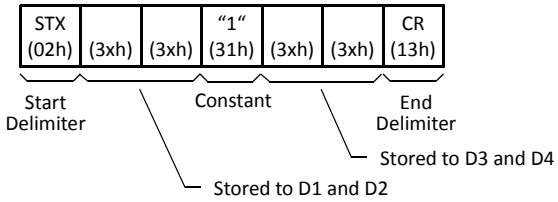
• Using Data Register

The incoming data including the constant value needs to be stored in data registers. When the RXD instruction completes receiving the incoming data, the receive status contains 64, meaning the RXD instruction has completed without errors, even if the constant value is not an expected value. Extra ladder programming is needed to see whether the constant value in the incoming data is correct or not.



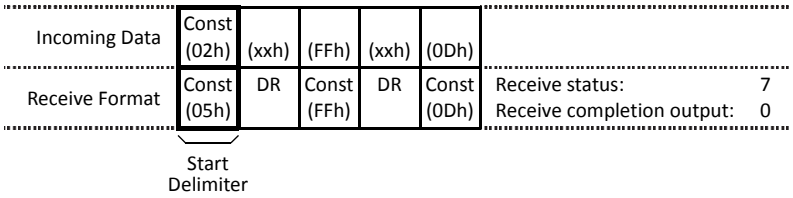
• Using Constant for Verification (system program version 200 or higher)

A constant to verify the constant value in the incoming data is designated in the receive format. If the constant value is not an expected value when the RXD instruction completes receiving the incoming data, the receive status contains 74, meaning the RXD instruction has completed but user communication error code 5 occurred. No extra ladder programming is needed to see whether the constant value in the received data is correct or not.



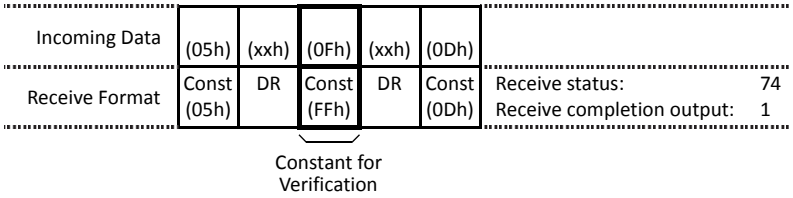
Note: When configuring constants, which are either characters or hexadecimal values, in the receive format, and the incoming data do not match the constants in the receive format, then a user communication error code is stored in the receive status. The error code contained in the receive status depends on whether the constants are used as a start delimiter or as constants for verification. If used as a start delimiter, user communication error code 7 is stored in the receive status, and the RXD instruction keeps waiting for valid incoming data. On the other hand, if used as constants for verification, the receive status contains 74, and the RXD instruction finishes the execution. To repeat receiving incoming communication, turn on the input for the RXD instruction.

- Start delimiter of incoming data does not match the receive format



RXD instruction keeps waiting for valid incoming data, and completes data receiving after receiving valid data including a correct start delimiter.

- Constant for verification of incoming data does not match the receive format

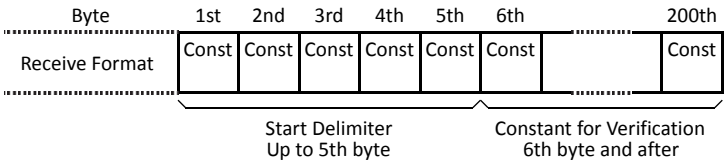


Receive status stores 74 (= 64 + 10)

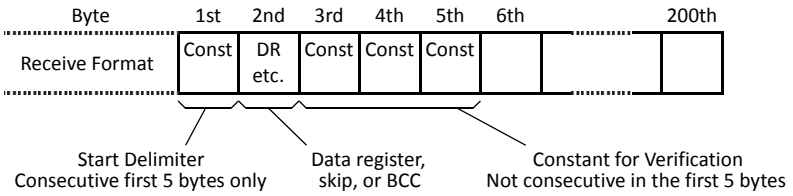
RXD instruction completes data receiving. To repeat receiving incoming communication, turn on the input for the RXD instruction.

Note: Constants configured in the beginning of receive formats are have different functions as shown below:

- More than five constants are configured in the beginning of the receive format



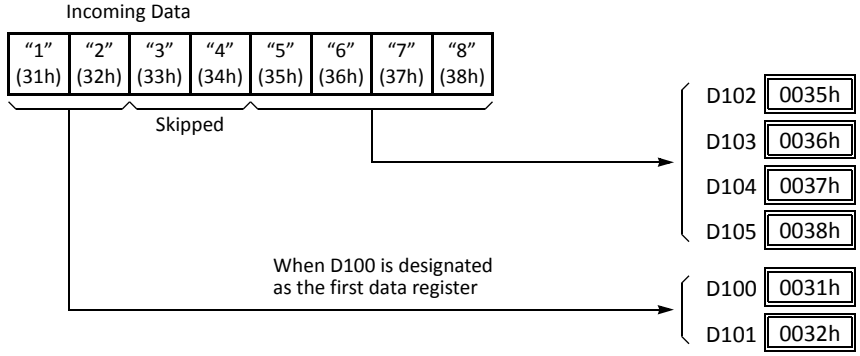
- Other than constants (data register, skip, or BCC) are included in the first five bytes of the receive format



Skip

When "skip" is designated in the receive format, a specified quantity of digits in the incoming data are skipped and not stored to data registers. A maximum of 99 digits (bytes) of characters can be skipped continuously.

Example: When a RXD instruction with skip for 2 digits starting at the third byte is executed



BCC (Block Check Character)

The MicroSmart has an automatic BCC calculation function to detect a communication error in incoming data. If a BCC code is designated in the receive format of a RXD instruction, the MicroSmart calculates a BCC value for a specified starting position through the position immediately preceding the BCC and compares the calculation result with the BCC code in the received incoming data. The start position for the BCC calculation can be specified from the first byte through the 15th byte. The BCC can be 1 or 2 digits.

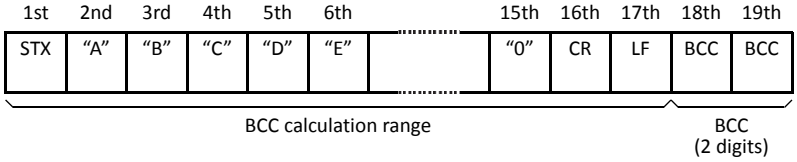
When an end delimiter is not used in the RXD instruction, the BCC code must be positioned at the end of the receive format designated in Source 1 device. When an end delimiter is used, the BCC code must be immediately before or after the end delimiter. The MicroSmart reads a specified number of BCC digits in the incoming data according to the receive format to calculate and compare the received BCC code with the BCC calculation results.

BCC Calculation Start Position

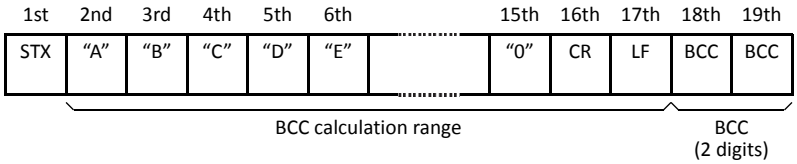
The start position for the BCC calculation can be specified from the first byte through the 15th byte. The BCC is calculated for the range starting at the designated position up to the byte immediately before the BCC of the receive data.

Example: Received data consists of 17 bytes plus 2 BCC digits.

(1) Calculation start position = 1



(2) Calculation start position = 2



BCC Calculation Formula

BCC calculation formula can be selected from XOR (exclusive OR), ADD (addition), ADD-2comp, Modbus ASCII, or Modbus RTU.

Example: Incoming data consists of 41h, 42h, 43h, and 44h.

(1) BCC calculation formula = XOR

Calculation result = 41h ⊕ 42h ⊕ 43h ⊕ 44h = 04h

(2) BCC calculation formula = ADD

Calculation result = 41h + 42h + 43h + 44h = 10Ah → 0Ah (Only the last 1 or 2 digits are used as BCC.)

(3) BCC calculation formula = ADD-2comp

Calculation result = FEh, F6h (2 digits without conversion)

(4) BCC calculation formula = Modbus ASCII

Calculation result = 88 (ASCII)

(5) BCC calculation formula = Modbus RTU

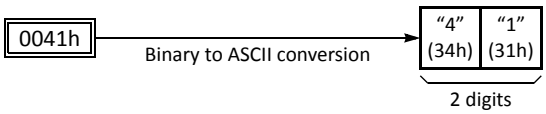
Calculation result = 85h 0Fh (binary)

Conversion Type

The BCC calculation result can be converted or not according to the designated conversion type as described below:

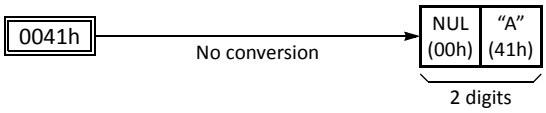
Example: BCC calculation result is 0041h.

(1) Binary to ASCII conversion



Note: On WindLDR, Modbus ASCII is defaulted to binary to ASCII conversion.

(2) No conversion



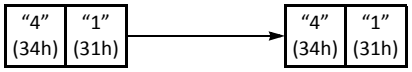
Note: On WindLDR, Modbus RTU is defaulted to no conversion.

BCC Digits (Bytes)

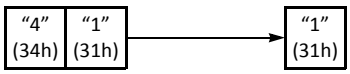
The quantity of digits (bytes) of the BCC code can be selected from 1 or 2.

Example:

(1) BCC digits = 2



(2) BCC digits = 1

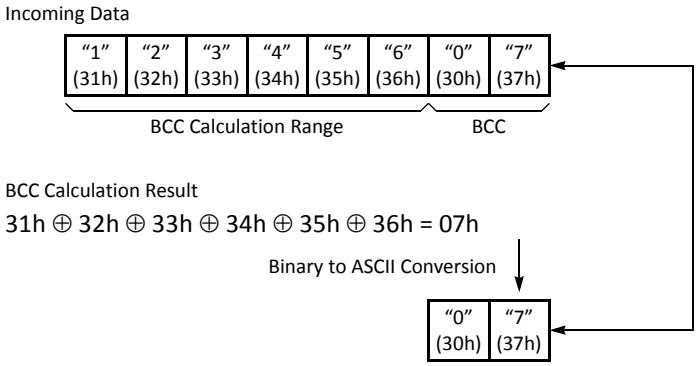


Note: On WindLDR, Modbus ASCII and Modbus RTU are defaulted to 2 digits.

Comparing BCC Codes

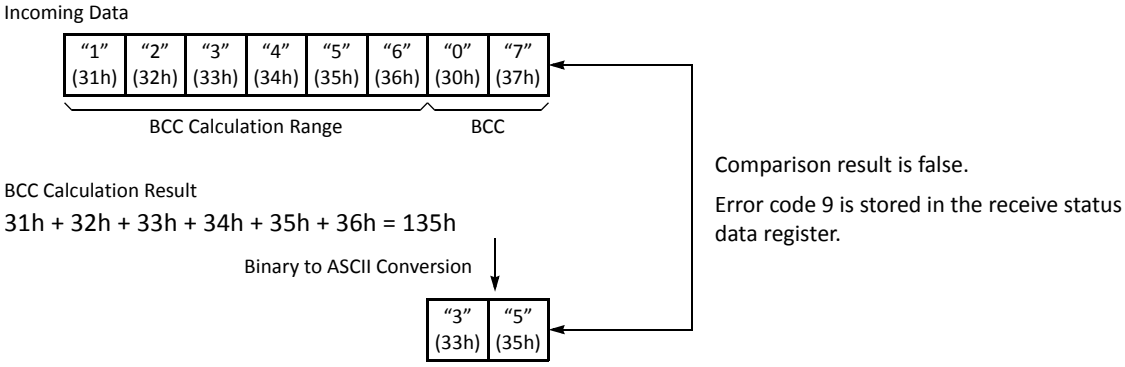
The MicroSmart compares the BCC calculation result with the BCC code in the received incoming data to check for any error in the incoming communication due to external noises or other causes. If a disparity is found in the comparison, an error code is stored in the data register designated as receive status in the RXD instruction. For user communication error code, see page 10-32.

Example 1: BCC is calculated for the first byte through the sixth byte using the XOR format, converted in binary to ASCII, and compared with the BCC code appended to the seventh and eighth bytes of the incoming data.



Comparison result is true to indicate that data is received correctly.

Example 2: BCC is calculated for the first byte through the sixth byte using the ADD format, converted in binary to ASCII, and compared with the BCC code appended to the seventh and eighth bytes of the incoming data.



Receive Completion Output

Designate an output, Q0 through Q627, or internal relay, M0 through M2557, as a device for the receive completion output.

When the start input for a RXD instruction is turned on, preparation for receiving data is initiated, followed by data conversion and storage. When a sequence of all data receive operation is complete, the designated output or internal relay is turned on.

Conditions for Completion of Receiving Data

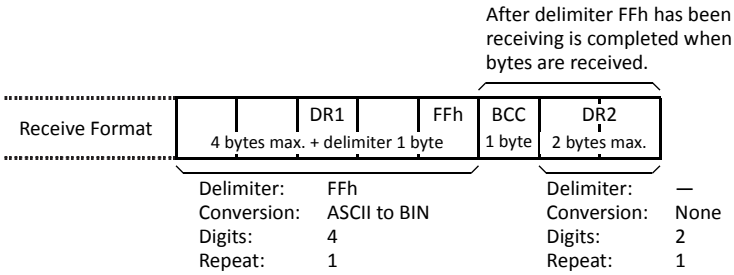
After starting to receive data, the RXD instruction can be completed in three ways depending on the designation of end delimiter and delimiter in the receive format.

End Delimiter	Delimiter	Conditions for Completion of Receiving Data
With	With or Without	When a specified byte count of data (digits × repeat) has been received or when an end delimiter is received. When a BCC exists immediately after the end delimiter, the BCC is received before ending data receiving.
Without	With	After the last constant (including delimiter) designated in the RXD instruction has been received, data receiving is completed when the subsequent byte count of data has been received.
Without	Without	When a specified byte count of data (digits × repeat) has been received.

Note: Whenever a receive timeout has occurred, data receiving is stopped arbitrarily.

Data receiving is completed when one of the above three conditions is met. To abort a RXD instruction, use the special internal relay for user communication receive instruction cancel flag. See page 10-28.

Example: A RXD instruction does not have an end delimiter and has a delimiter programmed in the receive format for data registers.



Receive Status

Designate a data register, D0-D1998, D2000-D7998, or D10000-D49998, as a device to store the receive status information including a receive status code and a user communication error code.

Receive Status Code

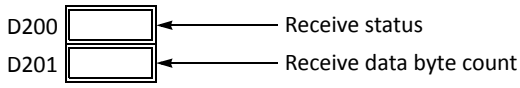
Receive Status Code	Status	Description
16	Preparing data receive	From turning on the start input for a RXD instruction to read the receive format, until the RXD instruction is enabled by an END processing
32	Receiving data	From enabling the RXD instruction by an END processing, until incoming data is received
48	Data receive complete	From receiving incoming data, until the received data is converted and stored in data registers according to the receive format
64	Receive instruction complete	All data receive operation is completed and the next data receive is made possible
128	User communication receive instruction cancel flag active	RXD instructions are cancelled by special internal relay for user communication receive instruction cancel flag, such as M8022 or M8023

If the receive status code is other than shown above, an error of receive instruction is suspected. See User Communication Error Code on page 10-32.

Receive Data Byte Count

The data register next to the device designated for receive status stores the byte count of data received by the RXD instruction. When a start delimiter, end delimiter, and BCC are included in the received data, the byte counts for these codes are also included in the receive data byte count.

Example: Data register D200 is designated as a device for receive status.



User Communication Receive Instruction Cancel Flag

Special internal relays for user communication receive instruction cancel flag are used to cancel all RXD instructions for each port. While the MicroSmart has completed receive format and is ready for receiving incoming data, turning on the user communication receive instruction cancel flag cancels all RXD instructions for each port. This function is useful to cancel receive instructions only, without stopping the MicroSmart.

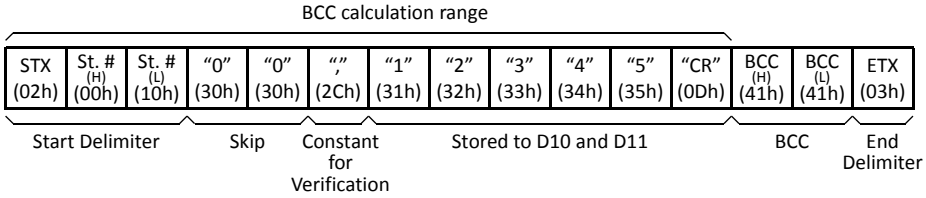
To make the cancelled RXD instructions active, turn off the flag and turn on the input to the RXD instruction again.

Device Address	Description	CPU Stopped	Power OFF	Remarks
M8022	User Communication Receive Instruction Cancel Flag (Port 1)	Cleared	Cleared	
M8023	User Communication Receive Instruction Cancel Flag (Port 2)	Cleared	Cleared	
M8033	User Communication Receive Instruction Cancel Flag (Port 3)	Cleared	Cleared	
M8145	User Communication Receive Instruction Cancel Flag (Port 4)	Cleared	Cleared	
M8146	User Communication Receive Instruction Cancel Flag (Port 5)	Cleared	Cleared	
M8147	User Communication Receive Instruction Cancel Flag (Port 6)	Cleared	Cleared	Reserved in all-in-one CPU
M8170	User Communication Receive Instruction Cancel Flag (Port 7)	Cleared	Cleared	Slim CPU only

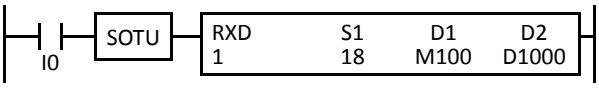
Programming RXD Instruction Using WindLDR

The following example demonstrates how to program a RXD instruction including a start delimiter, skip, constant for verification, BCC, and end delimiter using WindLDR. Converted data is stored to data registers D10 and D11. Internal relay M100 is used as destination D1 for the receive completion output. Data register D1000 is used as destination D2 for the receive status, and data register D1001 is used to store the receive data byte count.

Receive data example:



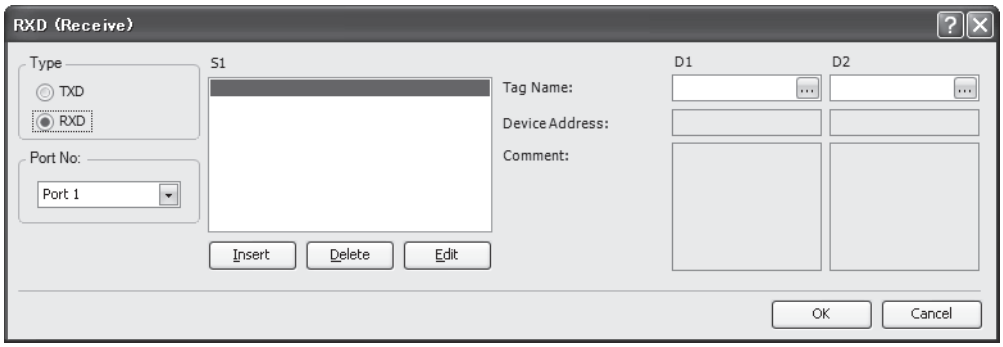
RXD sample program:



Communication port:	Port 1
Receive completion output:	M100
Receive status register:	D1000
Receive data byte count:	D1001

1. Start to program a RXD instruction. Move the cursor where you want to insert the RXD instruction, and type **RXD**. You can also insert the RXD instruction by clicking the User Communication icon in the menu bar and clicking where you want to insert the RXD instruction in the program edit area, then the Transmit dialog box appears. Click **RXD** to change the dialog box to the Receive dialog box.

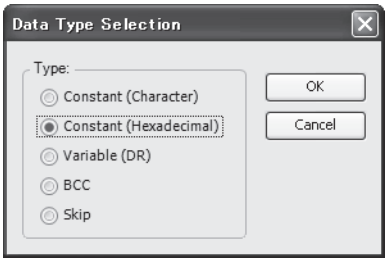
The Receive instruction dialog box appears.

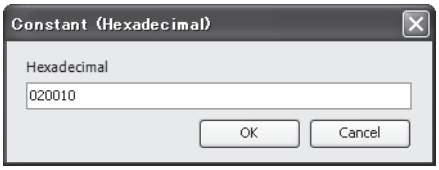


2. Check that **RXD** is selected in the Type box and select **Port 1** in the Port box. Then, click **Insert**.

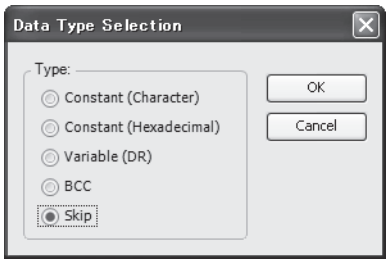
The Data Type Selection dialog box appears. You will program source device S1 using this dialog box.

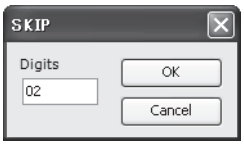
3. Click **Constant (Hexadecimal)** in the Type box and click **OK**. Next, in the Constant (Hexadecimal) dialog box, type **020010** to program the start delimiter STX (02h), Station No. H (00h), and Station No. L (10h). When finished, click **OK**.



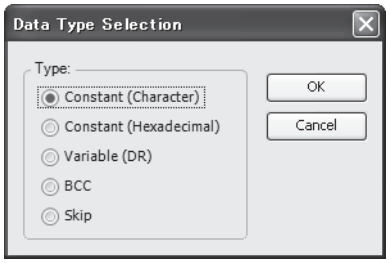


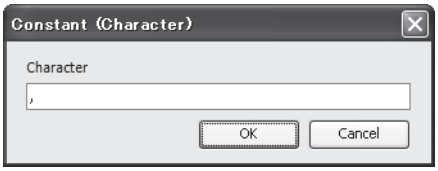
4. Since the Receive instruction dialog box reappears, repeat the above procedure. In the Data Type Selection dialog box, click **Skip** and click **OK**. Next, in the Skip dialog box, type **02** in the Digits box and click **OK**.



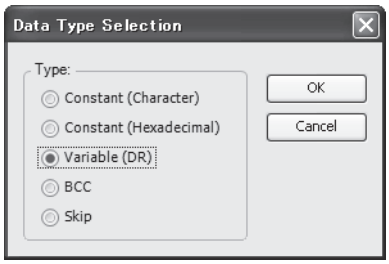


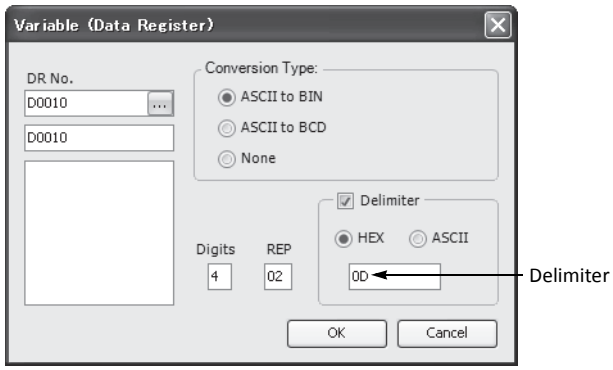
5. Again in the Data Type Selection dialog box, click **Constant (Character)** and click **OK**. Next, in the Constant (Character) dialog box, type **, (2Ch)** in the Character box to program a comma as a constant to verify. When finished, click **OK**.



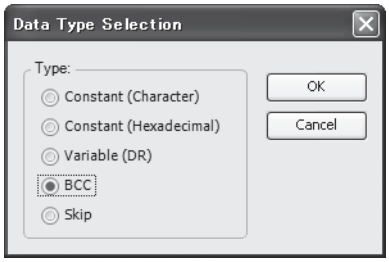


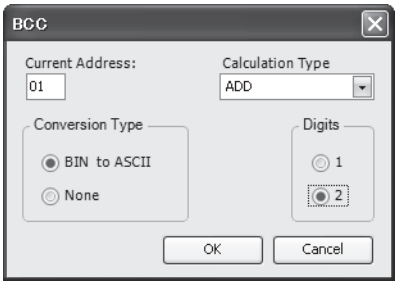
6. Again in the Data Type Selection dialog box, click **Variable (DR)** and click **OK**. Next, in the Variable (Data Register) dialog box, type **D10** in the DR No. box and click **ASCII to BIN** to select ASCII to binary conversion. Enter **4** in the Digits box (4 digits) and **2** in the REP box (2 repeat cycles). Click **Variable**, select **HEX**, and type **0D** to designate a delimiter. When finished, click **OK**.



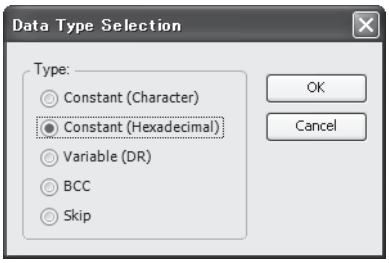


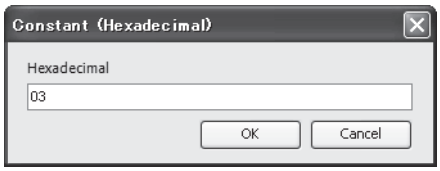
7. Again in the Data Type Selection dialog box, click **BCC** and click **OK**. Next, in the BCC dialog box, enter **1** in the Calculation Start Position box, select **ADD** for the Calculation Type, click **BIN to ASCII** for the Conversion Type, and click **2** for the Digits. When finished, click **OK**.



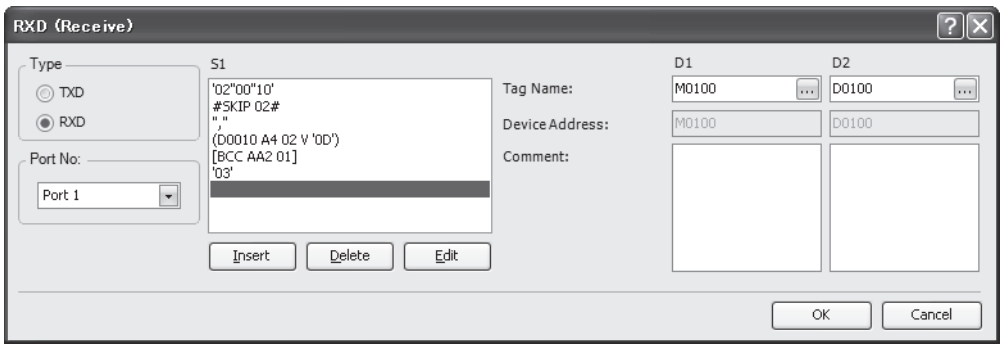


8. Once again in the Data Type Selection dialog box, click **Constant (Hexadecimal)** and click **OK**. Next, in the Constant (Hexadecimal) dialog box, type **03** to program the end delimiter ETX (03h). When finished, click **OK**.





9. In the Receive instruction dialog box, type **M100** in the destination D1 box and type **D1000** in the destination D2 box. When finished, click **OK**.



Programming of the RXD instruction is complete and the receive data will be stored as follows:

D10	1234h	= 4660
D11	0005h	= 5

User Communication Error

When a user communication error occurs, a user communication error code is stored in the data register designated as a transmit status in the TXD instruction or as a receive status in the RXD instruction. When multiple errors occur, the final error code overwrites all preceding errors and is stored in the status data register.

The status data register also contains transmit/receive status code. To extract a user communication error code from the status data register, divide the value by 16. The remainder is the user communication error code. See pages 10-11 and 10-28.

Three error codes 5, 7, and 10 have been updated in CPU modules with system program version 200 or higher.

To correct the error, correct the user program by referring to the error causes described below:

User Communication Error Code

User Communication Error Code	Error Cause	Transmit/Receive Completion Output
1	Start inputs to more than 5 TXD instructions are on simultaneously.	Transmit completion outputs of the first 5 TXD instructions from the top of the ladder diagram are turned on.
2	Transmission destination busy timeout	Goes on after busy timeout.
3	Start inputs to more than 5 RXD instructions with a start delimiter are on simultaneously.	Among the first 5 RXD instructions from the top of the ladder diagram, receive completion outputs of RXD instructions go on if the start delimiter matches the first byte of the received data.
4	While a RXD instruction without a start delimiter is executed, another RXD instruction with or without a start delimiter is executed.	The receive completion output of the RXD instruction at a smaller address goes on.
5	While a RXD instruction with a start delimiter is executed, another RXD instruction with the same start delimiter is executed.	No effect on the receive completion output.
6	— Reserved —	—
7	The first bytes of received data do not match the specified start delimiter.	No effect on the receive completion output. If incoming data with a matching start delimiter is received subsequently, the receive completion output goes on.
8	When ASCII to binary or ASCII to BCD conversion is specified in the receive format, any code other than 0 to 9 and A to F is received. (These codes are regarded as 0 during conversion.)	The receive completion output goes on.
9	BCC calculated from the RXD instruction does not match the BCC appended to the received data.	The receive completion output goes on.
10	Constants including the end delimiter code specified in the RXD instruction do not match the received constants.	The receive completion output goes on.
11	Receive timeout between characters (After receiving one byte of data, the next byte is not received in the period specified for the receive timeout value.)	The receive completion output goes on.
12	Overrun error (Before the receive processing is completed, the next data is received.)	The receive completion output goes off.
13	Framing error (Detection error of start bit or stop bit)	No effect on the completion output.
14	Parity check error (Error is found in the parity check.)	No effect on the completion output.
15	TXD or RXD instruction is executed while user protocol is not selected for the communication port in the Function Area Settings.	No effect on the completion output.

ASCII Character Code Table

Upper Bit / Lower Bit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	$^{N}U_{L}$	$^{D}L_{E}$	SP	0	@	P	`	p								
Decimal	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
1	$^{S}O_{H}$	$^{D}C_{1}$	!	1	A	Q	a	q								
Decimal	1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241
2	$^{S}T_{X}$	$^{D}C_{2}$	”	2	B	R	b	r								
Decimal	2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242
3	$^{E}T_{X}$	$^{D}C_{3}$	#	3	C	S	c	s								
Decimal	3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243
4	$^{E}O_{T}$	$^{D}C_{4}$	$	4	D	T	d	t								
Decimal	4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244
5	$^{E}N_{Q}$	$^{N}A_{K}$	%	5	E	U	e	u								
Decimal	5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245
6	$^{A}C_{K}$	$^{S}Y_{N}$	&	6	F	V	f	v								
Decimal	6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246
7	$^{B}E_{L}$	$^{E}T_{B}$	’	7	G	W	g	w								
Decimal	7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247
8	BS	$^{C}A_{N}$	(	8	H	X	h	x								
Decimal	8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248
9	HT	EM	)	9	I	Y	i	y								
Decimal	9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249
A	LF	$^{S}U_{B}$	*	:	J	Z	j	z								
Decimal	10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250
B	VT	$^{E}S_{C}$	+	;	K	[	k	{								
Decimal	11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251
C	FF	FS	,	<	L	\	l	|								
Decimal	12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252
D	CR	GS	-	=	M	]	m	}								
Decimal	13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253
E	SO	RS	.	>	N	^	n	~								
Decimal	14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254
F	SI	US	/	?	O	_	o									
Decimal	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255

RS232C Line Control Signals

While the MicroSmart is in the user communication mode, special data registers can be used to enable or disable DSR and DTR control signal options for port 2 through port 7. The DSR and DTR control signal options cannot be used for port 1.

The RTS signal line of port 2 through port 7 remains on.

In the maintenance communication mode, DSR has no effect and DTR remain on.

Special Data Registers for Port 2 to Port 7 RS232C Line Control Signals

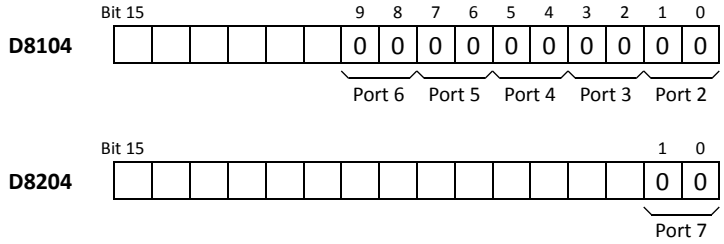
Special data registers D8104 through D8106 and D8204 through D8206 are allocated for RS232C line control signals.

Communication Port	DR No.	Data Register Function	Data Register Value Updated	R/W
Port 2 to Port 6	**D8104**	Control signal status	Every scan	R
	D8105	DSR input control signal option	When sending/receiving data	R/W
	D8106	DTR output control signal option	When sending/receiving data	R/W
Port 7 (Slim type CPU only)	**D8204**	Control signal status	Every scan	R
	D8205	DSR input control signal option	When sending/receiving data	R/W
	D8206	DTR output control signal option	When sending/receiving data	R/W

Control Signal Status D8104 (Port 2 to Port 6) and D8204 (Port 7)

Special data registers D8104 and D8204 store a value to show that DSR and DTR are on or off at port 2 through port 7. The data of D8104 and D8204 are updated at every END processing.

The control status of each port is allocated as shown below:



D8104/D8204 2-bit Binary Value	DTR	DSR	Description
00	OFF	OFF	Both DSR and DTR are off
01	OFF	ON	DSR is on
10	ON	OFF	DTR is on
11	ON	ON	Both DSR and DTR are on

DSR Control Signal Status in RUN and STOP Modes

Communication Mode	D8105/D8205 3-bit Binary Value	DSR (Input) Status	
		RUN Mode	STOP Mode
User Communication Mode	**000 (default)**	No effect	No effect (TXD/RXD disabled)
	001	ON: Enable TXD/RXD OFF: Disable TXD/RXD	No effect (TXD/RXD disabled)
	010	ON: Disable TXD/RXD OFF: Enable TXD/RXD	No effect (TXD/RXD disabled)
	011	ON: Enable TXD OFF: Disable TXD	No effect (TXD/RXD disabled)
	100	ON: Disable TXD OFF: Enable TXD	No effect (TXD/RXD disabled)
	≥ **101**	No effect	No effect (TXD/RXD disabled)
Maintenance Mode	—	No effect	No effect

DTR Control Signal Status in RUN and STOP Modes

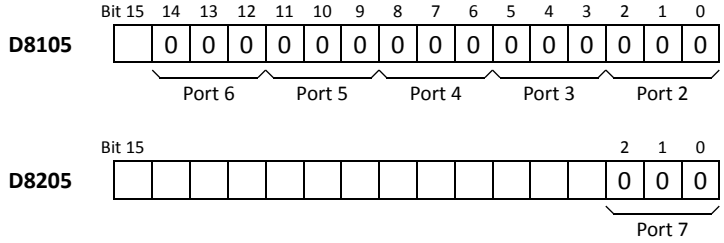
Communication Mode	D8106/D8206 2-bit Binary Value	DTR (Output) Status	
		RUN Mode	STOP Mode
User Communication Mode	**00 (default)**	ON	OFF
	01	OFF	OFF
	10	RXD enabled: ON RXD disabled: OFF	OFF
	11	ON	OFF
Maintenance Mode	—	ON	ON

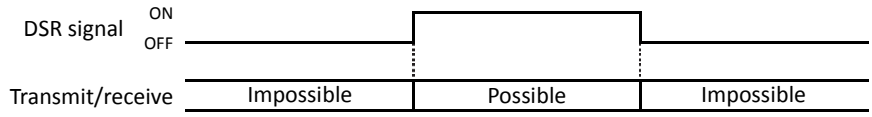
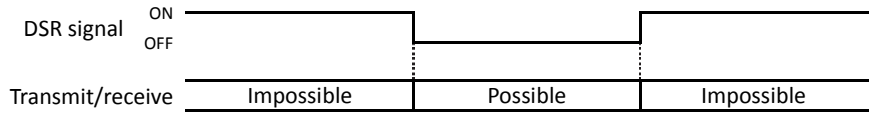
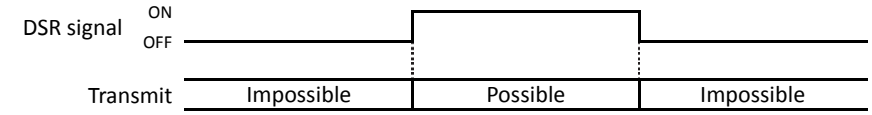
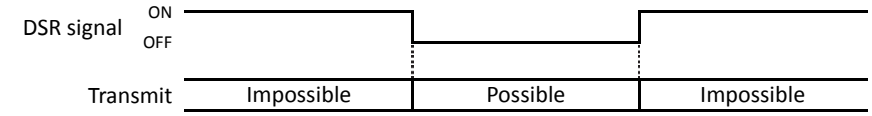
DSR Input Control Signal Option D8105 (Port 2 to Port 6) and D8205 (Port 7)

Special data registers D8105 and D8205 are used to control data flow between the MicroSmart RS232C port 2 through port 7 and the remote terminal depending on the DSR (data set ready) signal sent from the remote terminal. The DSR signal is an input to the MicroSmart to determine the status of the remote terminal. The remote terminal informs the MicroSmart using DSR whether the remote terminal is ready for receiving data or is sending valid data.

The DSR control signal option can be used only for the user communication through the RS232C port 2 to port 7.

The control status of each port is allocated as shown below:



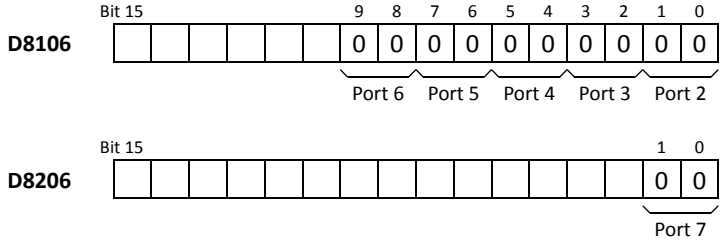
D8105/D8205 3-bit Binary Value	Description
000	DSR is not used for data flow control. When DSR control is not needed, set 0 to D8105/D8205.
001	When DSR is on, the MicroSmart can transmit and receive data. 
010	When DSR is off, the MicroSmart can transmit and receive data. 
011	When DSR is on, the MicroSmart can transmit data. This function is usually called “Busy Control” and is used for controlling transmission to a remote terminal with a slow processing speed, such as a printer. When the remote terminal is busy, data input to the remote terminal is restricted. 
100	When DSR is off, the MicroSmart can transmit data. 
≥ **101**	Same as D8105/D8205 = 000. DSR is not used for data flow control.

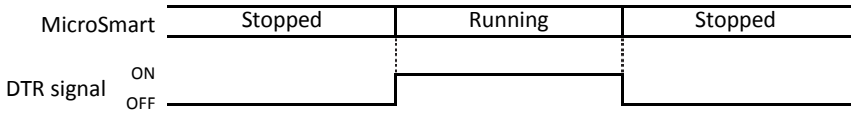
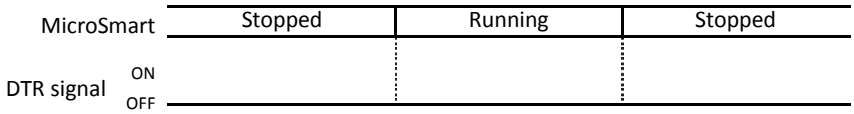
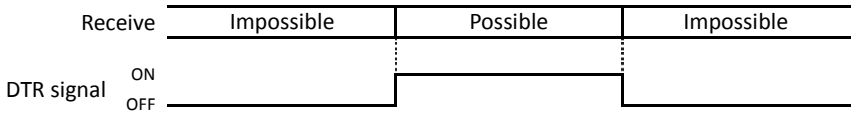
DTR Output Control Signal Option D8106 (Port 2 to Port 6) and D8206 (Port 7)

Special data registers D8106 and D8206 are used to control the DTR (data terminal ready) signal to indicate the MicroSmart operating status or transmitting/receiving status.

The DTR control signal option can be used only for the user communication through the RS232C port 2 to port 7.

The control status of each port is allocated as shown below:

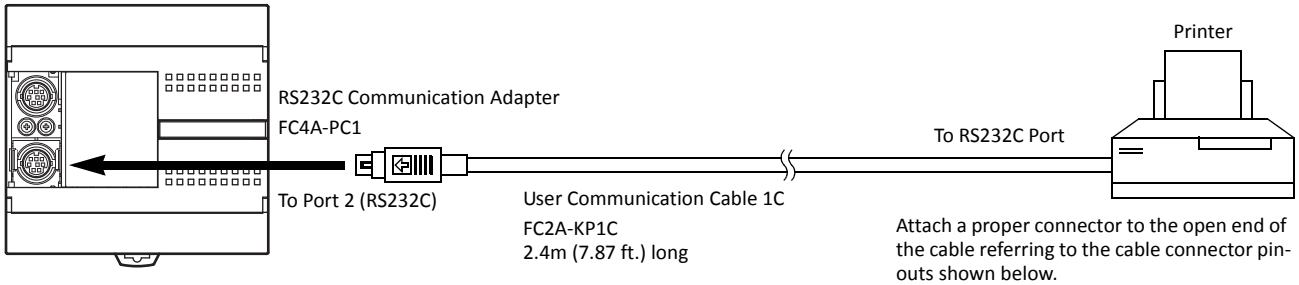


D8106/D8206 2-bit Binary Value	Description
00	While the MicroSmart is running, DTR is on whether the MicroSmart is transmitting or receiving data. While the MicroSmart is stopped, DTR remains off. Use this option to indicate the MicroSmart operating status. 
01	Whether the MicroSmart is running or stopped, DTR remains off. 
10	While the MicroSmart can receive data, DTR is turned on. While the MicroSmart can not receive data, DTR remains off. Use this option when flow control of receive data is required. 
11	Same as D8106/D8206 = 00.

Sample Program – User Communication TXD

This example demonstrates a program to send data to a printer using the user communication TXD2 (transmit) instruction, with the optional RS232C communication adapter installed on the port 2 connector of the 24-I/O type CPU module.

System Setup



Cable Connection and Pinouts

Mini DIN Connector Pinouts

Description		Color	Pin
Shield		—	**Cover**
NC	No Connection	Black	**1**
NC	No Connection	Yellow	**2**
TXD	Transmit Data	Blue	**3**
NC	No Connection	Green	**4**
DSR	Data Set Ready	Brown	**5**
NC	No Connection	Gray	**6**
SG	Signal Ground	Red	**7**
NC	No Connection	White	**8**

D-sub 9-pin Connector Pinouts

Pin	Description	
1	NC	No Connection
2	NC	No Connection
3	DATA	Receive Data
4	NC	No Connection
5	GND	Ground
6	NC	No Connection
7	NC	No Connection
8	BUSY	Busy Signal
9	NC	No Connection

The name of BUSY terminal differs depending on printers, such as DTR. The function of this terminal is to send a signal to remote equipment whether the printer is ready to print data or not. Since the operation of this signal may differ depending on printers, confirm the operation before connecting the cable.

⚠ Caution

- Do not connect any wiring to the NC (no connection) pins; otherwise, the MicroSmart and the printer may not work correctly and may be damaged.

Description of Operation

The data of counter C2 and data register D30 are printed every minute. A printout example is shown on the right.

Printout Example

```
--- PRINT TEST ---

11H 00M

CNT2...0050
D030...3854

--- PRINT TEST ---

11H 01M

CNT2...0110
D030...2124
```

Programming Special Data Register

Special data register D8105 is used to monitor the BUSY signal and to control the transmission of print data.

Special DR	Value	Description
D8105	3 (011)	While DSR is on (not busy), the CPU sends data. While DSR is off (busy), the CPU stops data transmission. If the off duration exceeds a limit (approx. 5 sec), a transmission busy timeout error will occur, and the remaining data is not sent. The transmit status data register stores an error code. See pages 10-11 and 10-32.

The MicroSmart monitors the DSR signal to prevent the receive buffer of the printer from overflowing. For the DSR signal, see page 10-36.

Setting User Communication Mode in WindLDR Function Area Settings

Since this example uses the RS232C port 2, select User Protocol for Port 2 in the Function Area Settings using WindLDR. See page 10-5.

Setting Communication Parameters

Set the communication parameters to match those of the printer. See page 10-5. For details of the communication parameters of the printer, see the user's manual for the printer. An example is shown below:

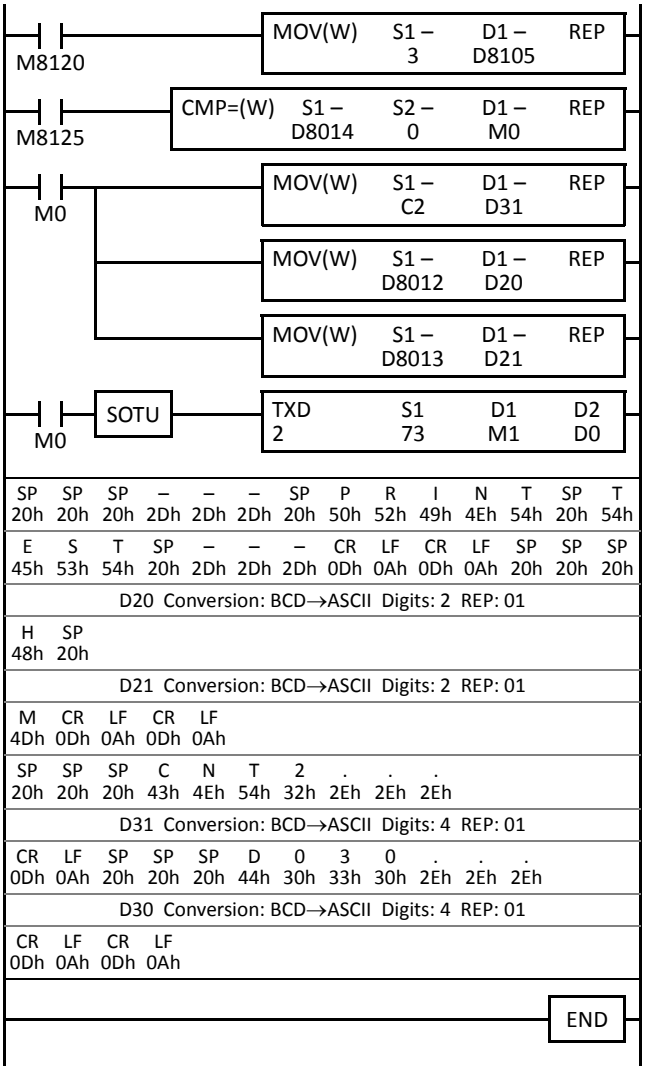
Communication Parameters:

Baud rate	9600 bps
Data bits	8
Parity check	None
Stop bits	1

Note: The receive timeout value is used for the RXD instruction in the user communication mode. Since this example uses only the TXD instruction, the receive timeout value has no effect.

Ladder Diagram

The second data stored in special data register D8014 is compared with 0 using the CMP= (compare equal to) instruction. Each time the condition is met, the TXD2 instruction is executed to send the C2 and D30 data to the printer. A counting circuit for counter C2 is omitted from this sample program.



M8120 is the initialize pulse special internal relay.

3 → D8105 to enable the DSR option for busy control.

M8125 is the in-operation output special internal relay.

CMP=(W) compares the D8014 second data with 0.

When the D8014 data equals 0 second, M0 is turned on.

Counter C2 current value is moved to D31.

D8012 hour data is moved to D20.

D8013 minute data is moved to D21.

TXD2 is executed to send 73-byte data through the RS232C port 2 to the printer.

D20 hour data is converted from BCD to ASCII, and 2 digits are sent.

D21 minute data is converted from BCD to ASCII, and 2 digits are sent.

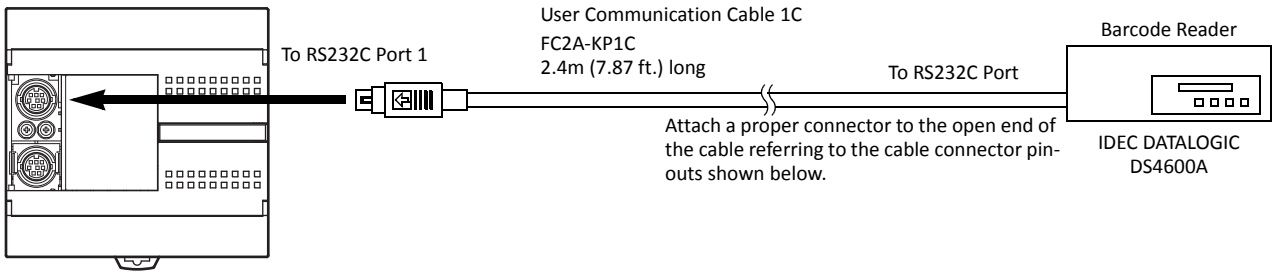
D31 counter C2 data is converted from BCD to ASCII, and 4 digits are sent.

D30 data is converted from BCD to ASCII, and 4 digits are sent.

Sample Program – User Communication RXD

This example demonstrates a program to receive data from a barcode reader with a RS232C port using the user communication RXD1 (receive) instruction.

System Setup



Mini DIN Connector Pinouts

Description		Color	Pin
Shield		—	**Cover**
NC	No Connection	Black	**1**
NC	No Connection	Yellow	**2**
TXD	Transmit Data	Blue	**3**
RXD	Receive Data	Green	**4**
NC	No Connection	Brown	**5**
NC	No Connection	Gray	**6**
SG	Signal Ground	Red	**7**
NC	No Connection	White	**8**

D-sub 25-pin Connector Pinouts

Pin	Description	
1	FG	Frame Ground
2	TXD1	Transmit Data
3	RXD1	Receive Data
7	GND	Ground

Caution

- Do not connect any wiring to the NC (no connection) pins; otherwise, the MicroSmart and the barcode reader may not work correctly and may be damaged.

Description of Operation

A barcode reader is used to scan barcodes of 8 numerical digits. The scanned data is sent to the MicroSmart through the RS232C port 1 and stored to data registers. The upper 8 digits of the data are stored to data register D20 and the lower 8 digits are stored to data register D21.

Setting User Communication Mode in WindLDR Function Area Settings

Since this example uses the RS232C port 1, select User Protocol for Port 1 in the Function Area Settings using WindLDR. See page 10-5.

Setting Communication Parameters

Set the communication parameters to match those of the barcode reader. See page 10-5. For details of the communication parameters of the barcode reader, see the user's manual for the barcode reader. An example is shown below:

Communication Parameters:

Baud rate	9600 bps
Data bits	7
Parity check	Even
Stop bits	1

Configuring Barcode Reader

The values shown below are an example of configuring a barcode reader. For actual settings, see the user's manual for the barcode reader.

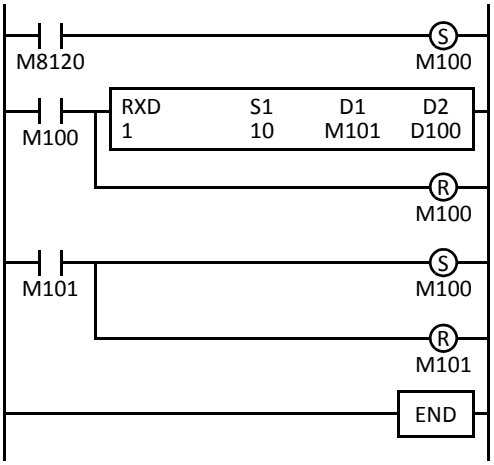
Synchronization mode	Auto			
Read mode	Single read or multiple read			
Communication parameter	Baud rate: Parity check:	9600 bps Even	Data bits: Stop bit:	7 1
Other communication settings	Header: Data echo back: Output timing: Data output filter: Sub serial:	02h No Output priority 1 No No	Terminator: BCR data output: Character suppress: Main serial input:	03h Yes No No
Comparison preset mode	Not used			

Device Addresses

M100	Input to start receiving barcode data
M101	Receive completion output for barcode data
M8120	Initialize pulse special internal relay
D20	Store barcode data (upper 4 digits)
D21	Store barcode data (lower 4 digits)
D100	Receive status data register for barcode data
D101	Receive data byte count data register

Ladder Diagram

When the MicroSmart starts operation, the RXD1 instruction is executed to wait for incoming data. When data receive is complete, the data is stored to data registers D20 and D21. The receive completion signal is used to execute the RXD1 instruction to wait for another incoming data.



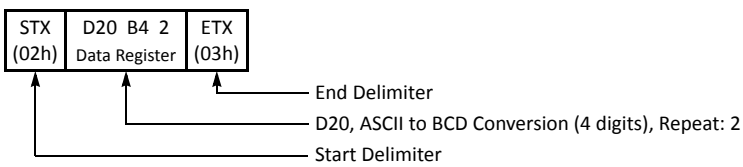
M8120 is the initialize pulse special internal relay used to set M100.

At the rising edge of M100, RXD1 is executed to be ready for receiving data.

Even after M100 is reset, RXD1 still waits for incoming data.

When data receive is complete, M101 is turned on, then M100 is set to execute RXD1 to receive the next incoming data.

RXD1 Data



BCC Calculation Examples

The FC5A MicroSmart CPU modules can use three new BCC calculation formulas of ADD-2comp, Modbus ASCII, and Modbus RTU for transmit instructions TXD1 and TXD2 and receive instructions RXD1 and RXD2. These block check characters are calculated as described below.

ADD-2comp

Add the characters in the range from the BCC calculation start position to the byte immediately before the BCC, then invert the result bit by bit, and add 1.

1. Add the characters in the range from the BCC calculation start position to the byte immediately before the BCC.

2. Invert the result bit by bit, and add 1 (2's complement).

3. Store the result to the BCC position according to the designated conversion type (Binary to ASCII conversion or No conversion) and the designated quantity of BCC digits.

Example: Binary to ASCII conversion, 2 BCC digits

When the result of step **2** is 175h, the BCC will consist of 37h, 35h.

Modbus ASCII — Calculating the LRC (longitudinal redundancy check)

Calculate the BCC using LRC (longitudinal redundancy check) for the range from the BCC calculation start position to the byte immediately before the BCC.

1. Convert the ASCII characters in the range from the BCC calculation start position to the byte immediately before the BCC, in units of two characters, to make 1-byte hexadecimal data. (Example: 37h, 35h → 75h)

2. Add up the results of step **1**.

3. Invert the result bit by bit, and add 1 (2's complement).

4. Convert the lowest 1-byte data to ASCII characters. (Example: 75h → 37h, 35h)

5. Store the two digits to the BCC (LRC) position.

If the BCC calculation range consists of an odd number of bytes, the BCC calculation results in an indefinite value. Modbus protocol defines that the BCC calculation range is an even number of bytes.

Modbus RTU — Calculating the CRC-16 (cyclic redundancy checksum)

Calculate the BCC using CRC-16 (cyclic redundancy checksum) for the range from the BCC calculation start position to the byte immediately before the BCC. The generation polynomial is: $X^{16} + X^{15} + X^2 + 1$.

1. Take the exclusive OR (XOR) of FFFFh and the first 1-byte data at the BCC calculation start position.

2. Shift the result by 1 bit to the right. When a carry occurs, take the exclusive OR (XOR) of A001h, then go to step **3**.
If not, directly go to step **3**.

3. Repeat step **2**, shifting 8 times.

4. Take the exclusive OR (XOR) of the result and the next 1-byte data.

5. Repeat step **2** through step **4** up to the byte immediately before the BCC.

6. Swap the higher and lower bytes of the result of step **5**, and store the resultant CRC-16 to the BCC (CRC) position. (Example: 1234h → 34h, 12h)

11: DATA LINK COMMUNICATION

Introduction

This chapter describes the data link communication function used to set up a distributed control system.

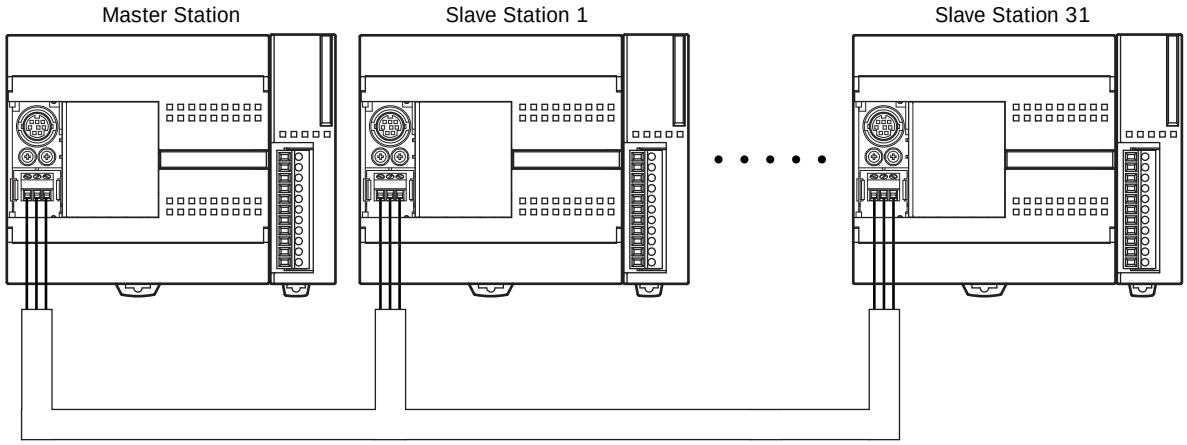
A data link communication system consists of one master station and a maximum of 31 slave stations, each station comprising any all-in-one type or slim type CPU module. When the data link communication is enabled, the master station has 12 data registers assigned for each slave station, and each slave station has 12 data registers for communication with the master station. Using these data registers, the master station can send and receive data of 6 data registers to and from each slave station. No particular program is required for sending or receiving data in the data link communication system.

Data link communication proceeds independently of the user program execution, and the data registers for the data link communication are updated at the END processing.

When data of inputs, outputs, internal relays, timers, counters, or shift registers are moved to data registers using the move instructions in the user program, these data can also be exchanged between the master and slave stations.

The FC4A MicroSmart (except all-in-one 10-I/O type CPU module), OpenNet Controller, MICRO3, MICRO3C, and FA-3S series PLCs can also be connected to the data link communication system.

One CPU module can be either a master station or a slave station. Data link master and slave cannot be used at the same time.



Data Link Specifications

Electric Specifications	Compliance with EIA-RS485
Baud Rate	19,200, 38,400, 57,600 bps
Synchronization	Start-stop synchronization Start bit: 1 Data bits: 7 Parity: Even Stop bit: 1
Communication Cable	Shielded twisted pair cable, core wire 0.3 mm^2
Maximum Cable Length	200m (656 feet) / 1200m (3937 feet) total (Note)
Maximum Slave Stations	31 slave stations
Transmit/Receive Data	Transmit data: 186 words maximum, Receive data: 186 words maximum 0 through 6 words each for transmission and receiving per slave station
Special Internal Relay	M8005-M8007: communication control and error M8080-M8116: communication completion for each slave station M8117: communication completion for all slave stations

Data Register	D900-D1271:	transmit/receive data
Special Data Register	D8069-D8099: D8100:	communication error code data link slave station number

Note: When FC5A-SIF4 expansion RS485 module is used at the master station and all slave stations to set up a data link communication system, the maximum cable length is 1200m. Otherwise, the maximum cable length is 200m.

Data Link System Setup

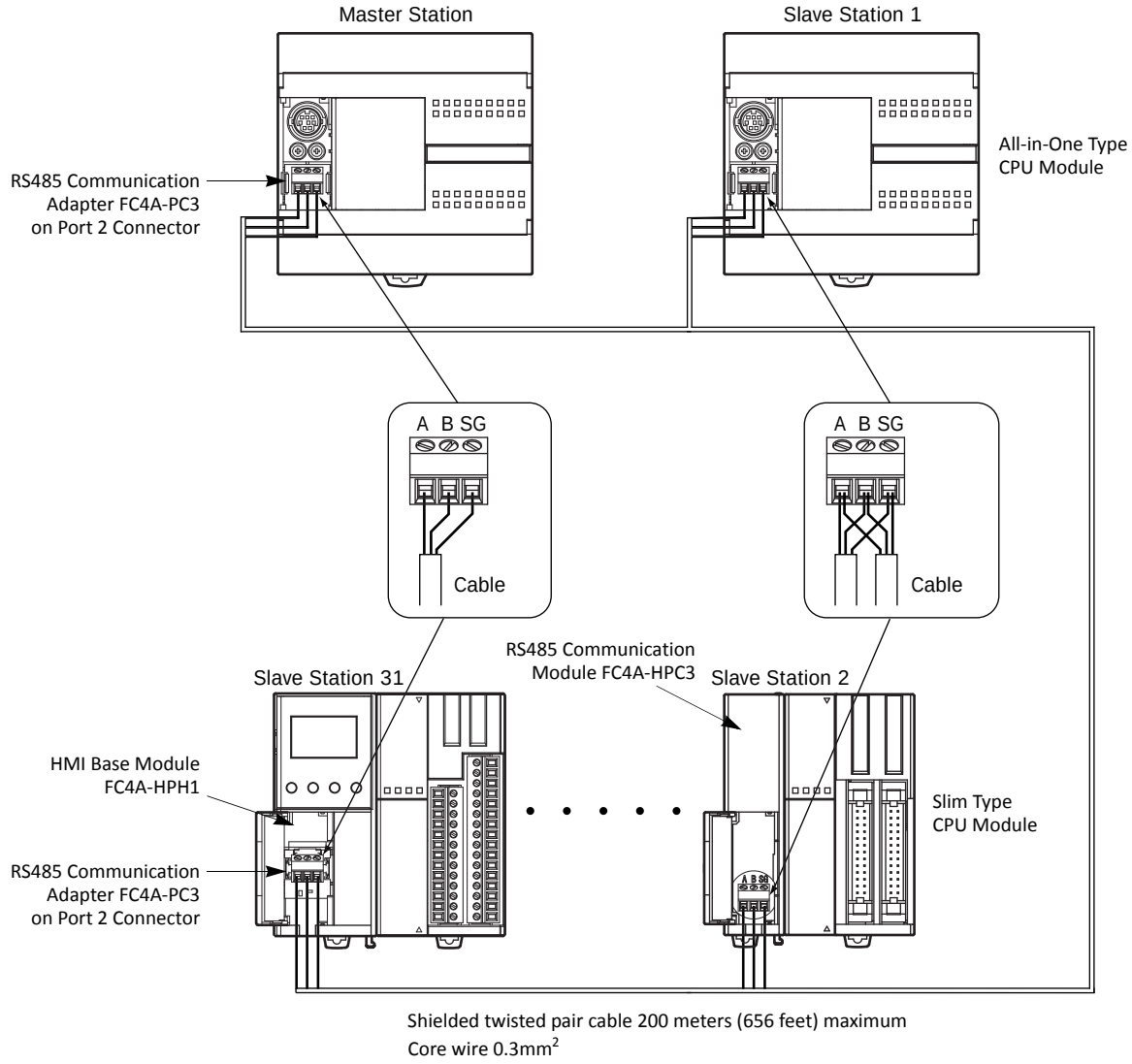
To set up a data link system, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector on the all-in-one type CPU module.

When using the slim type CPU module, mount the RS485 communication module (FC4A-HPC3) next to the CPU module.

When using the optional HMI module (FC4A-PH1) with the slim type CPU module, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector on the HMI base module (FC4A-HPH1).

FC5A-SIF4 Expansion RS485 communication module can also be mounted to the CPU module to add port 3 through 7.

Connect the RS485 terminals A, B, and SG on every CPU module using a shielded twisted pair cable as shown below. The total length of the cable for the data link system can be extended up to 200 meters (656 feet).



Data Register Allocation for Transmit/Receive Data

The master station has 12 data registers assigned for data communication with each slave station. Each slave station has 12 data registers assigned for data communication with the master station. When data is set in data registers at the master station assigned for data link communication, the data is sent to the corresponding data registers at a slave station. When data is set in data registers at a slave station assigned for data link communication, the data is sent to the corresponding data registers at the master station.

Master Station

Slave Station Number	Data Register	Transmit/Receive Data	Slave Station Number	Data Register	Transmit/Receive Data
Slave 1	D900-D905	Transmit data to slave 1	Slave 17	D1092-D1097	Transmit data to slave 17
	D906-D911	Receive data from slave 1		D1098-D1103	Receive data from slave 17
Slave 2	D912-D917	Transmit data to slave 2	Slave 18	D1104-D1109	Transmit data to slave 18
	D918-D923	Receive data from slave 2		D1110-D1115	Receive data from slave 18
Slave 3	D924-D929	Transmit data to slave 3	Slave 19	D1116-D1121	Transmit data to slave 19
	D930-D935	Receive data from slave 3		D1122-D1127	Receive data from slave 19
Slave 4	D936-D941	Transmit data to slave 4	Slave 20	D1128-D1133	Transmit data to slave 20
	D942-D947	Receive data from slave 4		D1134-D1139	Receive data from slave 20
Slave 5	D948-D953	Transmit data to slave 5	Slave 21	D1140-D1145	Transmit data to slave 21
	D954-D959	Receive data from slave 5		D1146-D1151	Receive data from slave 21
Slave 6	D960-D965	Transmit data to slave 6	Slave 22	D1152-D1157	Transmit data to slave 22
	D966-D971	Receive data from slave 6		D1158-D1163	Receive data from slave 22
Slave 7	D972-D977	Transmit data to slave 7	Slave 23	D1164-D1169	Transmit data to slave 23
	D978-D983	Receive data from slave 7		D1170-D1175	Receive data from slave 23
Slave 8	D984-D989	Transmit data to slave 8	Slave 24	D1176-D1181	Transmit data to slave 24
	D990-D995	Receive data from slave 8		D1182-D1187	Receive data from slave 24
Slave 9	D996-D1001	Transmit data to slave 9	Slave 25	D1188-D1193	Transmit data to slave 25
	D1002-D1007	Receive data from slave 9		D1194-D1199	Receive data from slave 25
Slave 10	D1008-D1013	Transmit data to slave 10	Slave 26	D1200-D1205	Transmit data to slave 26
	D1014-D1019	Receive data from slave 10		D1206-D1211	Receive data from slave 26
Slave 11	D1020-D1025	Transmit data to slave 11	Slave 27	D1212-D1217	Transmit data to slave 27
	D1026-D1031	Receive data from slave 11		D1218-D1223	Receive data from slave 27
Slave 12	D1032-D1037	Transmit data to slave 12	Slave 28	D1224-D1229	Transmit data to slave 28
	D1038-D1043	Receive data from slave 12		D1230-D1235	Receive data from slave 28
Slave 13	D1044-D1049	Transmit data to slave 13	Slave 29	D1236-D1241	Transmit data to slave 29
	D1050-D1055	Receive data from slave 13		D1242-D1247	Receive data from slave 29
Slave 14	D1056-D1061	Transmit data to slave 14	Slave 30	D1248-D1253	Transmit data to slave 30
	D1062-D1067	Receive data from slave 14		D1254-D1259	Receive data from slave 30
Slave 15	D1068-D1073	Transmit data to slave 15	Slave 31	D1260-D1265	Transmit data to slave 31
	D1074-D1079	Receive data from slave 15		D1266-D1271	Receive data from slave 31
Slave 16	D1080-D1085	Transmit data to slave 16	—		
	D1086-D1091	Receive data from slave 16			

If any slave stations are not connected, master station data registers which are assigned to the vacant slave stations can be used as ordinary data registers.

Slave Station

Data	Data Register	Transmit/Receive Data
Slave Station Data	D900-D905	Transmit data to master station
	D906-D911	Receive data from master station

Slave station data registers D912 through D1271 can be used as ordinary data registers.

Special Data Registers for Data Link Communication Error

In addition to data registers assigned for data communication, the master station has 31 special data registers and each slave station has one special data register to store data link communication error codes. If any communication error occurs in the data link system, communication error codes are set to a corresponding data register for link communication error at the master station and to data register D8069 at the slave station. For details of link communication error codes, see below.

When data link master/slave is used on port 3 through port 7, data link communication error codes are not stored in D8069 through D8099. Those error codes are stored in consecutive data registers starting from the data register specified in Function Area Settings.

If a communication error occurs in the data link communication system, the data is resent two times. If the error still exists after three attempts, then the error code is set to the data registers for data link communication error. Since the error code is not communicated between the master and slave stations, error codes must be cleared individually.

Master Station

Special Data Register	Data Link Communication Error Data	Special Data Register	Data Link Communication Error Data
D8069	Slave station 1 communication error	D8085	Slave station 17 communication error
D8070	Slave station 2 communication error	D8086	Slave station 18 communication error
D8071	Slave station 3 communication error	D8087	Slave station 19 communication error
D8072	Slave station 4 communication error	D8088	Slave station 20 communication error
D8073	Slave station 5 communication error	D8089	Slave station 21 communication error
D8074	Slave station 6 communication error	D8090	Slave station 22 communication error
D8075	Slave station 7 communication error	D8091	Slave station 23 communication error
D8076	Slave station 8 communication error	D8092	Slave station 24 communication error
D8077	Slave station 9 communication error	D8093	Slave station 25 communication error
D8078	Slave station 10 communication error	D8094	Slave station 26 communication error
D8079	Slave station 11 communication error	D8095	Slave station 27 communication error
D8080	Slave station 12 communication error	D8096	Slave station 28 communication error
D8081	Slave station 13 communication error	D8097	Slave station 29 communication error
D8082	Slave station 14 communication error	D8098	Slave station 30 communication error
D8083	Slave station 15 communication error	D8099	Slave station 31 communication error
D8084	Slave station 16 communication error	—	—

If any slave stations are not connected, master station data registers which are assigned to the vacant slave stations can be used as ordinary data registers.

Slave Station

Special Data Register	Data Link Communication Error Data
D8069	Slave station communication error

Notes: Slave station data registers D8070 through D8099 can be used as ordinary data registers.

Data Link Communication Error Code

The data link error code is stored in the special data register allocated to indicate a communication error in the data link system. When port 2 is used and this error occurs, special internal relay M8005 (communication error) is also turned on at both master and slave stations. The detailed information of general errors can be viewed using WindLDR. Select **Online** > **Monitor** > **Monitor**, then **Online** > **Status** > **Error Status: Details**. See page 13-2.

Error Code	Error Details
1h (1)	Overrun error (data is received when the receive data registers are full)
2h (2)	Framing error (failure to detect start or stop bit)
4h (4)	Parity error (an error was found by the parity check)
8h (8)	Receive timeout (line disconnection)
10h (16)	BCC (block check character) error (disparity with data received up to BCC)
20h (32)	Retry cycle over (error occurred in all 3 trials of communication)
40h (64)	I/O definition quantity error (discrepancy of transmit/receive station number or data quantity)

When more than one error is detected in the data link system, the total of error codes is indicated. For example, when framing error (error code 2h) and BCC error (error code 10h) are found, error code 12h (18) is stored.

Data Link Communication between Master and Slave Stations

The master station has 6 data registers assigned to transmit data to a slave station and 6 data registers assigned to receive data from a slave station. The quantity of data registers for data link can be selected from 0 through 6 using WindLDR. The following examples illustrate how data is exchanged between the master and slave stations when 2 or 6 data registers are used for data link communication with each of 31 slave stations.

Example 1: Transmit Data 2 Words and Receive Data 2 Words

Master Station

D8069	Communication Error
D900 - D901	Transmit Data
D906 - D907	Receive Data
D8070	Communication Error
D912 - D913	Transmit Data
D918 - D919	Receive Data
D8071	Communication Error
D924 - D925	Transmit Data
D930 - D931	Receive Data
D8072	Communication Error
D936 - D937	Transmit Data
D942 - D943	Receive Data
⋮	⋮
D8098	Communication Error
D1248 - D1249	Transmit Data
D1254 - D1255	Receive Data
D8099	Communication Error
D1260 - D1261	Transmit Data
D1266 - D1267	Receive Data

Slave Stations

D8069	Communication Error	Slave Station 1
D900 - D901	Transmit Data	
D906 - D907	Receive Data	
D8069	Communication Error	Slave Station 2
D900 - D901	Transmit Data	
D906 - D907	Receive Data	
D8069	Communication Error	Slave Station 3
D900 - D901	Transmit Data	
D906 - D907	Receive Data	
D8069	Communication Error	Slave Station 4
D900 - D901	Transmit Data	
D906 - D907	Receive Data	
⋮	⋮	⋮
D8069	Communication Error	Slave Station 30
D900 - D901	Transmit Data	
D906 - D907	Receive Data	
D8069	Communication Error	Slave Station 31
D900 - D901	Transmit Data	
D906 - D907	Receive Data	

Example 2: Transmit Data 6 Words and Receive Data 6 Words

Master Station

D8069	Communication Error
D900 - D905	Transmit Data
D906 - D911	Receive Data
D8070	Communication Error
D912 - D917	Transmit Data
D918 - D923	Receive Data
D8071	Communication Error
D924 - D929	Transmit Data
D930 - D935	Receive Data
D8072	Communication Error
D936 - D941	Transmit Data
D942 - D947	Receive Data
⋮	⋮
D8098	Communication Error
D1248 - D1253	Transmit Data
D1254 - D1259	Receive Data
D8099	Communication Error
D1260 - D1265	Transmit Data
D1266 - D1271	Receive Data

Slave Stations

D8069	Communication Error	Slave Station 1
D900 - D905	Transmit Data	
D906 - D911	Receive Data	
D8069	Communication Error	Slave Station 2
D900 - D905	Transmit Data	
D906 - D911	Receive Data	
D8069	Communication Error	Slave Station 3
D900 - D905	Transmit Data	
D906 - D911	Receive Data	
D8069	Communication Error	Slave Station 4
D900 - D905	Transmit Data	
D906 - D911	Receive Data	
⋮	⋮	⋮
D8069	Communication Error	Slave Station 30
D900 - D905	Transmit Data	
D906 - D911	Receive Data	
D8069	Communication Error	Slave Station 31
D900 - D905	Transmit Data	
D906 - D911	Receive Data	

Note: When data link is used on port 3 through port 7, data link communication error codes are stored in the consecutive data registers starting from the data register designated in Function Area Settings.

Special Internal Relays for Data Link Communication

Special internal relays M8005 through M8007 and M8080 through M8117 are assigned for the data link communication.

M8005 Data Link Communication Error

When an error occurs during communication in the data link system, M8005 turns on. The M8005 status is maintained when the error is cleared and remains on until M8005 is reset using WindLDR or until the CPU is turned off. The cause of the data link communication error can be checked using **Online** > **Monitor** > **Monitor**, followed by **Online** > **Status** > **Error Status: Details**. See page 11-5.
Data link communication error is stored in M8005 only when data link is used on port 2.

M8006 Data Link Communication Prohibit Flag (Master Station)

When M8006 at the master station is turned on in the data link system, data link communication is stopped. When M8006 is turned off, data link communication resumes. The M8006 status is maintained when the CPU is turned off and remains on until M8006 is reset using WindLDR.
When M8006 is on at the master station, M8007 is turned on at slave stations in the data link system.

M8007 Data Link Communication Initialize Flag (Master Station)
Data Link Communication Stop Flag (Slave Station)

M8007 has a different function at the master or slave station of the data link communication system.

Master station: Data link communication initialize flag

When M8007 at the master station is turned on during operation, the link configuration is checked to initialize the data link system. When a slave station is powered up after the master station, turn M8007 on to initialize the data link system. After a data link system setup is changed, M8007 must also be turned on to ensure correct communication.

Slave station: Data link communication stop flag

When a slave station does not receive communication data from the master station for 10 seconds or more in the data link system, M8007 turns on. When a slave station does not receive data in 10 seconds after initializing the data link system, M8007 also turns on at the slave station. When the slave station receives correct communication data, M8007 turns off.

M8080-M8116 Slave Station Communication Completion Relay (Master Station)

Special internal relays M8080 through M8116 are used to indicate the completion of data refresh. When data link communication with a slave station is complete, a special internal relay assigned for the slave station is turned on for one scan time at the master station.

Special Internal Relay	Slave Station Number	Special Internal Relay	Slave Station Number	Special Internal Relay	Slave Station Number
M8080	Slave Station 1	**M8092**	Slave Station 11	**M8104**	Slave Station 21
M8081	Slave Station 2	**M8093**	Slave Station 12	**M8105**	Slave Station 22
M8082	Slave Station 3	**M8094**	Slave Station 13	**M8106**	Slave Station 23
M8083	Slave Station 4	**M8095**	Slave Station 14	**M8107**	Slave Station 24
M8084	Slave Station 5	**M8096**	Slave Station 15	**M8110**	Slave Station 25
M8085	Slave Station 6	**M8097**	Slave Station 16	**M8111**	Slave Station 26
M8086	Slave Station 7	**M8100**	Slave Station 17	**M8112**	Slave Station 27
M8087	Slave Station 8	**M8101**	Slave Station 18	**M8113**	Slave Station 28
M8090	Slave Station 9	**M8102**	Slave Station 19	**M8114**	Slave Station 29
M8091	Slave Station 10	**M8103**	Slave Station 20	**M8115**	Slave Station 30
—	—	—	—	**M8116**	Slave Station 31

M8080 Communication Completion Relay (Slave Station)

When data link communication with a master station is complete, special internal relay M8080 at the slave station is turned on for one scan time.

M8117 All Slave Station Communication Completion Relay

When data link communication with all slave stations is complete, special internal relay M8117 at the master station is turned on for one scan time. M8117 at slave stations does not go on.

Programming WindLDR

The Communication page in the Function Area Settings is used to program the data link master and slave stations.

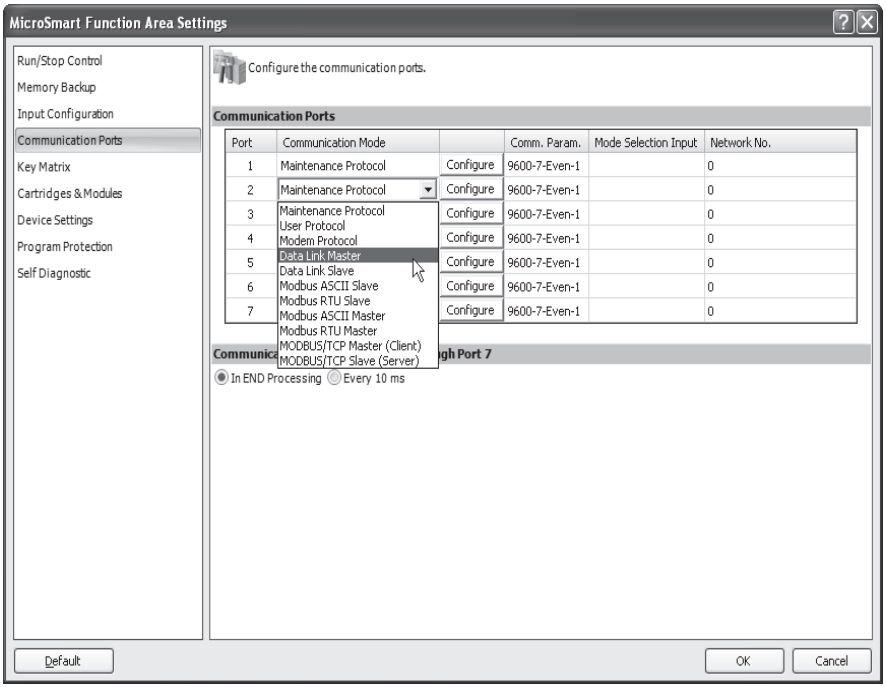
Since these settings relate to the user program, the user program must be downloaded to the CPU module after changing any of these settings.

Data Link Master Station

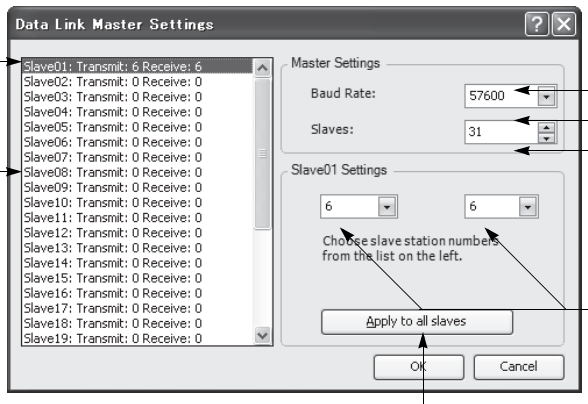
1. From the WindLDR menu bar, select **Configuration** > **Comm. Ports**.

The Function Area Settings dialog box for Communication Ports appears.

2. In the Communication Mode pull-down list for Port 2, select **Data Link Master**.



3. The Data Link Master Settings dialog box appears. Select a baud rate and the quantity of slave stations. Select a slave station number from the list on the left and make settings as shown below.



Click a slave number before making changes.

Slave Station Number
01 through 31

TX: Transmit from master
RX: Receive to master

Selected data quantity
0 through 6 words

Baud Rate
19200, 38400, or 57600 bps

Quantity of Slave Stations
1 through 31

Status DR (Port 3 through port 7)
When port 3 through port 7 are used, enter the data register for storing data link communication error codes.

Transmit/Receive Data Quantity (Words)
Select the quantity of data registers for transmit and receive data per slave station:
0 through 6 words

Selects the same quantities of transmit and receive data for all slave stations.

Note: When the data link system includes the MICRO^3 or MICRO^{3}C, select 19200 bps baud rate, and select 2 words of transmit/receive data for MICRO^3 or MICRO^{3}C.

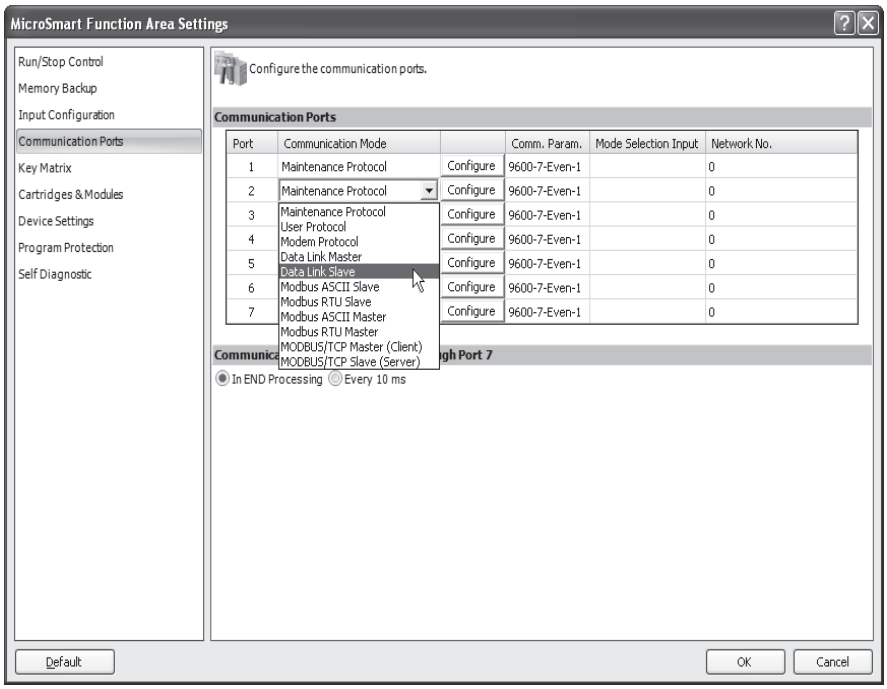
4. Click the **OK** button.

Data Link Slave Station

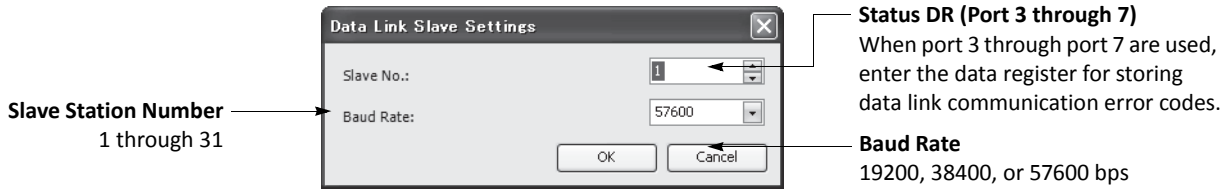
1. From the WindLDR menu bar, select **Configuration** > **Comm. Ports**.

The Function Area Settings dialog box for Communication Ports appears.

2. In the Communication Mode pull-down list for Port 2, select **Data Link Slave**.



3. The Data Link Slave Settings dialog box appears. Select a slave station number and baud rate.



4. Click the **OK** button.

D8040-D8044 and D8100 Data Link Slave Station Number

The data link slave station number can be changed by storing a number 1 through 31 into special data register allocated to port 2 through port 7, without the need for downloading the user program. If the number stored in special data register is not within 1 through 31, the slave station number in the Function Area Settings takes effect.

Port	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7
Data Register Number	D8100	D8040	D8041	D8042	D8043	D8044

Changing Data Link Slave Station Number of Port 2

1. Store a new data link slave station number in special data register D8100.

2. Initialize the data link master station, using one of the three methods: power down and up the master station, turn on M8007 (data link communication initialize flag) at the master station (see page 11-7), or from the WindLDR menu bar select **Online** > **Monitor** > **Monitor**, followed by **Online** > **Initialize** > **Initialize Data Link**.

Note: This function can be used only when data link slave station is assigned in the Function Area Settings as shown above.

Data Refresh

In the data link communication, the master station communicates with only one slave station in one communication cycle. When a slave station receives a communication from the master station, the slave station returns data stored in data registers assigned for data link communication. After receiving data from slave stations, the master station stores the data into data registers allocated to each slave station. The process of updating data into data registers is called refresh. When the maximum 31 slave stations are connected, the master station requires 31 communication cycles to communicate with all slave stations.

Mode	Separate Refresh Mode
Scan Time	Since the communication between the master station and slave stations proceeds independently of the user program scanning, the scan time is not affected.
Data Refresh Timing	At both master and slave stations, received data is refreshed at the END processing. Refresh completion can be confirmed with communication completion special internal relays M8080 through M8117.
Applicable Master Station	MicroSmart (FC4A/FC5A), OpenNet Controller, MICRO3, MICRO3C, FA-3S (PF3S-SIF4)
Applicable Slave Station	MicroSmart (FC4A/FC5A), OpenNet Controller, MICRO3, MICRO3C, FA-3S (PF3S-SIF4)

Note: When the data link system contains the MicroSmart (FC4A/FC5A) and MICRO^3/MICRO^{3}C, set the baud rate to 19200 bps and transmit/receive data quantity to 2 words in the Function Area Settings for the MicroSmart to communicate with MICRO^3/MICRO^{3}C stations.

Both master and slave stations refresh communication data at the END processing. When data refresh is complete, communication completion special internal relays M8080 through M8116 (slave station communication completion relay) go on at the master station for one scan time after the data refresh. At each slave station, special internal relay M8080 (communication completion relay) goes on.

When the master station completes communication with all slave stations, special internal relay M8117 (all slave station communication completion relay) goes on at the master station for one scan time.

Total Refresh Time at Master Station for Communication with All Slave Stations (Trfn)

The master station requires the following time to refresh the transmit and receive data for communication with all slave stations, that is the total of refresh times.

[Baud Rate 19200 bps] $Trfn = \sum Trf = \sum \{4.2\ ms + 2.4\ ms \times (Transmit\ Words + Receive\ Words) + 1\ scan\ time\}$

[Baud Rate 38400 bps] $Trfn = \sum Trf = \sum \{2.2\ ms + 1.3\ ms \times (Transmit\ Words + Receive\ Words) + 1\ scan\ time\}$

[Baud Rate 57600 bps] $Trfn = \sum Trf = \sum \{1.6\ ms + 0.9\ ms \times (Transmit\ Words + Receive\ Words) + 1\ scan\ time\}$

Example: Refresh Time

When data link communication is performed with such parameters as transmit words 6, receive words 6, slave stations 8, and average scan time 20 ms, then the total refresh time Trf8 for communication with all eight slave stations will be:

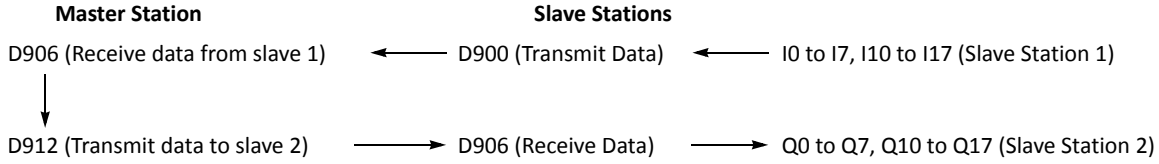
[Baud Rate 19200 bps] $Trf8 = \{4.2\ ms + 2.4\ ms \times (6 + 6) + 20\ ms\} \times 8 = 424.0\ ms$

[Baud Rate 38400 bps] $Trf8 = \{2.2\ ms + 1.3\ ms \times (6 + 6) + 20\ ms\} \times 8 = 302.4\ ms$

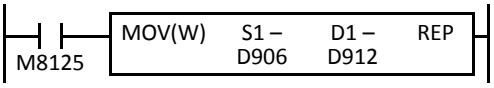
[Baud Rate 57600 bps] $Trf8 = \{1.6\ ms + 0.9\ ms \times (6 + 6) + 20\ ms\} \times 8 = 259.2\ ms$

Sample Program for Data Link Communication

This sample program demonstrates data communication from slave station 1 to the master station, then to slave station 2. Data of inputs I0 through I7 and I10 through I17 are stored to data register D900 (transmit data) at slave station 1. The D900 data is sent to data register D906 (receive data from slave 1) of the master station. At the master station, D906 data is moved to data register D912 (transmit data to slave 2). The D912 data is sent to data register D906 (receive data) of slave station 2, where the D906 data is set to outputs Q0 through Q7 and Q10 through Q17.



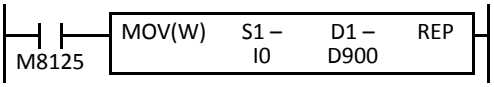
Master station program



M8125 is the in-operation output special internal relay which remains on during operation.

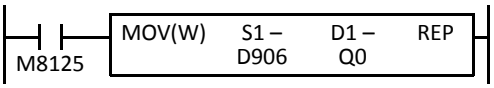
The data of data register D906 (receive data from slave station 1) is moved to data register D912 (transmit data to slave station 2).

Slave station 1 program



The 16-bit data of inputs I0 through I7 and I10 through I17 is moved to data register D900 (transmit data to master station).

Slave station 2 program



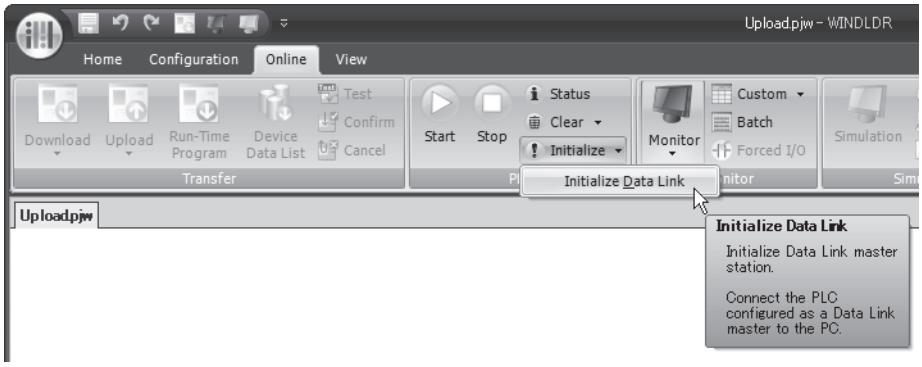
The data of data register D906 (receive data from master station) is moved to 16 output points of Q0 through Q7 and Q10 through Q17.

Operating Procedure for Data Link System

To set up and use a data link system, complete the following steps:

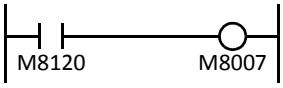
1. Connect the MicroSmart CPU modules at the master station and all slave stations as illustrated on page 11-2.
2. Create user programs for the master and slave stations. Different programs are used for the master and slave stations.
3. Using WindLDR, access **Configuration** > **Comm. Ports** and make settings for the master and slave stations. For programming WindLDR, see pages 11-8 and 11-9.
4. Download the user programs to the master and slave stations.
5. To start data link communication, power up slave stations first, and power up the master station at least 1 second later. Monitor the data registers used for data link at the master and slave stations.

Note: To enable data link communication, power up slave stations first. If a slave station is powered up later than or at the same time with the master station, the master station does not recognize the slave station. To make the master station recognize the slave station in this case, turn on special internal relay M8007 (data link communication initialize flag) at the master station (see page 11-7), or from the WindLDR menu bar select **Online** > **Monitor** > **Monitor**, followed by **Online** > **Initialize** > **Initialize Data Link**.



Data Link Initialization Program

If the master station does not recognize the slave station when the master station is powered up, include the following program into the user program for the master station.



M8120 is the initialize pulse special internal relay.

M8007 is the data link communication initialize flag.

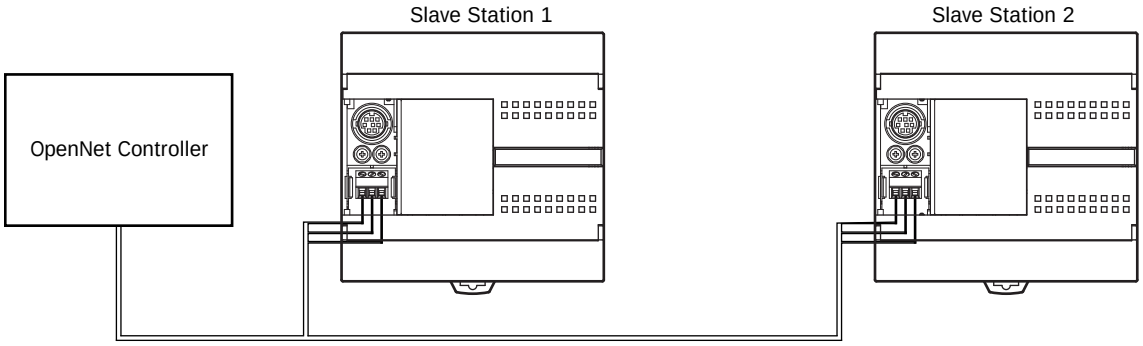
When the master station CPU module starts to run, M8120 turns on M8007 for one scan to initialize the data link communication. The master station will recognize the slave station.

Data Link with Other PLCs

The data link communication system can include IDEC's OpenNet Controller, MICRO^3/MICRO^{3}C micro programmable controllers, and FA-3S programmable controllers using serial interface modules.

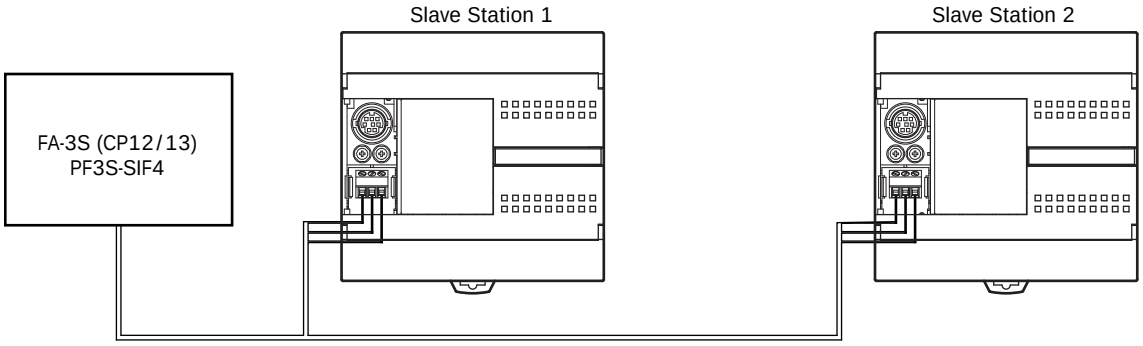
Data Link with OpenNet Controller

OpenNet Controller Settings	MicroSmart Settings	MicroSmart Settings
Transmit data: 6 words Receive data: 6 words Baud rate: 19200 or 38400 bps	Slave station number 1	Slave station number 2



Data Link with FA-3S High-performance CPU using Serial Interface Module PF3S-SIF4

FA-3S (PF3S-SIF4) Settings	MicroSmart Settings	MicroSmart Settings
Transmit data: 6 words Receive data: 6 words Baud rate: 19200 or 38400 bps	Slave station number 1	Slave station number 2



D8101 Data Link Transmit Wait Time (ms)

When a data link system consists of an FC5A master station and FA3S slave stations, use port 2 of the FC5A CPU module and store 20 to special data register D8101 of the FC5A CPU module at the master station. This way, the FC5A CPU module has a data link transmit wait time of 20 ms.

Data Register Number	Description
D8101	20: D8101 value specifies data link transmit wait time in ms.

12: MODBUS ASCII/RTU COMMUNICATION

Introduction

This chapter describes the Modbus master and slave communication function of the MicroSmart CPU module.

All FC5A MicroSmart CPU modules can be connected to the Modbus network using communication port 2 to port 7 through the RS485 or RS232C line. The MicroSmart Modbus communication function is compatible with ASCII and RTU modes.

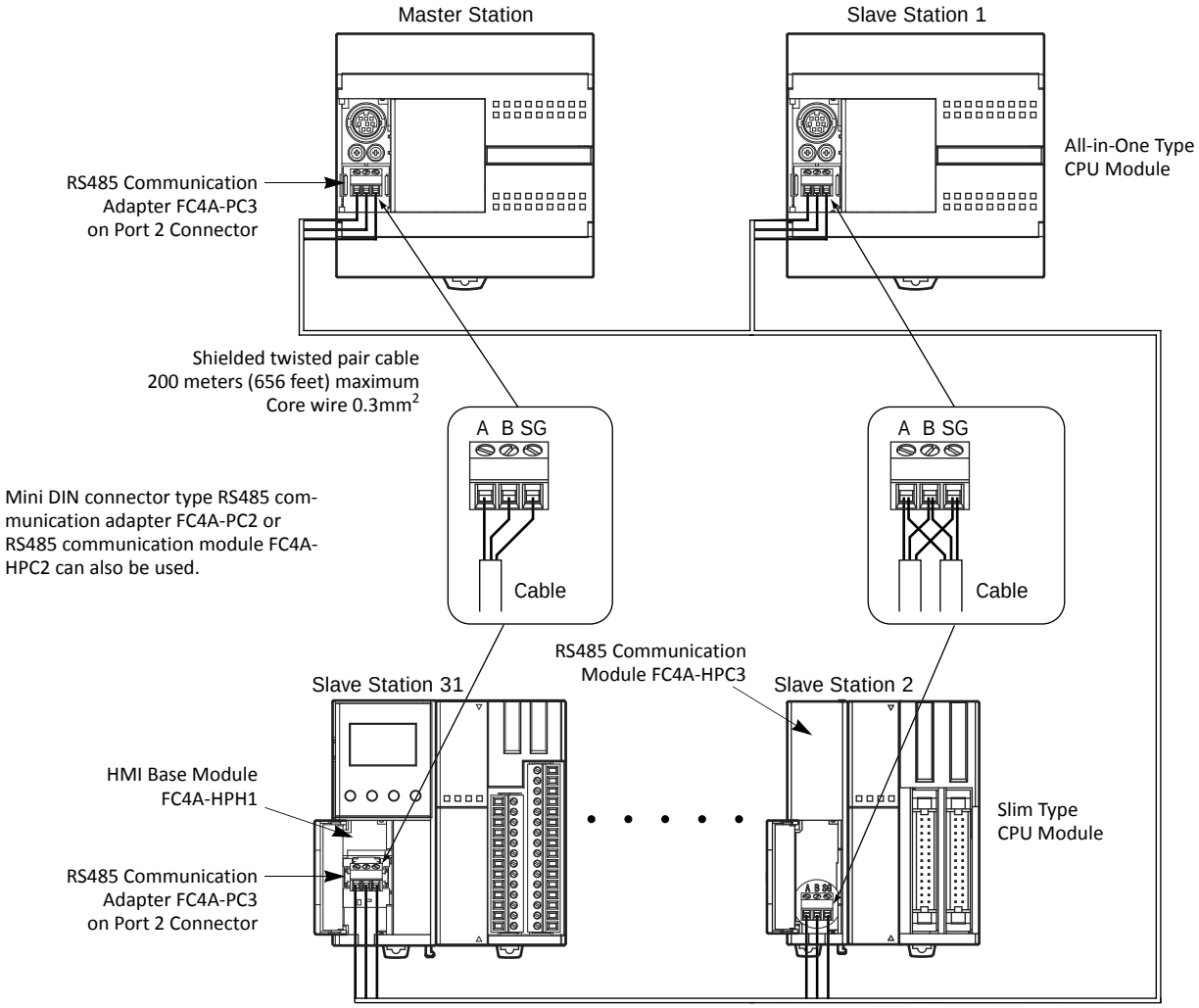
Modbus Communication System Setup

To set up a 1:N Modbus communication system, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector on the all-in-one type CPU module.

When using the slim type CPU module, mount the RS485 communication module (FC4A-HPC3) next to the CPU module. When using the optional HMI module with the slim type CPU module, install the RS485 communication adapter (FC4A-PC3) to the port 2 connector on the HMI base module.

FC5A-SIF4 expansion RS485 communication module can also be mounted to the CPU module to add port 3 through port 7 to set up a 1:N Modbus communication system.

Connect the RS485 terminals A, B, and SG on every CPU module using a shielded twisted pair cable as shown below. The total length of the cable for the RS485 Modbus communication system can be extended up to 200 meters (656 feet).



To set up RS232C communication system, use RS232C communication adapter (FC4A-PC1), RS232C communication module (FC4A-HPC1), or expansion RS232C communication module (FC5A-SIF2). The RS232C can set up only 1:1 communication system.

Note: When port 1 or 2 is used for Modbus communication, use the user communication cable 1C (FC2A-KP1C). For details about the system setup for port 1 or 2, see page 10-3. When preparing a cable for port 1, keep pins 6 and 7 open.

Modbus Master Communication

Modbus master communication settings and request tables for Modbus slave stations can be programmed using the WindLDR Function Area Settings. Communication with slave stations are performed in synchronism with user program execution, and the communication data are processed at the END processing in the order of request numbers specified in the request table. When request execution devices are designated, requests are executed only when the corresponding request execution device is turned on. When request execution devices are not designated, all requests are executed continuously.

Modbus Master Communication Specifications

Mode	ASCII Mode	RTU Mode
Baud Rate (bps) *1	9600, 19200, 38400, 57600, 115200	
Data Bits	7 bits (fixed)	8 bits (fixed)
Stop bits	1, 2 bits	
Parity	Even, Odd, None	
Slave Number	1 to 247 (0: broadcast slave number)	
Maximum Number of Slaves	31	
Receive Timeout *2	10 to 2550 ms (in increments of 10 ms)	
Timeout between Characters	10 ms	
Transmission Wait Time *3	1 to 5000 ms (in increments of 1 ms)	
Retry Cycles	1 to 10	

*1: 115200 bps can be selected when FC5A-SIF4 is used on port 3 through port 7.
*2: Specifies the period of time before receiving a response frame from a slave.
*3: D8054 is a special data register for Modbus communication transmission wait time (×1 ms) for port 2. Using D8054 can delay transmission from the MicroSmart. When port 3 through port 7 are used, the transmission wait time is designated in Communication Settings dialog box. For details, see page 12-5

Modbus Master Communication Start and Stop

When request execution devices are designated in the Modbus master request table, internal relays as many as the request quantity are allocated to execute Modbus master communication. The internal relays are allocated in the order of requests. For example, when internal relay M0 is designated as the request execution device, M0 is allocated to request No. 1, M1 to request No. 2, and so on. To execute a request, turn on the corresponding request execution device. When communication is completed, the request execution device turns off automatically. When it is required to send requests continuously, keep the corresponding request execution device on using a SET or OUT instruction.

When request execution devices are not designated, all requests programmed in the request table are executed continuously.

Communication Completion and Communication Error

Modbus communication finishes when a read or write process is completed successfully or when a communication error occurs. Immediately after a request communication has been completed, Modbus communication completion relay M8080 turns on for 1 scan time. At the same time, the completed request number and error code are stored to special data register D8053. The data in D8053 is valid only for the 1 scan time when M8080 is on.

When a communication error occurs, communication error special internal relay M8005 also turns on for 1 scan time immediately after the error. Communication error occurs when communication failure has repeated more than the designated retry cycles or when the master station does not receive response within the designated receive timeout period. When a communication error occurs, the request is canceled and the next request is transmitted.

M8005, D8053, and D8080 are used only when Modbus master is used on port 2.

Notes:
- Modbus master processes a maximum of one Modbus request per scan.
- When Modbus master is used on port 3 through port 7, the communication status can be confirmed by checking the error data stored in data registers allocated to each Modbus request in Modbus Master Request Table dialog box.

Communication Error Data of Each Slave

Error data of each slave are stored to special data registers D8069 through D8099 (error station number and error code). Error station number (high-order byte) and error code (low-order byte) are stored to the data registers in the order of error occurrence. When an error occurs at a slave station where an error has already occurred, only the error code is updated with the slave number data unchanged. Data of D8069 through D8099 are cleared when the CPU module is powered up.

D8069 through D8099 are used only when Modbus master is used on port 2.

Communication Error Data of Each Request

Error data of each request in the entire request table can be confirmed. To confirm error data of each request, select to use Error Status in the Request Table from the Function Area Settings and enter the data register number.

When Use a single DR for all communication requests is not selected, starting with the data register number, data registers as many as the quantity of requests are reserved for storing error data. When an error occurs for a request, an error code is stored to a corresponding data register.

When Use a single DR for all communication requests is selected, the same data register is shared by all requests. When an error occurs for a request, an error code is stored to the data register and the old value is overwritten.

Number of Requests in Modbus Master

The number of requests that can be programmed in a request table depends on CPU module type and the port number.

CPU Module	All-in-One Type CPU Modules	Slim Type CPU Modules	
Port	**Port 2 through Port 5**	**Port 2**	**Port 3 through Port 7**
No. of requests	255	2040	255

Note: 8 bytes of the user program area are needed per each request.

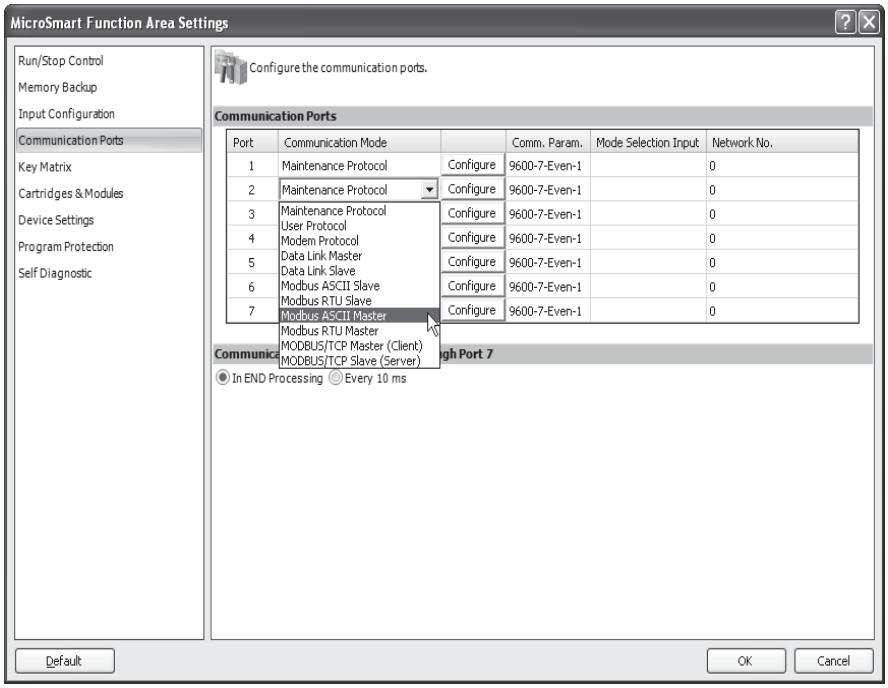
Programming Modbus Master Using WindLDR

Modbus master communication is programmed for either Modbus ASCII or Modbus RTU mode using WindLDR. Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

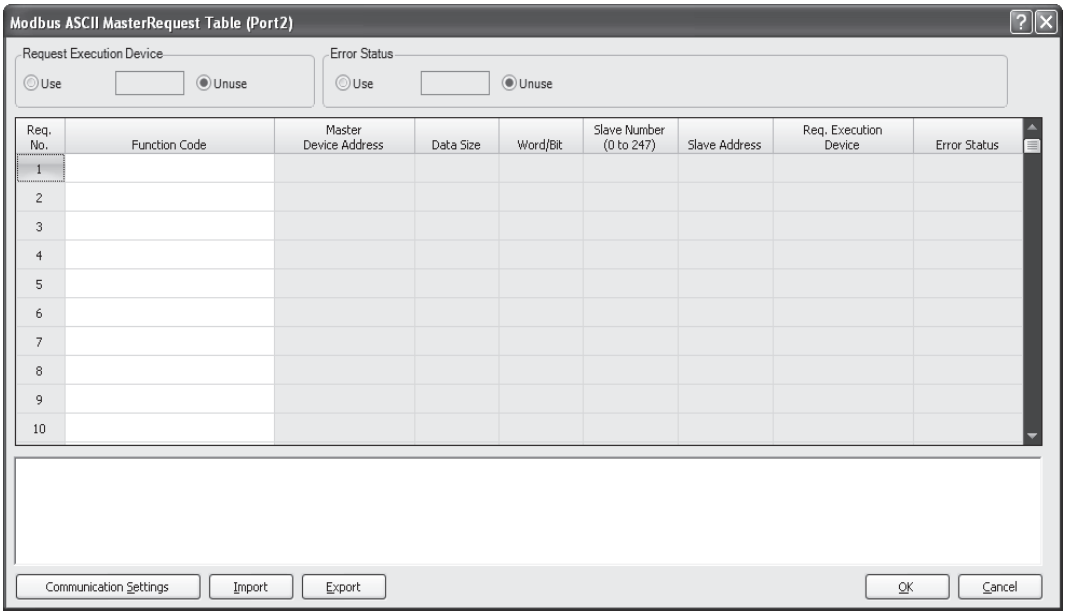
1. From the WindLDR menu bar, select **Configuration** > **Comm. Ports**.

The Function Area Settings dialog box for Communication Ports appears.

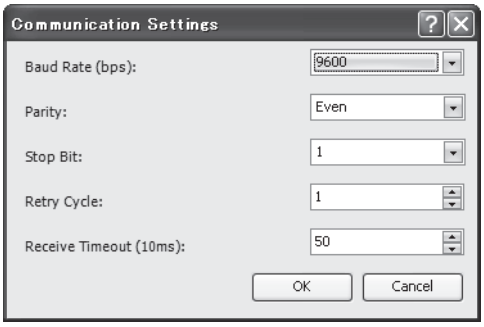
2. In the Communication Mode pull-down list for Port 2, select **Modbus ASCII Master** or **Modbus RTU Master**.



3. Click the **Configure** button for Port 2. The Modbus ASCII or RTU Master Request Table appears.



4. Click the **Communication Settings** button. The Communication Settings dialog box appears. Change settings, if required.



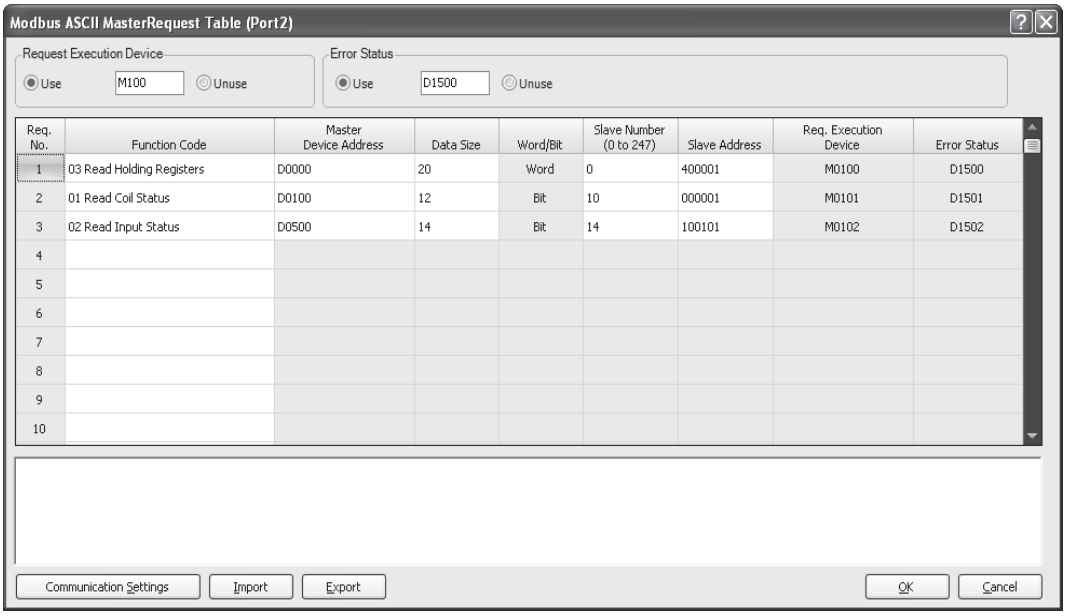
Baud Rate (bps) (Note 1)	9600, 19200, 38400, 57600, 115200
Parity	Even, Odd, None
Stop Bits	1 or 2
Retry Cycle	1 to 10
Receive Timeout	1 to 255 (×10 ms)
Transmission Wait Time (Note 2)	0 to 5000 (ms)

Note 1: 115200 bps can be used only when Modbus master is used on port 3 through port 7.

Note 2: Designate the transmission wait time when Modbus master is used on port 3 through port 7.

5. Click the **OK** button to return to the Modbus ASCII or RTU Master Request Table. Designate requests under the Function Code. A maximum of 255 (or 2040 on CPU modules with system program version 110 or higher) requests can be entered in one request table.

Choose to use Request Execution Devices and Error Status data registers. When using Request Execution Devices and Error Status data registers, enter the first number of the devices.



Notes for Editing the Request Table

Request execution devices and error status data registers are allocated in the order of request numbers. When deleting a request or changing the order of requests, the relationship of the request to the request execution devices and error status data register is changed. If the internal relay or data register is used in the user program, the device addresses must be changed accordingly. After completing the changes, download the user program again.

6. When editing the Master Request Table is complete, click the **OK** button to save changes.

7. After closing the Master Request Table, edit a user program for special data register D8054 (transmission wait time) and error detection.

8. Download the user program to the CPU module.

Now, programming for the Modbus master is complete. Details about parameters and valid values are as follows.

Function Code

The MicroSmart accepts eight function codes as listed in the table below:

Function Code	Data Size	Slave Address	MicroSmart as Modbus Slave
01 Read Coil Status	1 to 128 bits	000001 - 065535	Reads bit device statuses of Q (output), R (shift register), or M (internal relay).
02 Read Input Status	1 to 128 bits	100001 - 165535	Reads bit device statuses of I (input), T (timer contact), or C (counter contact).
03 Read Holding Registers	1 to 64 words	400001 - 465535	Reads word device data of D (data register), T (timer preset value), or C (counter preset value).
04 Read Input Registers	1 to 64 words	300001 - 365535	Reads word device data of T (timer current value) or C (counter current value).
05 Force Single Coil	1 bit	000001 - 065535	Changes a bit device status of Q (output), R (shift register), or M (internal relay).
06 Preset Single Register	1 word	400001 - 465535	Changes word device data of D (data register).
15 Force Multiple Coils	1 to 128 bits	000001 - 065535	Changes multiple bit device statuses of Q (output), R (shift register), or M (internal relay).
16 Preset Multiple Registers	1 to 64 words	400001 - 465535	Changes multiple word device data of D (data register).

Master Device Address

When function code 01, 02, 03, or 04 is selected to read data from Modbus slaves, designate the first data register or internal relay number to store the data received from the Modbus slave. When function code 05, 06, 15, or 16 is selected to write data to Modbus slaves, designate the first data register or internal relay number to store the data to write to the Modbus slave. Data registers and internal relays can be designated as the master device address.

Data Size and Word/Bit

Designate the quantity of data to read or write. The valid data size depends on the function code. When function code 01, 02, 05, or 15 is selected, designate the data size in bits. When function code 03, 04, 06, or 16 is selected, designate the data size in words. For valid data sizes, see the table above.

Slave No.

Designate slave numbers 0 through 247. The same slave number can be designated repeatedly for different request numbers which can be 1 through 255 (or 2040 on CPU modules with system program version 110 or higher). In the Modbus communication, slave number 0 is used for a broadcast slave number.

Slave Address

Designate data memory addresses of Modbus slaves. The valid slave address range depends on the function code. For valid slave addresses, see the table above.

Request Execution Device

To use request execution devices, click the radio button for “Use” and designate the first internal relay number in the Modbus ASCII or RTU Master Request Table. Devices used for executing requests are automatically listed in the table. To execute a request, turn on the corresponding request execution device.

Slim type CPU modules with system program version 110 or higher can also designate data registers the Request Execution Device. When the first data register number is designated as the Request Execution Device, data register bits as many as the number of requests are allocated from the least significant bit of the first data register. Data register bits assigned as the execution relays are automatically listed in the Request Table.

When request execution devices are not designated, all requests programmed in the Request Table are executed continuously.

Error Status Data Register

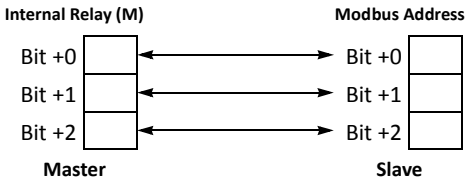
To use error status data registers, click the radio button for “Use” and designate the first data register number in the Modbus ASCII or RTU Master Request Table. Data registers used for storing error statuses are automatically listed in the table. When Use a single DR for all communication requests is selected, the first data register is shared by all requests.

Processing Requests

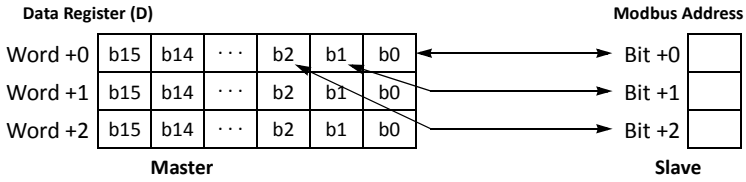
The data for Modbus communication are processed between the master and slaves as shown below.

Bit Data at Slaves (Function Codes 01, 02, 05, and 15)

- **Master Device Address: Internal Relay**

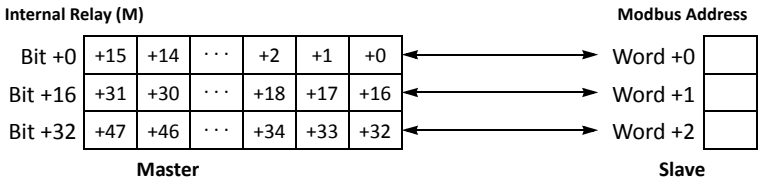


- **Master Device Address: Data Register**

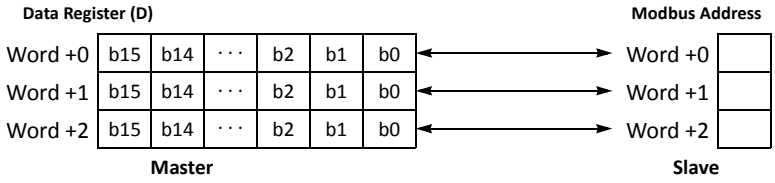


Word Data at Slaves (Function Codes 03, 04, 06, and 16)

- **Master Device Address: Internal Relay**



- **Master Device Address: Data Register**



Device Addresses for Modbus Master

Special internal relays and special data registers are allocated to Modbus master communication as shown below.

Internal Relay and Special Internal Relay Device Addresses

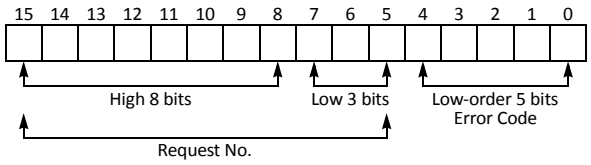
Port 2	Ports 3 to 7	Description	R/W
M8005	—	**Communication Error** When a communication error occurs, communication error special internal relay M8005 turns on for 1 scan time immediately after the error. Communication error occurs when communication failure has repeated more than the designated retry cycles or when the master station does not receive response within the designated receive timeout period. When a communication error occurs, the request is canceled and the next request is transmitted. The completed request number and error code are stored to special data register D8053.	R
M8080	—	**Modbus Communication Completion Relay** Immediately after a request communication has been completed, Modbus communication completion relay M8080 turns on for 1 scan time. Similarly, when an error occurs, M8080 turns on for 1 scan time. At the same time, the completed request number and error code are stored to special data register D8053.	R
Function Area Settings		**Request Execution Device** When a request execution device is turned on, the corresponding request is executed. When communication is completed, the request execution device turns off automatically.	R/W

Data Register and Special Data Register Device Addresses

Port 2	Ports 3 to 7	Description	R/W
D8053 (Note)	—	**Modbus Communication Error Code** When a Modbus communication is completed, the request number and error code are stored. High-order 11 bits: Request No. 1 to 2040 Low-order 5 bits: Error code 00h: Normal completion 01h: Function error 02h: Access destination error (address out of range, address+device quantity out of range) 03h: Device quantity error, 1-bit write data error 11h: ASCII code error (ASCII mode only) 12h: Frame length error 13h: BCC error 14h: Slave number error 16h: Timeout error	R
D8054	Function Area Settings	**Modbus Communication Transmission Wait Time** When the MicroSmart sends communication, transmission wait time can be designated by storing a wait time value to D8054. Valid values are 1 through 5000 in milliseconds.	R/W
D8069-D8099	—	**Error Station Number and Error Code** When a communication error occurs in the Modbus communication, the slave number (high-order byte) and error code (low-order byte) are stored to these data registers. Error codes are the same as D8053. When the CPU module is powered up, these data registers are cleared.	R
Function Area Settings		**Error Status** When a communication error occurs in the Modbus communication, the slave number (high-order byte) and error code (low-order byte) are stored to the Error Status data registers allocated to each request. Error codes are the same as D8053. When the CPU module is powered up, these data registers are cleared. When Use a single DR for all communication requests is selected, the Error Status data register is shared by all requests. The value in the data register is overwritten every time an error occurs.	R

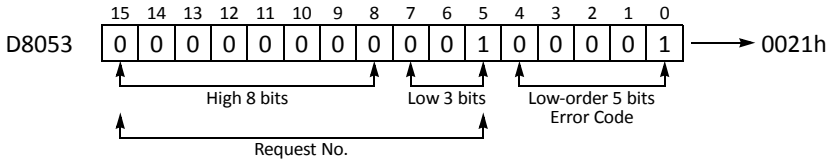
Note: The 16 bits in data register D8053 are assigned as shown below.

The 11-bit request number comprises high 8 bits and low 3 bits.



Low 3 Bits	Request No. Range
000	1 to 255
001	256 to 511
010	512 to 767
011	768 to 1023
100	1024 to 1279
101	1280 to 1535
110	1536 to 1791
111	1792 to 2040

Example: For request No. 256 and function error (01h), D8053 stores the following value.



Modbus Slave Communication

Modbus slave communication is made possible by selecting Modbus ASCII Slave or Modbus RTU Slave for port 1 to port 7 in the WindLDR Function Area Settings. When a Modbus slave receives a request from the Modbus master, the Modbus slave reads or writes data according to the request. The request is processed at the END processing of the user program.

Modbus Slave Communication Specifications

Mode	ASCII Mode	RTU Mode
Baud Rate (bps) *1	9600, 19200, 38400, 57600, 115200	
Data Bits	7 bits (fixed)	8 bits (fixed)
Stop bits	1, 2 bits	
Parity	Odd, even, none	
Slave Number	1 to 31 1 to 247 (CPU modules with system program version 110 or higher)	
Response Time *2	1 to 5000 ms (in increments of 1 ms)	
Timeout between Characters *3	—*4	1.5 characters minimum *5
Timeout between Frames *3	—*4	3.5 characters minimum *6

*1: 115200 bps can be selected when FC5A-SIF4 is used on port 3 through port 7.

*2: D8054 is a special data register for Modbus communication transmission wait time (×1 ms) for port 2. 0 designates 1 ms, and 5000 or more designates 5000 ms. Using D8054 can delay transmission from the MicroSmart. When port 1 or 3 through 7 are used, the response time is 1 ms.

*3: When timeout occurs, the MicroSmart discards the received data and waits for the first frame of the next valid communication.

*4: ASCII mode finds the beginning of a frame by the ":" code. While the MicroSmart is receiving an incoming request message and at the same time receives a ":" code, the MicroSmart discards the received data and waits for a slave number.

*5: For communication at 19200 bps or higher, space between characters needs to be a minimum of 0.75 ms.

*6: For communication at 19200 bps or higher, space between frames needs to be a minimum of 1.75 ms.

Communication Completion and Communication Error

Modbus communication finishes when a read or write process is completed successfully or when a communication error occurs. Immediately after a request communication has been completed, Modbus communication completion relay M8080 turns on for 1 scan time. When a communication error occurs, the error code is stored to special data register D8053. The data in D8053 is valid only for the 1 scan time when M8080 is on.

When a communication error occurs, communication error special internal relay M8005 also turns on for 1 scan time immediately after the error.

M8080 and D8053 are used only when Modbus master is used on port 2.

Address Map

Modbus Device Name	Modbus Address Map (Decimal) *1	Communication Frame Address *2	MicroSmart Device *3	Applicable Function Code
Coil (000000 and above)	000001 - 000504	0000 - 01F7	Q0 - Q627	1, 5, 15
	000701 - 000956	02BC - 03BB	R0 - R255	
	001001 - 003048	03E8 - 07F7	M0 - M2557	
	009001 - 009256	2328 - 2427	M8000 - M8317	
Input Relay (100000 and above)	100001 - 100504	0000 - 01F7	I0 - I627	2
	101001 - 101256	03E8 - 04E7	T0 - T255 (timer contact)	
	101501 - 101756	05DC - 06DB	C0 - C255 (counter contact)	
Input Register (300000 and above)	300001 - 300256	0000 - 00FF	T0 - T255 (timer current value)	4
	300501 - 300756	01F4 - 02F3	C0 - C255 (counter current value)	
Holding Register (400000 and above)	400001 - 408000	0000 - 1F3F	D0 - D7999	3, 6, 16
	408001 - 408500	1F40 - 2133	D8000 - D8499	
	409001 - 409256	2328 - 2427	T0 - T255 (timer preset value)	3
	409501 - 409756	251C - 261B	C0 - C255 (counter preset value)	
	410001 - 450000	2710 -C34F	D10000 - D49999	3, 6, 16

*1: Addresses generally used for Modbus communication. Calculation method of Modbus addresses for MicroSmart devices are described below.

*2: These 4-digit addresses are used in the communication frame. To calculate the address used in communication frame, extract lower 5 digits of the Modbus address, subtract 1 from the value, and convert the result into hexadecimal.

*3: These device addresses represent the slim type CPU module. For the device addresses of the all-in-one type CPU modules, see page 6-1.

Calculating Modbus Addresses for MicroSmart Devices

MicroSmart Device		Calculating Modbus Address	Calculation Example
I, Q, M	M XXX X (2): Octal (1): Decimal	((1) – (4)) × 8 + (2) + (5) Minimum address Offset	Example: M1325 (132 – 0) × 8 + 5 + 1001 = 2062 Modbus address: 2062 2062 – 1 = 2061 = 80Dh Communication frame address: 080Dh
R, T, C, D	D XXXXX (3): Decimal	((3) – (4)) + (5) Minimum address Offset	Example: D1756 (1756 – 0) + 400001 = 401757 Modbus address: 401757 Extract lower 5 digits → 1757 1757 – 1 = 1756 = 6CDh Communication frame address: 06DCh

Modbus Device Name	MicroSmart Device	Minimum Address (4)	Offset (5)
Coil	Q0 - Q627	0	1
	R0 - R255	0	701
	M0 - M2557	0	1001
	M8000 - M8317	8000	9001
Input Relay	I0 - I627	0	100001
	T0 - T255 (timer contact)	0	101001
	C0 - C255 (counter contact)	0	101501
Input Register	T0 - T255 (timer current value)	0	300001
	C0 - C255 (counter current value)	0	300501
Holding Register	D0 - D7999	0	400001
	D8000 - D8499	8000	408001
	T0 - T255 (timer preset value)	0	409001
	C0 - C255 (counter preset value)	0	409501
	D10000 - D49999	10000	410001

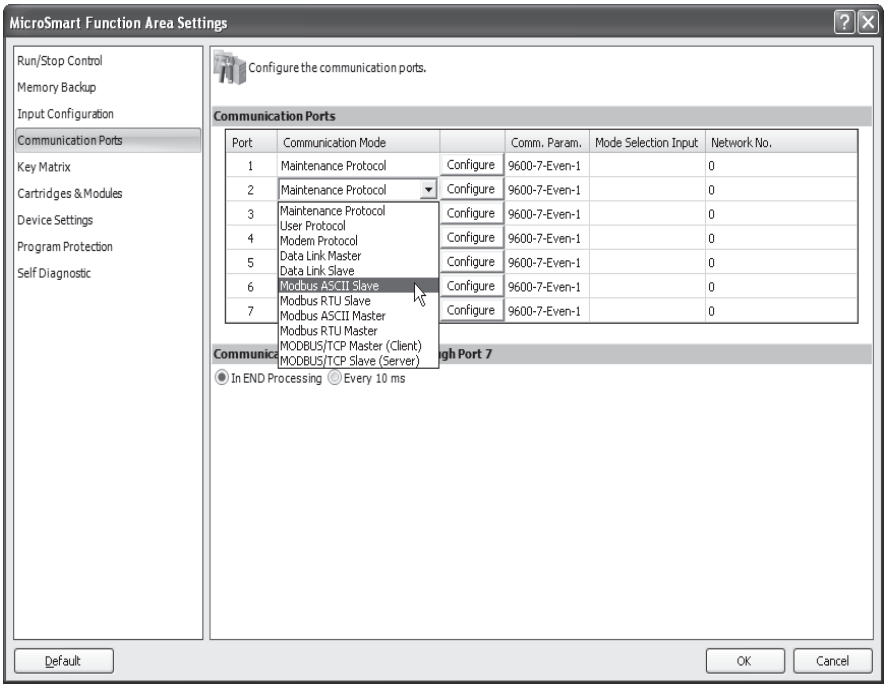
Programming Modbus Slave Using WindLDR

Modbus slave communication is programmed for either Modbus ASCII or Modbus RTU mode using WindLDR. Since these settings relate to the user program, the user program must be downloaded to the MicroSmart after changing any of these settings.

1. From the WindLDR menu bar, select **Configuration** > **Comm. Ports**.

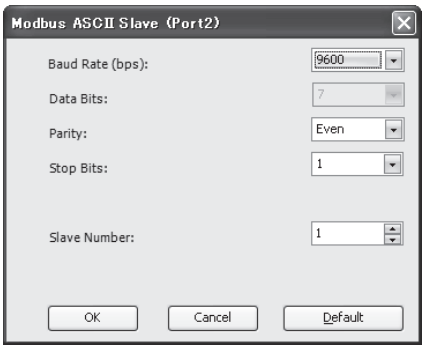
The Function Area Settings dialog box for Communication Ports appears.

2. In the Communication Mode pull-down list for Port 2, select **Modbus ASCII Slave** or **Modbus RTU Slave**.

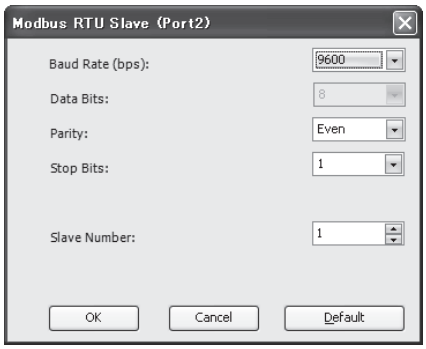


3. Click the **Configure** button. The Communication Parameters dialog box appears. Change settings, if required.

Modbus ASCII Slave



Modbus RTU Slave



Baud Rate (bps)	9600 19200 38400 57600 115200
Data Bits	7 (ASCII mode) 8 (RTU mode)
Parity	Even, Odd, None
Stop Bits	1 or 2
Slave Number	1 to 31 *

* 1 to 247 (CPU modules with system program version 110 or higher)

4. Click the **OK** button to save changes.

5. After closing the Function Area Settings screen, edit a user program for special data register D8054 (transmission wait time) and error detection.

6. Download the user program to the CPU module.

Now, programming for the Modbus slave is complete. Details about parameters and valid values are as follows.

Device Addresses for Modbus Slave

Special internal relays and special data registers are allocated to Modbus slave communication as shown below.

Special Internal Relay Device Addresses

Port 2	Ports 1, 3 to 7	Description	R/W
M8005	—	**Communication Error** When a communication error occurs, communication error special internal relay M8005 turns on for 1 scan time immediately after the error. The error code is stored to special data register D8053.	R
M8080	—	**Modbus Communication Completion Relay** Immediately after a request communication has been completed, Modbus communication completion relay M8080 turns on for 1 scan time. Similarly, when an error occurs, M8080 turns on for 1 scan time. At the same time, the error code is stored to special data register D8053.	R

Special Data Register Device Addresses

Port 2	Ports 1, 3 to 7	Description	R/W
D8053	—	**Modbus Communication Error Code** When a Modbus communication error occurs, an error code is stored. 01h: Function error 02h: Access destination error (address out of range, address+device quantity out of range) 03h: Device quantity error, 1-bit write data error 11h: ASCII code error (ASCII mode only) 12h: Frame length error 13h: BCC error	R
D8054	—	**Modbus Communication Transmission Wait Time** When the MicroSmart sends communication, transmission wait time can be designated by storing a wait time value to D8054. Valid values are 1 through 5000 in milliseconds.	R/W
D8100	Port 1: — Port 3: D8040 Port 4: D8041 Port 5: D8042 Port 6: D8043 Port 7: D8044	**Modbus Slave Number (CPU modules with system program version 110 or higher)** The Modbus slave number of port 2 through port 7 can be changed by storing a number 1 through 247 into the corresponding special data registers, without the need for downloading the user program. If the data stored in the special data register is not within the valid range of slave number, the slave number designated in Function Area Settings is used. For example, in order to change the Modbus slave number of port 2, store a new Modbus slave number in special data register D8100. As soon as the data in D8100 is changed, the data becomes the Modbus slave number of port 2. The data stored in these special data registers are saved to the ROM in the CPU module and maintained even when the backup battery is dead.	R/W

Communication Protocol

This section describes the communication frame format used for Modbus communication. ASCII mode and RTU mode use different communication frame formats.

Communication Frame Format

- **ASCII Mode**

Request from Modbus Master

":"	Slave No.	Function Code	Data	LRC	CR LF
1 byte	2 bytes	2 bytes		2 bytes	2 bytes

ACK Reply from Modbus Slave

":"	Slave No.	Function Code	Data	LRC	CR LF
1 byte	2 bytes	2 bytes		2 bytes	2 bytes

NAK Reply from Modbus Slave

":"	Slave No.	Function Code + 80H	Error Code	LRC	CR LF
1 byte	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

- **RTU Mode**

Request from Modbus Master

Idle 3.5 characters	Slave No.	Function Code	Data	CRC	Idle 3.5 characters
	1 byte	1 byte		2 bytes	

ACK Reply from Modbus Slave

Idle 3.5 characters	Slave No.	Function Code	Data	CRC	Idle 3.5 characters
	1 byte	1 byte		2 bytes	

NAK Reply from Modbus Slave

Idle 3.5 characters	Slave No.	Function Code + 80H	Error Code	CRC	Idle 3.5 characters
	1 byte	1 byte	1 byte	2 bytes	

Note: Idle means no data flowing on the communication line.

Communication Frame Format

ASCII mode finds the beginning of a frame by the ":" code. While the MicroSmart is receiving an incoming request message and at the same time receives a ":" code, the MicroSmart discards the received data and waits for a slave number.

RTU mode requires a minimum of 3.5-character-long idle time between frames to determine the beginning of a frame. The MicroSmart Modbus master sends requests at idle intervals of 5 ms, which can be changed by storing a required value to special data register D8054.

Slave No.

The MicroSmart can be assigned slave numbers 1 through 31 (or 247 on CPU modules with system program version 110 or higher). In the 1:1 communication using RS232C, the same slave number must be set in the master and the MicroSmart.

Slave No. 0 is reserved for broadcast slave number and is used to clear all device data in the slave, or the MicroSmart. In this case, the MicroSmart does not send a reply to the master.

LRC and CRC

ASCII mode uses LRC check codes and RTU mode uses CRC check codes.

- **Modbus ASCII Mode — Calculating the LRC (longitudinal redundancy check)**

Calculate the BCC using LRC for the range from the slave number to the byte immediately before the BCC.

1. Convert the ASCII characters in the range from the slave number to the byte immediately before the BCC, in units of two characters, to make 1-byte hexadecimal data. (Example: 37h, 35h → 75h)
2. Add up the results of step **1**.
3. Invert the result bit by bit, and add 1 (2's complement).
4. Convert the lowest 1-byte data to ASCII characters. (Example: 75h → 37h, 35h)
5. Store the two digits to the BCC (LRC) position.

- **Modbus RTU Mode — Calculating the CRC-16 (cyclic redundancy checksum)**

Calculate the BCC using CRC-16 for the range from the slave number to the byte immediately before the BCC. The generation polynomial is: $X^{16} + X^{15} + X^2 + 1$.

1. Take the exclusive OR (XOR) of FFFFh and the first 1-byte data at the slave number.
2. Shift the result by 1 bit to the right. When a carry occurs, take the exclusive OR (XOR) of A001h, then go to step **3**. If not, directly go to step **3**.
3. Repeat step **2**, shifting 8 times.
4. Take the exclusive OR (XOR) of the result and the next 1-byte data.
5. Repeat step **2** through step **4** up to the byte immediately before the BCC.
6. Swap the higher and lower bytes of the result of step **5**, and store the resultant CRC-16 to the BCC (CRC) position. (Example: 1234h → 34h, 12h)

Communication Format

This section describes the communication format for each function code from the slave number up to immediately before the check code.

Function Code 01 (Read Coil Status) and Function Code 02 (Read Input Status)

Function code 01 reads bit device statuses of Q (output), R (shift register), or M (internal relay). One through 128 consecutive bits can be read out.

Function code 02 reads bit device statuses of I (input), T (timer contact), or C (counter contact). One through 128 consecutive bits can be read out.

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	No. of Bits
xxh	01h / 02h	xxxxh	xxxxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Quantity of Data	First 8 Bits	Second 8 Bits		Last 8 Bits
xxh	01h / 02h	xxh	xxh	xxh		xxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	81h / 82h	xxh

Communication Example

Purpose	Read 15 bits starting at output Q10. Q10 → (1 – 0) × 8 + 0 + 1 = 9 Modbus address: 9 9 – 1 = 8 = 8h Communication frame address: 0008h
Condition	Slave No. 8 Q10 through Q26 binary data: 1234h

- **ASCII Mode**

Request from Modbus Master	':' 3038 3031 30303038 30303046 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3031 3032 3334 3132 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3831 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 01 0008 000F (CRC)
ACK Reply from Modbus Slave	08 01 02 34 12 (CRC)
NAK Reply from Modbus Slave	08 81 xx (CRC)

Function Code 03 (Read Holding Registers) and Function Code 04 (Read Input Registers)

Function code 03 reads word device data of D (data register), T (timer preset value), or C (counter preset value). One through 64 consecutive words can be read out.

Function code 04 reads word device data of T (timer current value) or C (counter current value). One through 64 consecutive words can be read out.

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	No. of Words
xxh	03h / 04h	xxxxh	xxxxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Quantity of Data	First High Byte	First Low Byte		Last Low Byte
xxh	03h / 04h	xxh	xxh	xxh		xxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	83h / 84h	xxh

- **Communication Example**

Purpose	Read 2 words starting at data register D1710. D1710 → (1710 – 0) + 400001 = 401711 Modbus address: 401711 Extract lower 5 digits → 1711 1711 – 1 = 1710 = 6AEh Communication frame address: 06AEh
Condition	Slave No. 8 D1710 data: 1234h D1711 data: 5678h

- **ASCII Mode**

Request from Modbus Master	':' 3038 3033 30364145 30303032 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3033 3034 3132 3334 3536 3738 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3833 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 03 06AE 0002 (CRC)
ACK Reply from Modbus Slave	08 03 04 12 34 56 78 (CRC)
NAK Reply from Modbus Slave	08 83 xx (CRC)

Function Code 05 (Force Single Coil)

Function code 05 changes a bit device status of Q (output), R (shift register), or M (internal relay).

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	OFF: 0000H ON: FF00H
xxh	05h	xxxxh	xxxxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Address	OFF: 0000H ON: FF00H
xxh	05h	xxxxh	xxxxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	85h	xxh

Communication Example

Purpose	Force internal relay M1320 on. M1320 → (132 – 0) × 8 + 0 + 1001 = 2057 Modbus address: 2057 2057 – 1 = 2056 = 808h Communication frame address: 0808h
Condition	Slave No. 8

- **ASCII Mode**

Request from Modbus Master	':' 3038 3035 30383038 46463030 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3035 30383038 46463030 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3835 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 05 0808 FF00 (CRC)
ACK Reply from Modbus Slave	08 05 0808 FF00 (CRC)
NAK Reply from Modbus Slave	08 85 xx (CRC)

Function Code 06 (Preset Single Register)

Function code 06 changes word device data of D (data register).

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	New Data
xxh	06h	xxxxh	xxxxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Address	Acknowledge Data
xxh	06h	xxxxh	xxxxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	86h	xxh

Communication Example

Purpose	Write 8000 to data register D1708. D1708 → (1708 – 0) + 400001 = 401709 Modbus address: 401709 Extract lower 5 digits → 1709 1709 – 1 = 1708 = 6ACh Communication frame address: 06ACh
Condition	Slave No. 8

- **ASCII Mode**

Request from Modbus Master	':' 3038 3036 30364143 31463430 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3036 30364143 31463430 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3836 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 06 06AC 1F40 (CRC)
ACK Reply from Modbus Slave	08 06 06AC 1F40 (CRC)
NAK Reply from Modbus Slave	08 86 xx (CRC)

Function Code 15 (Force Multiple Coils)

Function code 15 changes bit device statuses of Q (output), R (shift register), or M (internal relay). One through 128 consecutive bits can be changed.

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	No. of Bits	Quantity of Data	First 8 Bits	Second 8 Bits		Last 8 Bits
xxh	0Fh	xxxxh	xxxxh	xxh	xxh	xxh		xxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Address	No. of Bits
xxh	0Fh	xxxxh	xxxxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	8Fh	xxh

Communication Example

Purpose	Write the following bit statuses to internal relays M605 through M624. M605 (ON), M606 (0N), M607 (OFF) M610 (ON), M611 (OFF), M612 (ON), M613 (ON), M614 (OFF), M615 (OFF), M616 (0N), M617 (OFF) M620 (OFF), M621 (OFF), M622 (OFF), M623 (OFF), M624 (OFF) M605 (LSB) through M614 (MSB) binary data: 6B M615 (LSB) through M624 (MSB) binary data: 02 M605 → (60 – 0) × 8 + 5 + 1001 = 1486 Modbus address: 1486 1486 – 1 = 1485 = 5CDh Communication frame address: 05CDh
Condition	Slave No. 8

- **ASCII Mode**

Request from Modbus Master	':' 3038 3046 30354344 30303130 3032 3642 3032 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3046 30354344 30303130 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3846 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 0F 05CD 0010 02 6B 02 (CRC)
ACK Reply from Modbus Slave	08 0F 05CD 0010 (CRC)
NAK Reply from Modbus Slave	08 8F xx (CRC)

Function Code 16 (Preset Multiple Registers)

Function code 16 changes word device data of D (data register). One through 64 consecutive words can be changed.

Communication Frame

Request from Modbus Master

Slave No.	Function Code	Address	No. of Words	Quantity of Data	First High Byte	First Low Byte		Last Low Byte
xxh	10h	xxxxh	xxxxh	xxh	xxh	xxh		xxh

ACK Reply from Modbus Slave

Slave No.	Function Code	Address	No. of Words
xxh	10h	xxxxh	xxxxh

NAK Reply from Modbus Slave

Slave No.	Function Code	Error Code
xxh	90h	xxh

Communication Example

Purpose	Write the following data to four data registers D1708 through D1711. D1708 (1234h) D1709 (5678h) D1710 (ABCDh) D1711 (EF01h) D1708 → (1708 – 0) + 400001 = 401709 Modbus address: 401709 Extract lower 5 digits → 1709 1709 – 1 = 1708 = 6ACh Communication frame address: 06ACh
Condition	Slave No. 8

- **ASCII Mode**

Request from Modbus Master	':' 3038 3130 30364143 30303034 3038 3132 3334 3536 3738 4142 4344 4546 3031 (LRC) CRLF
ACK Reply from Modbus Slave	':' 3038 3130 30364143 30303034 (LRC) CRLF
NAK Reply from Modbus Slave	':' 3038 3930 xxxx (LRC) CRLF

- **RTU Mode**

Request from Modbus Master	08 10 06AC 0004 08 12 34 56 78 AB CD EF 01 (CRC)
ACK Reply from Modbus Slave	08 10 06AC 0004 (CRC)
NAK Reply from Modbus Slave	08 90 xx (CRC)

13: TROUBLESHOOTING

Introduction

This chapter describes the procedures to determine the cause of trouble and actions to be taken when any trouble occurs while operating the MicroSmart.

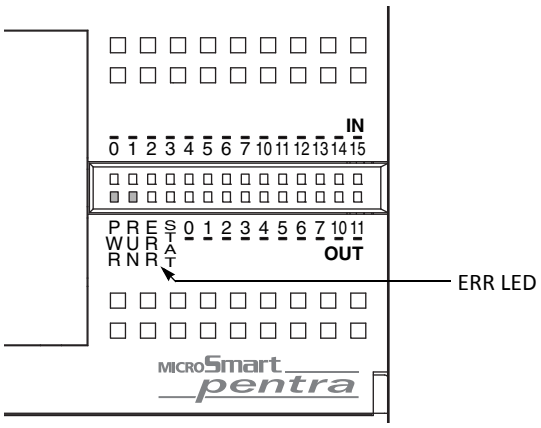
The MicroSmart has self-diagnostic functions to prevent the spread of troubles if any trouble should occur. In case of any trouble, follow the troubleshooting procedures to determine the cause and to correct the error.

Errors are checked in various stages. While editing a user program on WindLDR, incorrect devices and other data are rejected. User program syntax errors are found during compilation on WindLDR. When an incorrect program is downloaded to the MicroSmart, user program syntax errors are still checked. Errors are also checked at starting and during operation of the MicroSmart. When an error occurs, the error is reported by turning on the ERR LED on the MicroSmart and an error message can be viewed on WindLDR. Error codes can also be read on the HMI module.

ERR LED

The MicroSmart CPU module has an error indicator ERR. When an error occurs in the MicroSmart CPU module, the ERR LED is lit. See the trouble shooting diagrams on page 13-11.

For error causes to turn on the ERR LED, see page 13-4.



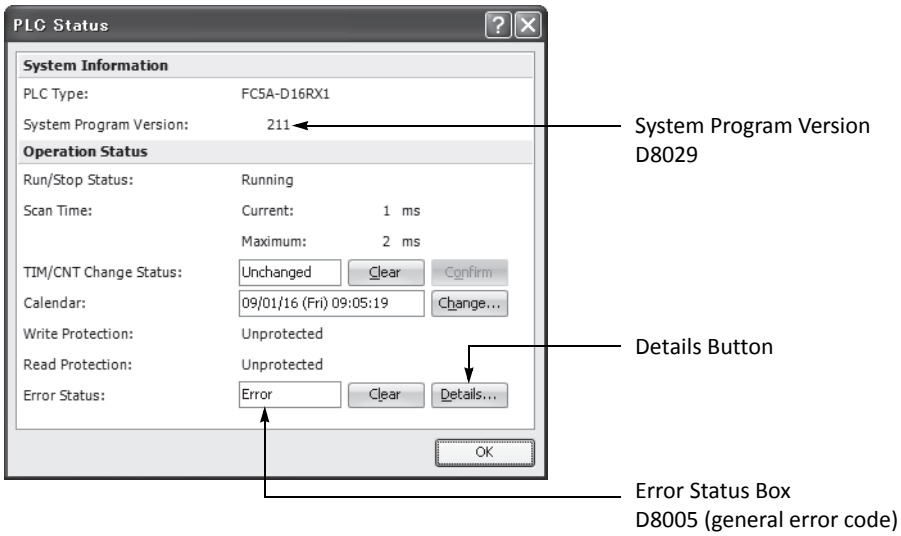
Reading Error Data

When any error occurs during the MicroSmart operation, “Error” is indicated and error details can be read using WindLDR on a computer.

Monitoring WindLDR

1. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**. The monitor mode is enabled.
2. From the WindLDR menu bar, select **Online** > **Status**. The PLC Status dialog box appears.

When any error exists, “Error” is displayed in the error status box.



3. On the right of the Error Status in the PLC Status dialog box, click the **Details** button.

The PLC Error Status screen appears.

Clearing Error Codes from WindLDR

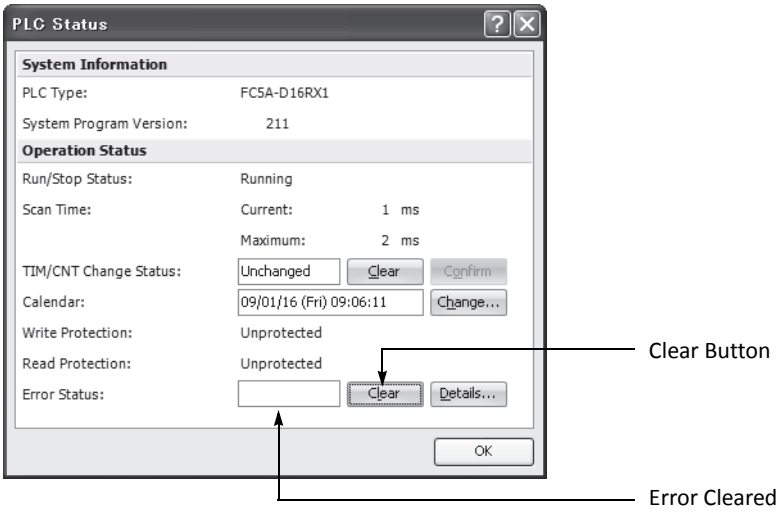
After removing the cause of the error, clear the error code using the following procedure:

1. From the WindLDR menu bar, select **Online** > **Monitor** > **Monitor**. The monitor mode is enabled.

2. From the WindLDR menu bar, select **Online** > **Status**. The PLC Status dialog box appears.

3. On the right of the **Error Status** in the PLC Status dialog box, click the **Clear** button.

This procedure clears the error code from special data register D8005 (general error code), and the error is cleared from the PLC Status dialog box.

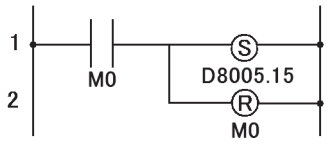


Special Data Registers for Error Information

Two data registers are assigned to store information on errors.

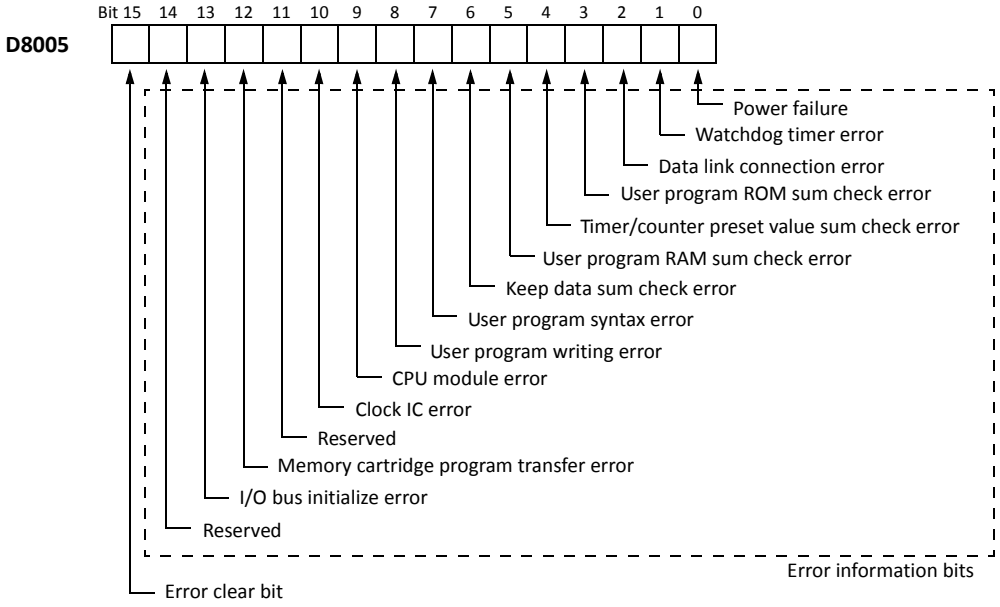
D8005	General Error Code
D8006	User Program Execution Error Code

Example: This ladder program clears the error information using the error clear bit of special data register D8005.



General Error Codes

The error code is stored in special data register D8005.
If '1' is stored in each bit of D8005, the corresponding error is occurring.



CPU Module Operating Status, Output, and ERR LED during Errors

Error Items	Operating Status	Output	ERR LED	Checked at
Power failure	Stop	OFF	OFF	Any time
Watchdog timer error	Stop	OFF	ON	Any time
Data link connection error	Stop	OFF	OFF	Initializing data link
User program ROM sum check error	Stop	OFF	ON	Starting operation
TIM/CNT preset value sum check error	Maintained	Maintained	OFF	Starting operation
User program RAM sum check error	Stop *1	OFF	ON	During operation
Keep data error	Maintained/ Stop *2	Maintained/ OFF *2	OFF	Turning power on
User program syntax error	Stop	OFF	ON	Downloading user program
User program writing error	Stop	OFF	ON	Downloading user program
CPU module error	Stop	OFF	ON	Turning power on
Clock IC error	Maintained	Maintained	ON	Any time
Memory cartridge program transfer error *3	Stop	OFF	ON	Turning power on
I/O bus initialize error	Stop	OFF	ON	Turning power on
User program execution error	Maintained	Maintained	ON	Executing user program

*1: When a program RAM sum check error occurs, operation is stopped momentarily for reloading the user program. After completing the reloading, operation resumes.

*2: Operation starts to run and outputs are turned on or off according to the user program as default, but it is also possible to stop operation and turn off outputs using the Function Area Settings on WindLDR. See page 5-3.

*3: Memory cartridge program transfer error bit is available on FC5A-D12K1E and FC5A-D12S1E only.

Error Causes and Actions

0001h: Power Failure

This error indicates when the power supply is lower than the specified voltage. This error is also recorded when the power is turned off. Clear the error code using the HMI module or WindLDR on a computer.

0002h: Watchdog Timer Error

The watchdog timer monitors the time required for one program cycle (scan time). When the time exceeds approximately 340 ms, the watchdog timer indicates an error. Clear the error code using the HMI module or WindLDR on a computer. If this error occurs frequently, the MicroSmart CPU module has to be replaced.

0004h: Data Link Connection Error

This error indicates that the Function Area Settings for data link communication are incorrect or the cable is not connected correctly. Make sure that slave stations are set to station numbers 1 through 31 using WindLDR. No duplication of station numbers is allowed. See page 11-8.

To correct this error, make corrections in the Function Area Settings and download the user program to each station, or connect the cable correctly. Turn power off and on again for the slave station. Then take one of the following actions:

- Turn power off and on for the master station.
- Initialize data link communication for the master station using WindLDR on a computer. See page 11-12.
- Turn on special internal relay M8007 (data link communication initialize flag) at the master station. See page 11-7.

0008h: User Program ROM Sum Check Error

The user program stored in the MicroSmart CPU module EEPROM is broken. Download a correct user program to the MicroSmart, and clear the error code using the HMI module or WindLDR on a computer.

When a memory cartridge is installed on the CPU module, the user program in the memory cartridge is checked.

0010h: Timer/Counter Preset Value Sum Check Error

The execution data of timer/counter preset values is broken. The timer/counter preset values are initialized to the values of the user program automatically. Note that changed preset values are cleared and that the original values are restored. Clear the error code using the HMI module or WindLDR on a computer.

0020h: User Program RAM Sum Check Error

The data of the user program compile area in the MicroSmart CPU module RAM is broken.When this error occurs, the user program is recompiled automatically, and the timer/counter preset values and expansion data register preset values are initialized to the values of the user program. Note that changed preset values are cleared and that the original values are restored. Clear the error code using the HMI module or WindLDR on a computer.

0040h: Keep Data Sum Check Error

This error indicates that the data designated to be maintained during power failure is broken because of memory backup failure. Note that the "keep" data of internal relays and shift registers are cleared. Data of counters and data registers are also cleared. Clear the error code using the HMI module or WindLDR on a computer.

If this error occurs in a short period of power interruption after the battery has been charged as specified, the battery is defective and the CPU module has to be replaced.

0080h: User Program Syntax Error

This error indicates that the user program has a syntax error. Correct the user program, and download the corrected user program to the MicroSmart. The error code is cleared when a correct user program is transferred.

0100h: User Program Writing Error

This error indicates a failure of writing into the MicroSmart CPU module ROM when downloading a user program. The error code is cleared when writing into the EEPROM is completed successfully. If this error occurs frequently, the MicroSmart CPU module has to be replaced.

When a memory cartridge is installed on the CPU module, writing into the memory cartridge is checked.

0200h: CPU Module Error

This error is issued when the ROM is not found. When this error occurred, turn power off and on. Clear the error code using the HMI module or WindLDR on a computer. If this error occurs frequently, the MicroSmart CPU module has to be replaced.

0400h: Clock IC Error

This error indicates that the real time calendar/clock in the clock cartridge has lost clock backup data or has an error caused by invalid clock data.

Clear the error code and set the calendar/clock data using the HMI module or WindLDR on a computer. The clock cartridge will recover from the error. If the error continues, the clock cartridge has to be replaced. See Troubleshooting Diagram on page 13-18.

1000h: Memory Cartridge Program Transfer Error

This error indicates that the user program cannot be downloaded to/uploaded from CPU module using the memory cartridge. The memory cartridge program transfer fails when one of the following conditions is met:

- When the user program in the CPU module is password-protected and the password of the user program in the memory cartridge does not match. Configure the correct password to the user program in the memory cartridge. For details on entering the password, see page 2-93.
- When uploading the user program from the CPU module is prohibited. Upload cannot be executed.

2000h: I/O Bus Initialize Error

This error indicates that an I/O module has a fault. If this error occurs frequently or normal I/O function is not restored automatically, the I/O module has to be replaced.

User Program Execution Error

This error indicates that invalid data is found during execution of a user program. When this error occurs, the ERR LED and special internal relay M8004 (user program execution error) are also turned on. The detailed information of this error can be viewed from the error code stored in special data register D8006 (user program execution error code).

User Program Execution Error Code (D8006)	Error Details
1	Source/destination device is out of range
2	MUL result is out of data type range.
3	DIV result is out of data type range, or division by 0.
4	BCDLS has S1 or S1+1 exceeding 9999.
5	HTOB(W) has S1 exceeding 9999.
6	BTOH has any digit of S1 exceeding 9.
7	HTOA/ATOH/BTOA/ATOB has quantity of digits to convert out of range.
8	ATOH/ATOB has non-ASCII data for S1 through S1+4.
9	WKTIM has S1, S2, and S3 exceeding the valid range. S1: 0 through 127 S2/S3: Hour data 0 through 23, minute data 0 through 59 S2/S3 can be 10000. WKTBL instruction is not programmed or WKTIM instruction is executed before WKTBL instruction when 1 (additional days in the week table) or 2 (skip days in the week table) is set for MODE in the WKTIM instruction.
10	WKTBL has S1 through Sn out of range. Month: 01 through 12 Day: 01 through 31
11	DGRD data exceeds 65535 with BCD5 digits selected.
12	CVXTY/CVYTX is executed without matching XYFS. XYFS and CVXTY/CVYTX have the same S1, but have different data types.
13	CVXTY/CVYTX has S2 exceeding the value specified in XYFS.
14	Label in LJMP, LCAL, or DJNZ is not found.
15	TXD/RXD is executed while the RS232C port 1 or 2 is *not* set to user communication mode.
16	PID instruction execution error (see page 14-4 (Advanced.Vol.)).
17	Preset value is written to a timer/counter whose preset value is designated with a data register.
18	Attempt was made to execute an instruction that cannot be used in an interrupt program: SOTU, SOTD, TML, TIM, TMH, TMS, CNT, CDP, CUD, SFR, SFRN, WKTIM, WKTBL, DISP, DGRD, TXD, RXD, DI, EI, XYFS, CVXTY, CVYTX, PULS, PWM, RAMP, ZRN, PID, DTML, DTIM, DTMH, DTMS, TTIM, RUNA, and STPA (see page 5-35).
19	Attempt was made to execute an instruction that is not available for the PLC.
20	PULS, PWM, RAMP, or ZRN has an invalid value in control registers.
21	DECO has S1 exceeding 255.
22	BCNT has S2 exceeding 256.
23	ICMP>= has S1 < S3.
24	— Reserved —
25	BCDLS has S2 exceeding 7.
26	DI or EI is executed when interrupt input or timer interrupt is not programmed in the Function Area Settings.
27	Work area is broken when using DTML, DTIM, DTMH, DTMS, or TTIM.
28	S1 for trigonometric function instruction is invalid.

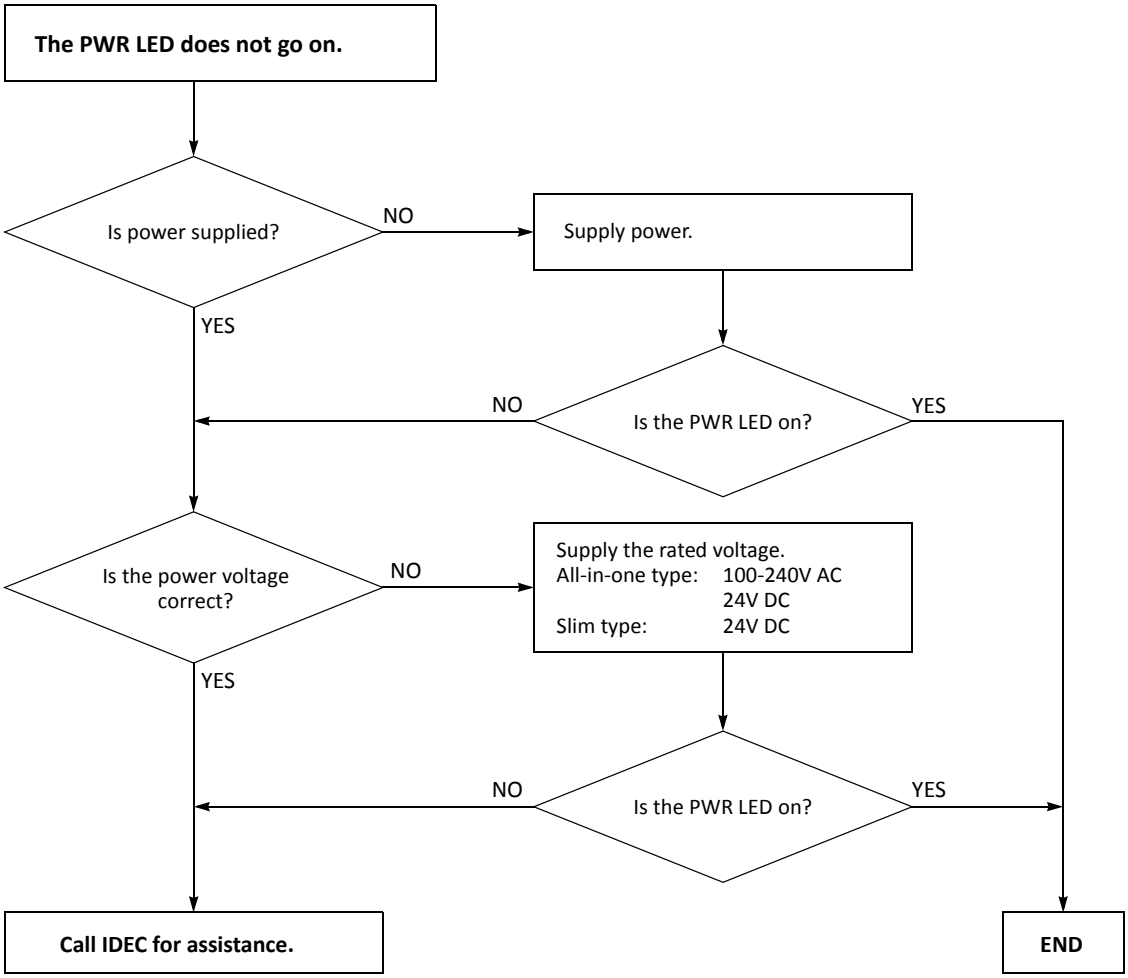
User Program Execution Error Code (D8006)	Error Details
29	Result of F (float) data type instruction is out of the data type range.
30	N_B for SFTL/SFTR is out of range.
31	FIEX instruction is executed before FIFOF instruction.
32	TADD, TSUB, HOUR, or HTOS has invalid data for source device S1.
33	In the RNDM instruction, S1 is larger than S2, or S1 or S2 data exceeds 32767.
34	NDSRC has invalid data for source device S3.
35	In the SUM instruction, the execution result exceeds the valid range for the selected data type, or S2 data is 0.

Troubleshooting Diagrams

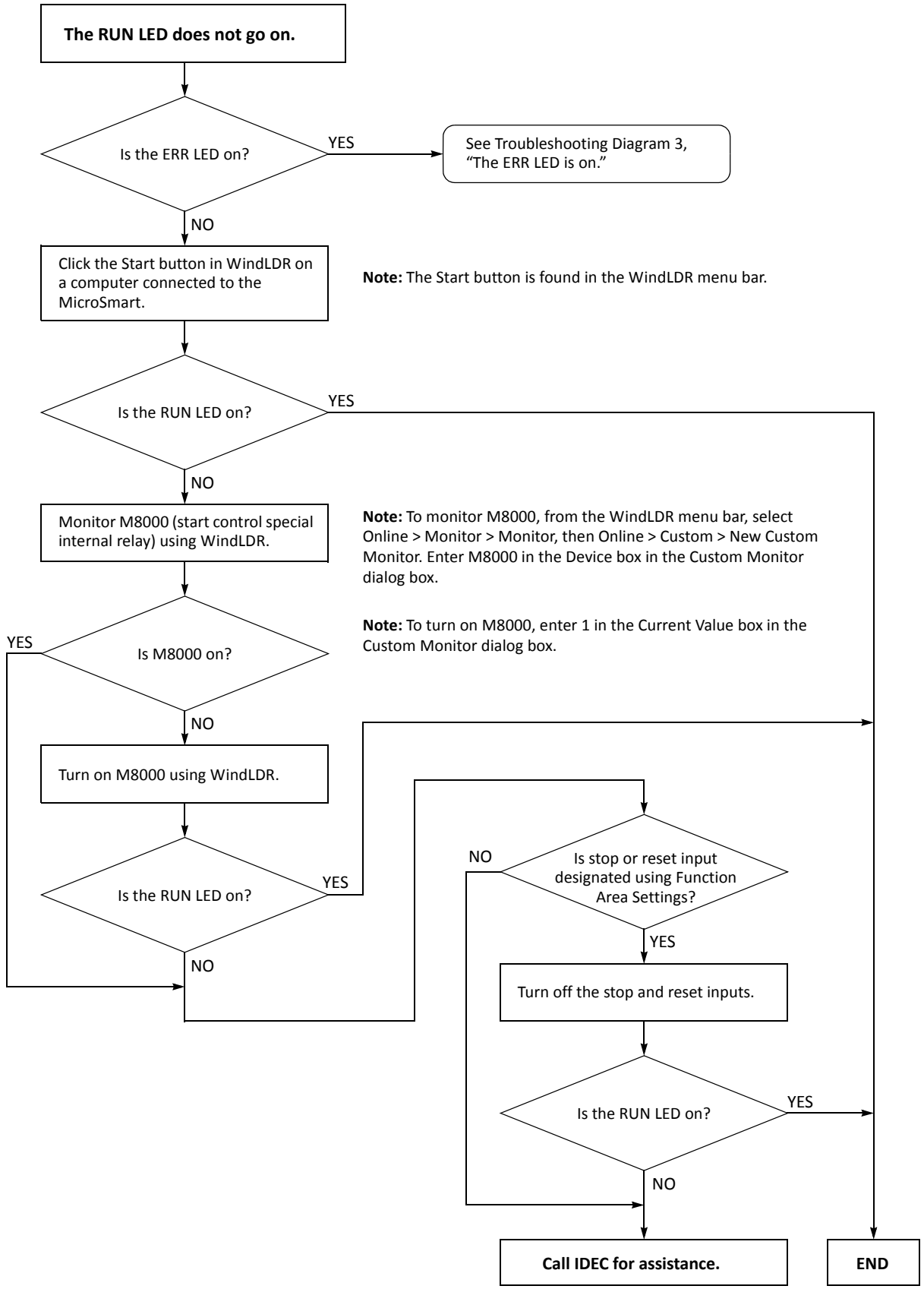
When one of the following problems is encountered, see the trouble shooting diagrams on the following pages.

Problem	Troubleshooting Diagram
The PWR LED does not go on.	Diagram 1
The RUN LED does not go on.	Diagram 2
The ERR LED is on.	Diagram 3
Input does not operate normally.	Diagram 4
Output does not operate normally.	Diagram 5
Communication between WindLDR on a computer and the MicroSmart is not possible.	Diagram 6
Cannot stop or reset operation.	Diagram 7
Watchdog timer error occurs and the CPU does not run.	Diagram 8
The interrupt/catch input cannot receive short pulses.	Diagram 9
Frequency measurement does not work.	Diagram 10
The calendar/clock does not operate correctly.	Diagram 11
Analog I/O module does not work (END refresh type).	Diagram 12
Data link communication is impossible.	Diagram 13
Data is not transmitted at all in the user communication mode.	Diagram 14
Data is not transmitted correctly in the user communication mode.	Diagram 15
Data is not received at all in the user communication mode.	Diagram 16
Data is not received correctly in the user communication mode.	Diagram 17
Modbus master communication does not work.	Diagram 18
WindLDR does not communicate with PLC via USB.	Diagram 19
Modbus master communication request is slow.	Diagram 20

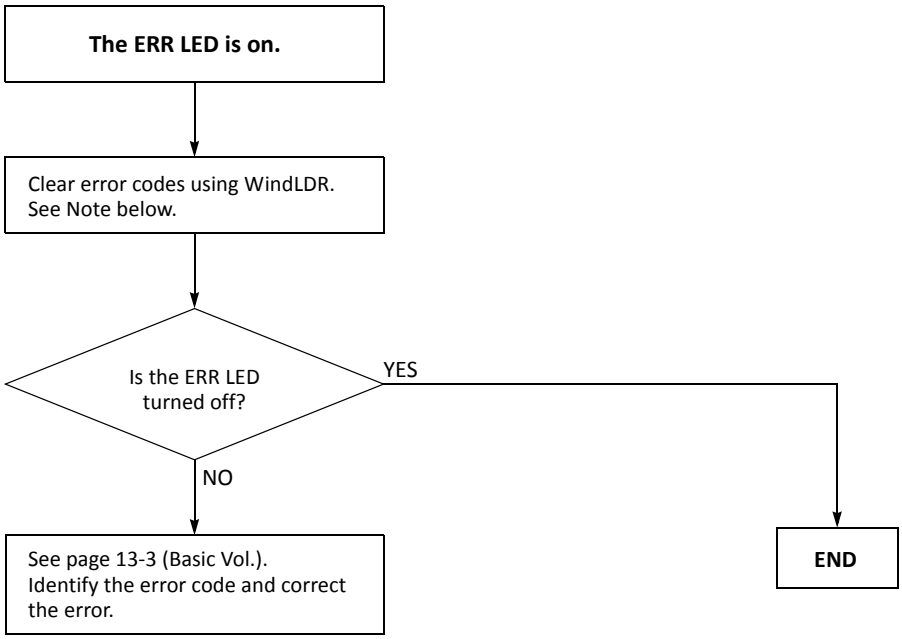
Troubleshooting Diagram 1



Troubleshooting Diagram 2

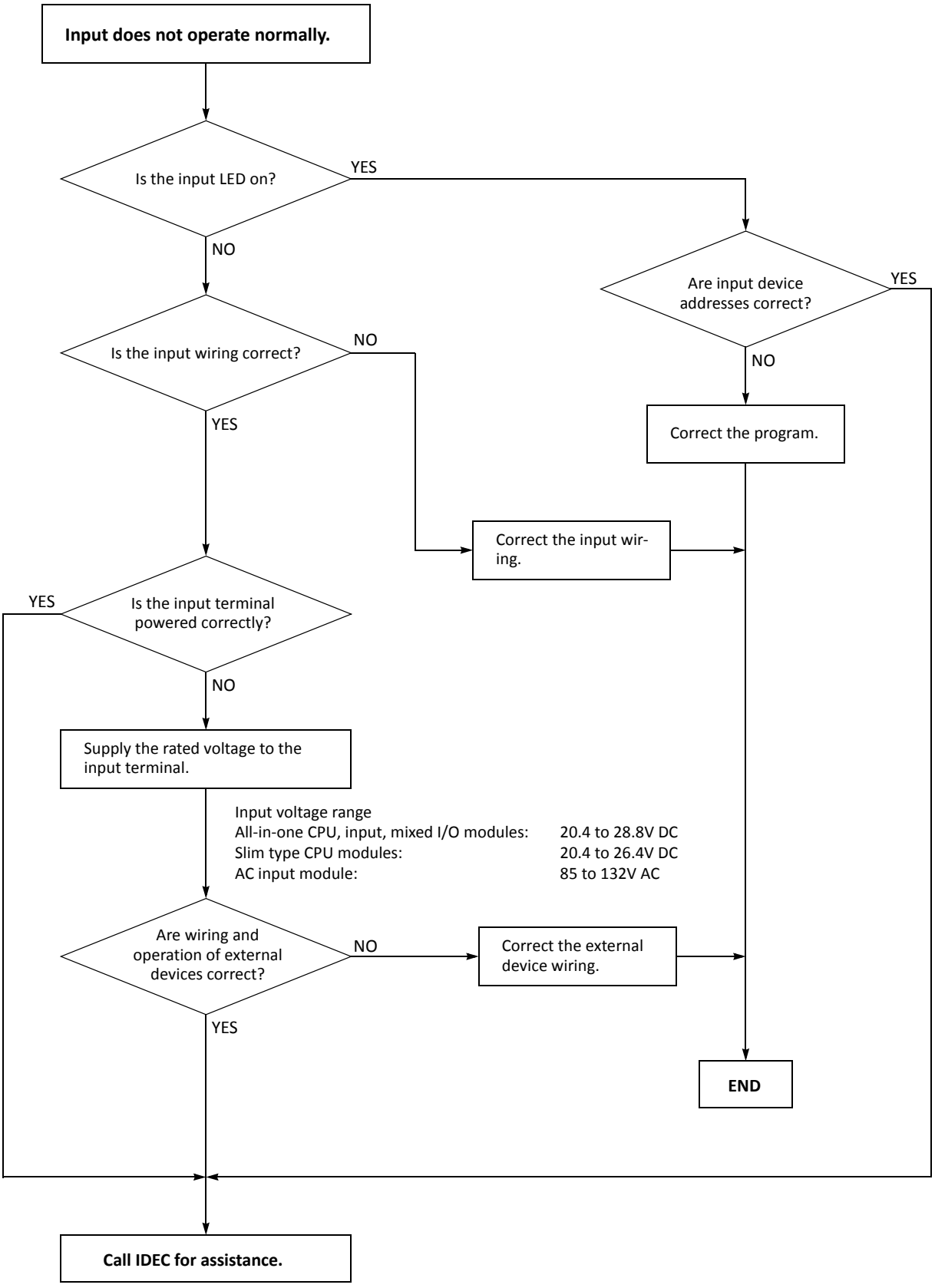


Troubleshooting Diagram 3

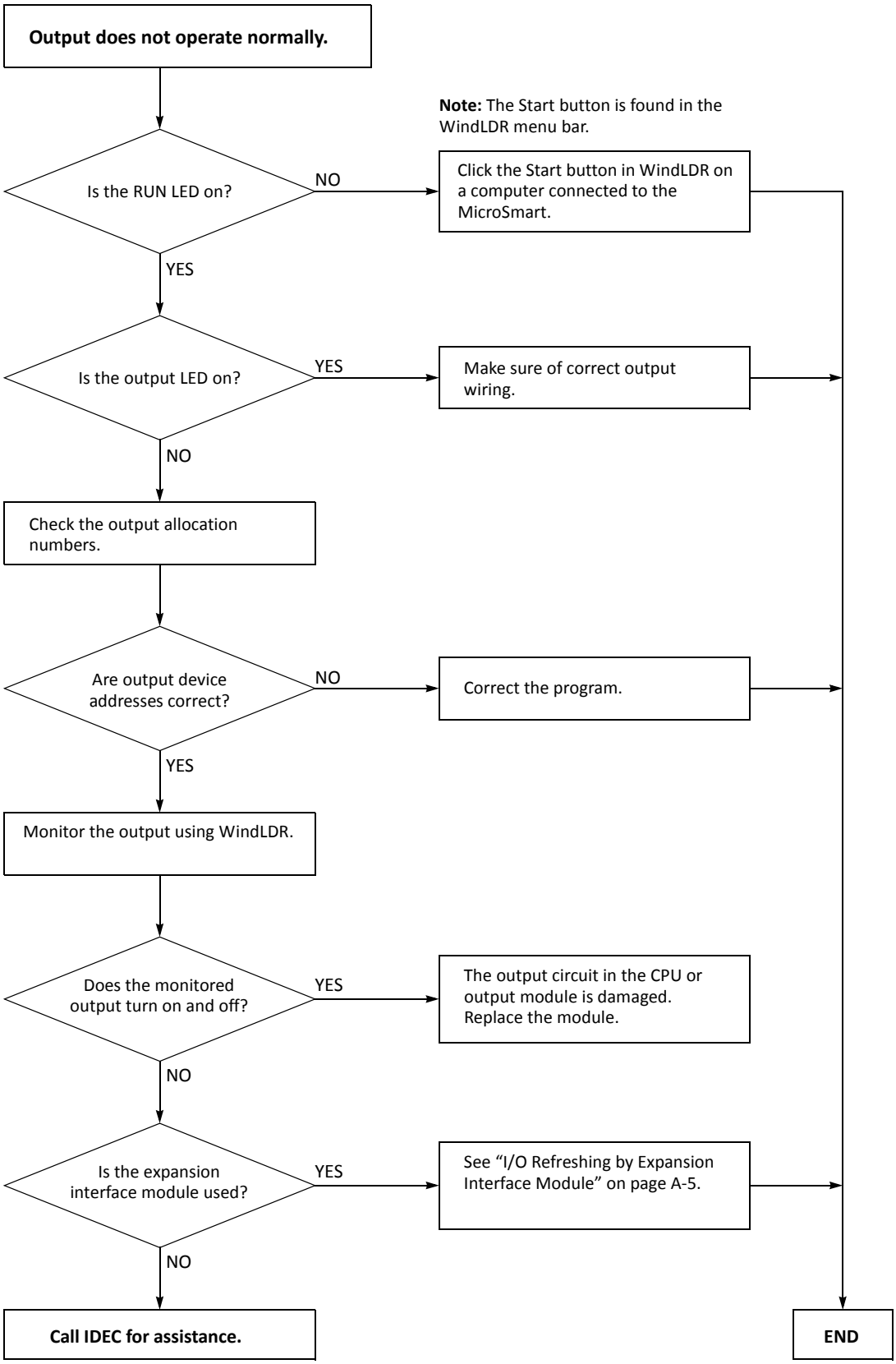


Note: Temporary errors can be cleared to restore normal operation by clearing error codes from WindLDR. See page 13-2.

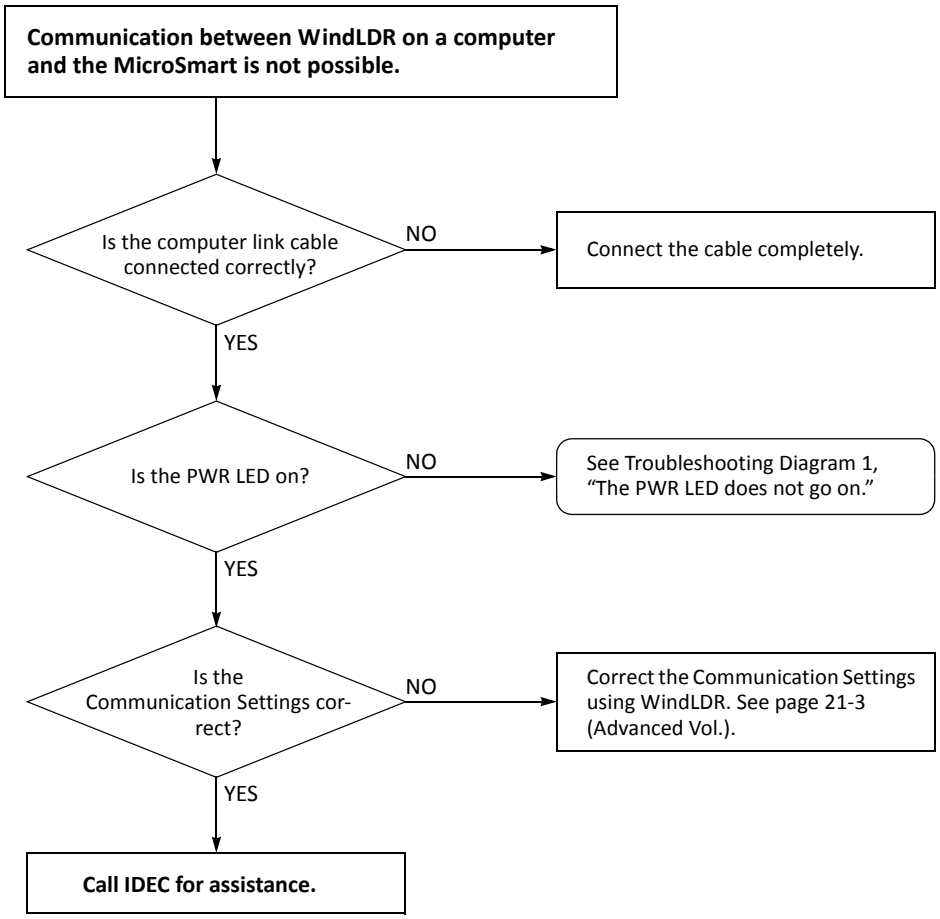
Troubleshooting Diagram 4



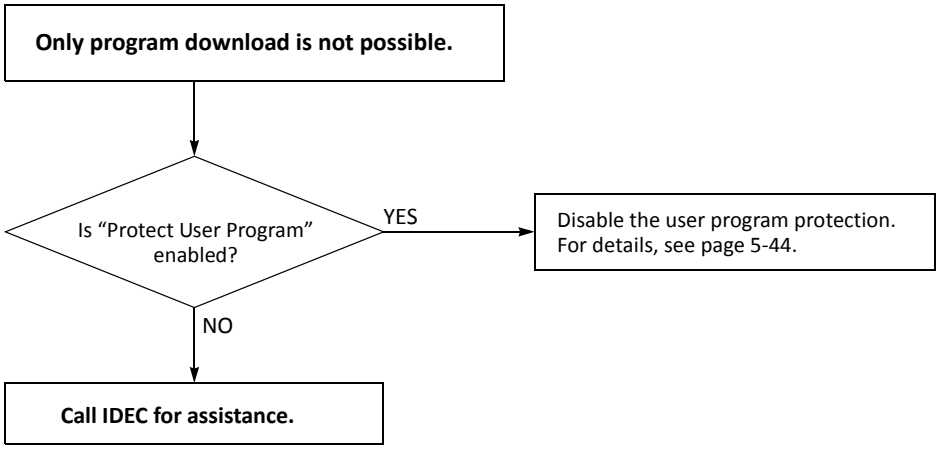
Troubleshooting Diagram 5



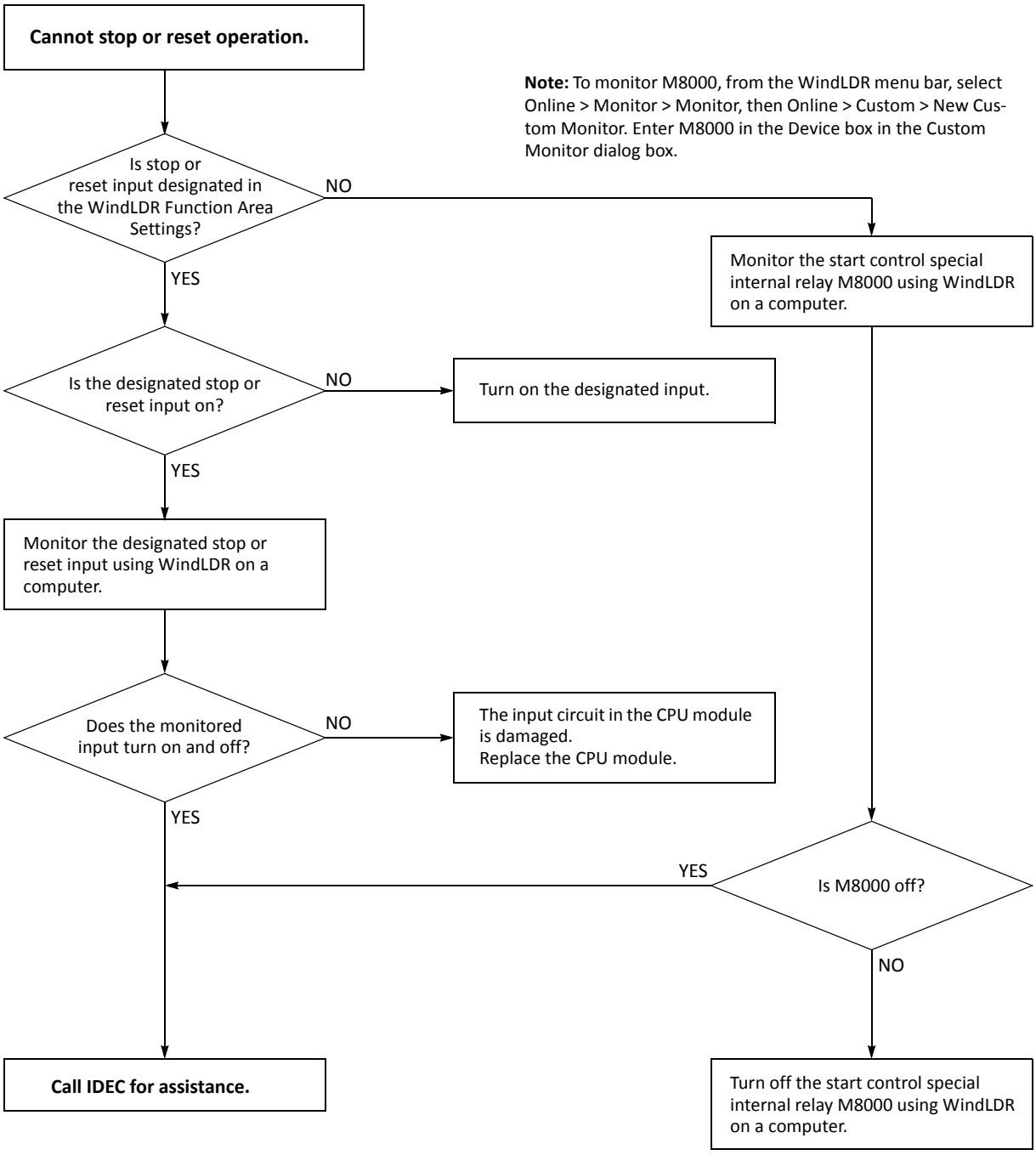
Troubleshooting Diagram 6



When only program download is not possible:



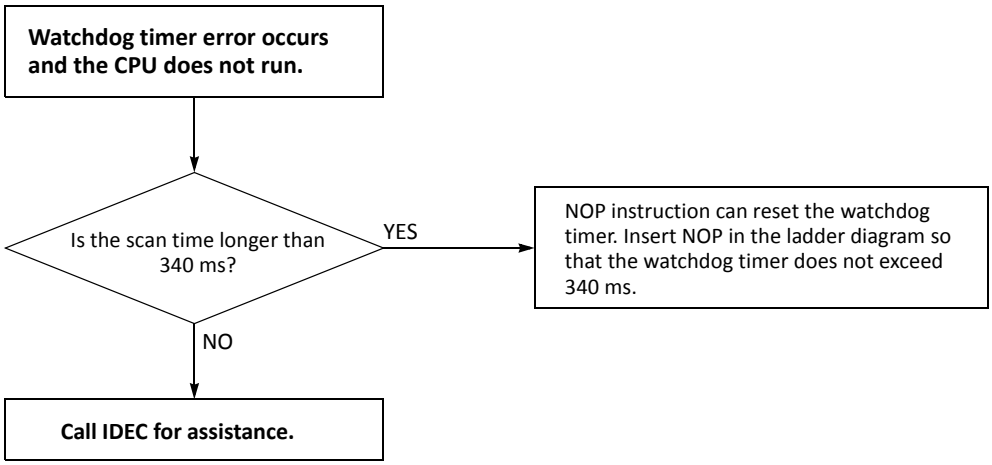
Troubleshooting Diagram 7



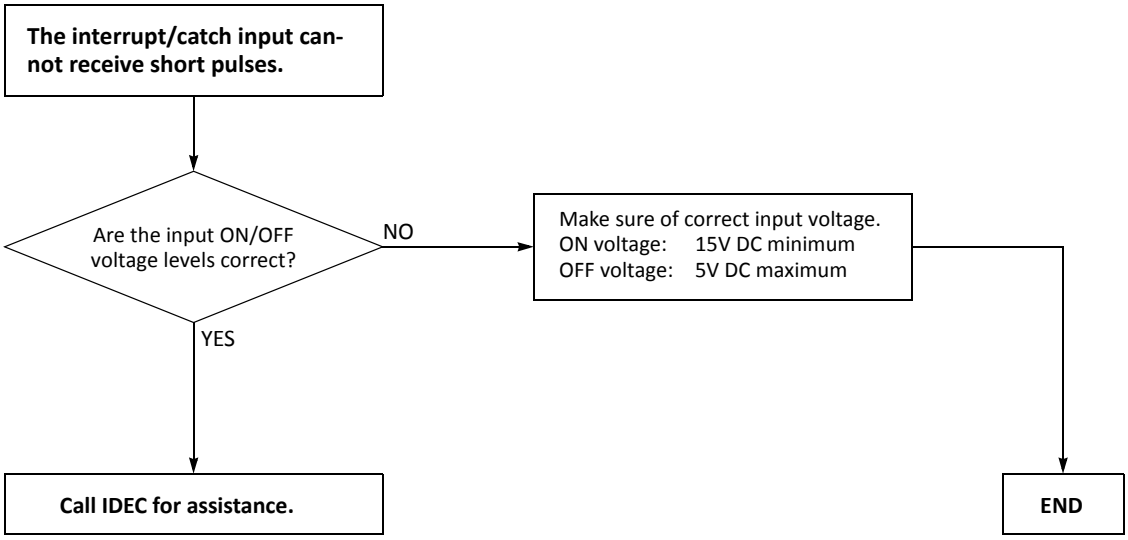
Note: To monitor M8000, from the WindLDR menu bar, select Online > Monitor > Monitor, then Online > Custom > New Custom Monitor. Enter M8000 in the Device box in the Custom Monitor dialog box.

Note: To turn off M8000, enter 0 in the Current Value box in the Custom Monitor dialog box.

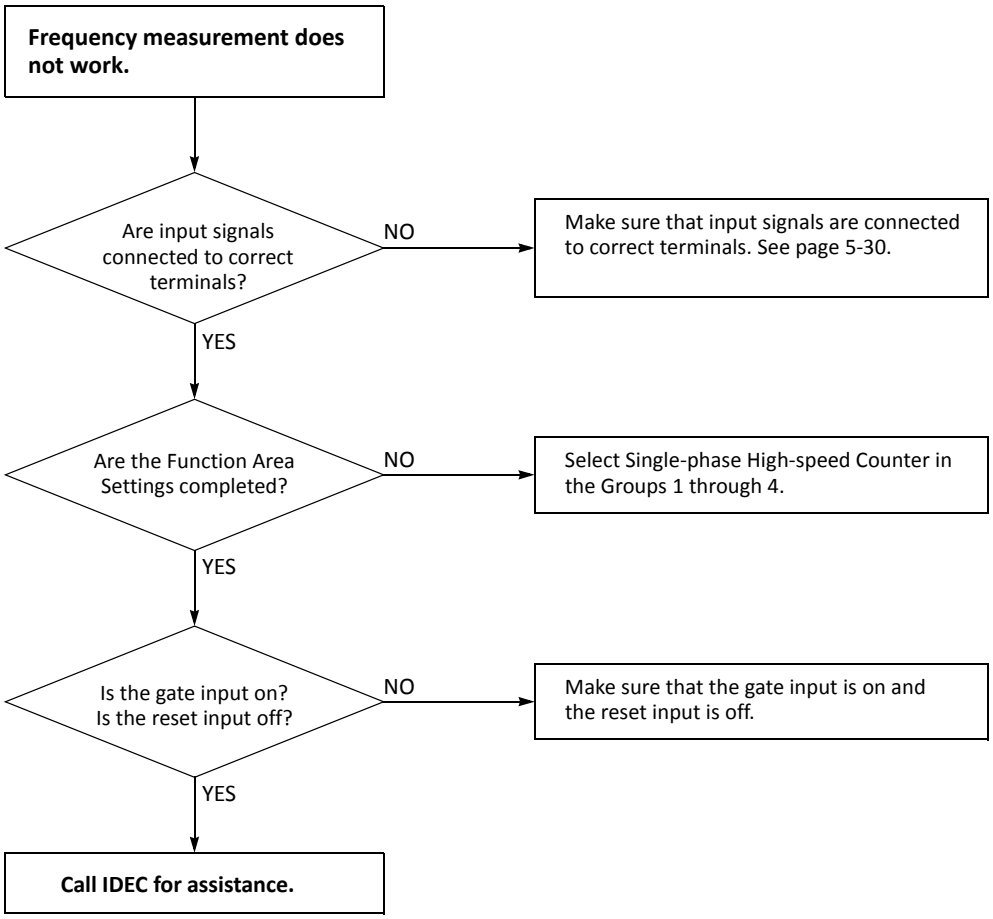
Troubleshooting Diagram 8



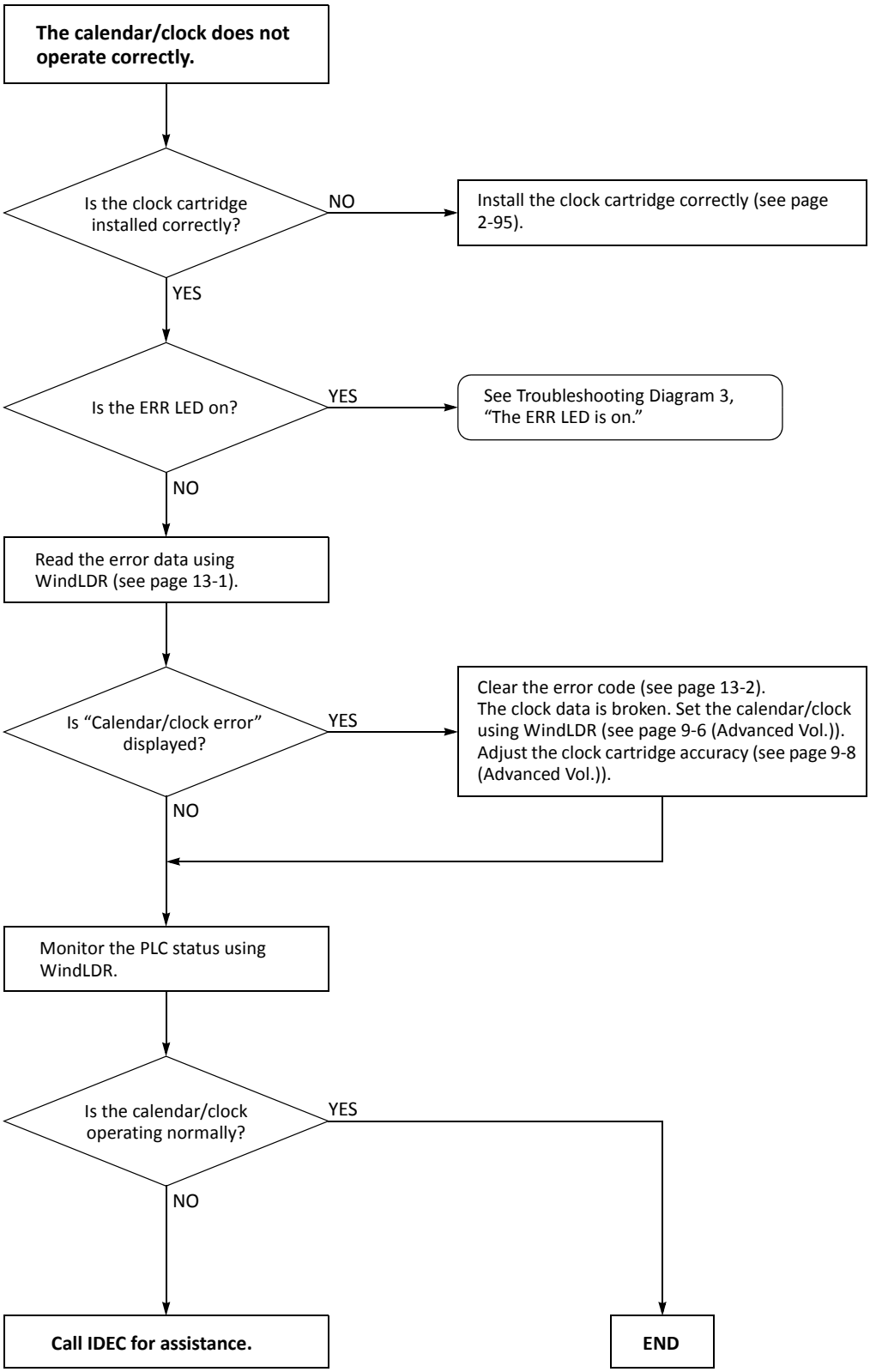
Troubleshooting Diagram 9



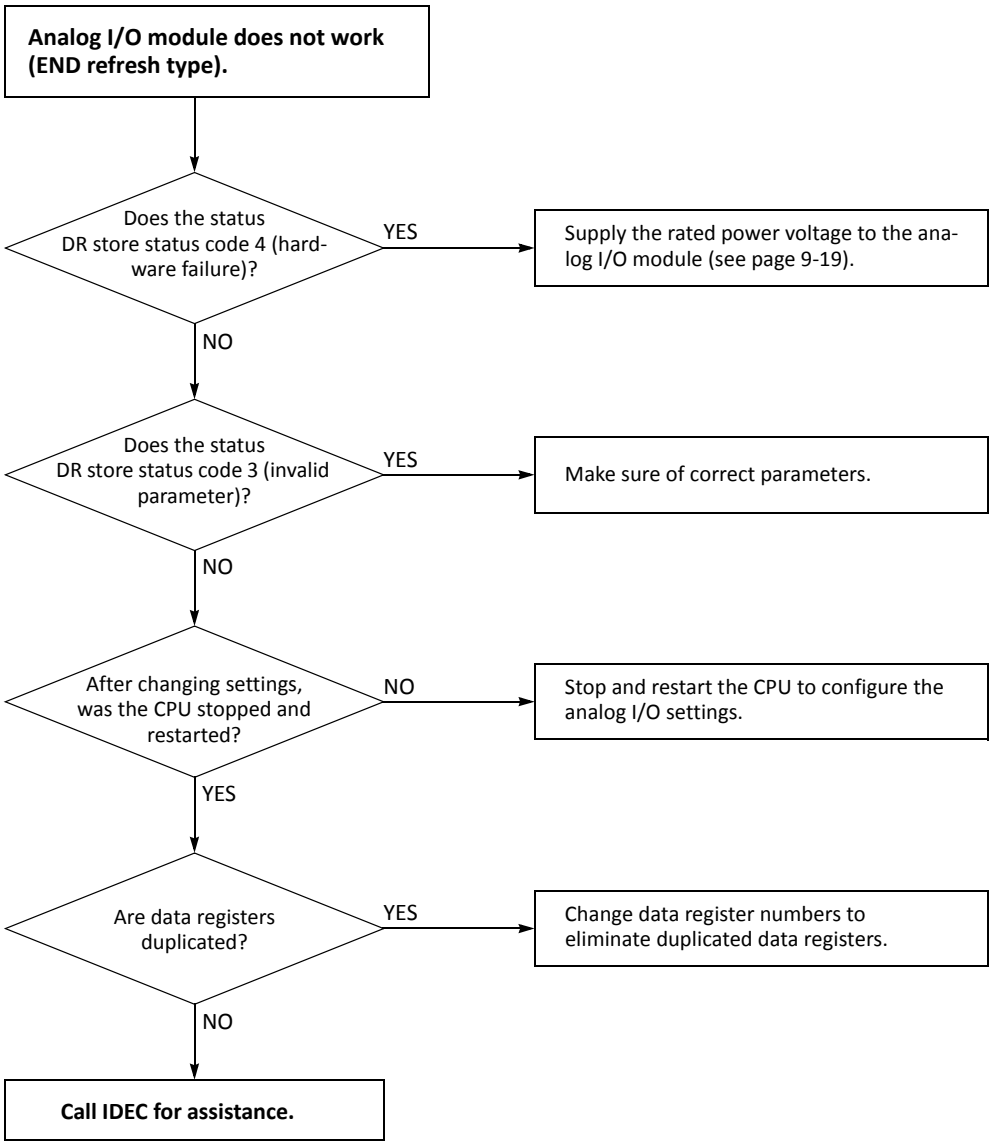
Troubleshooting Diagram 10



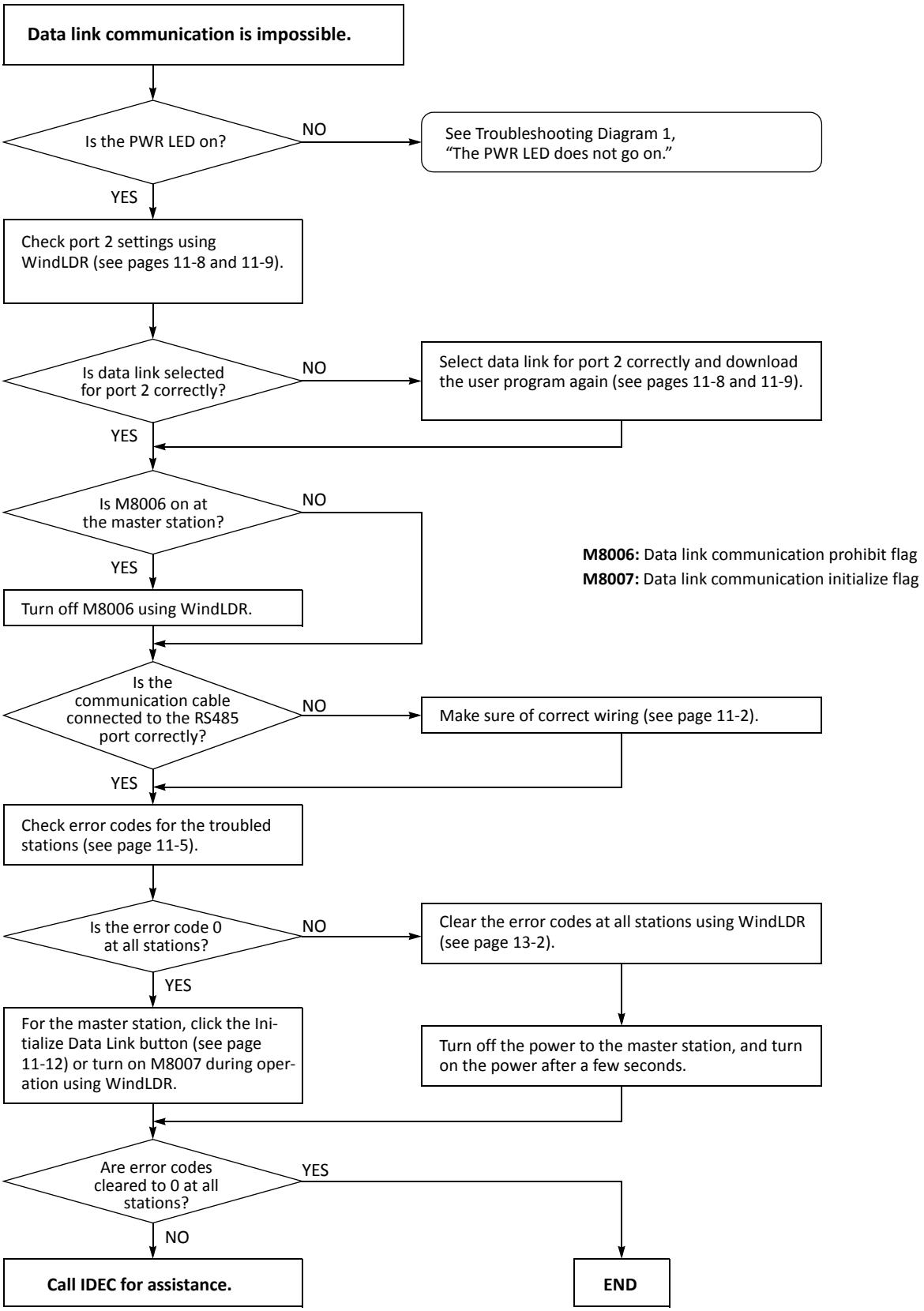
Troubleshooting Diagram 11



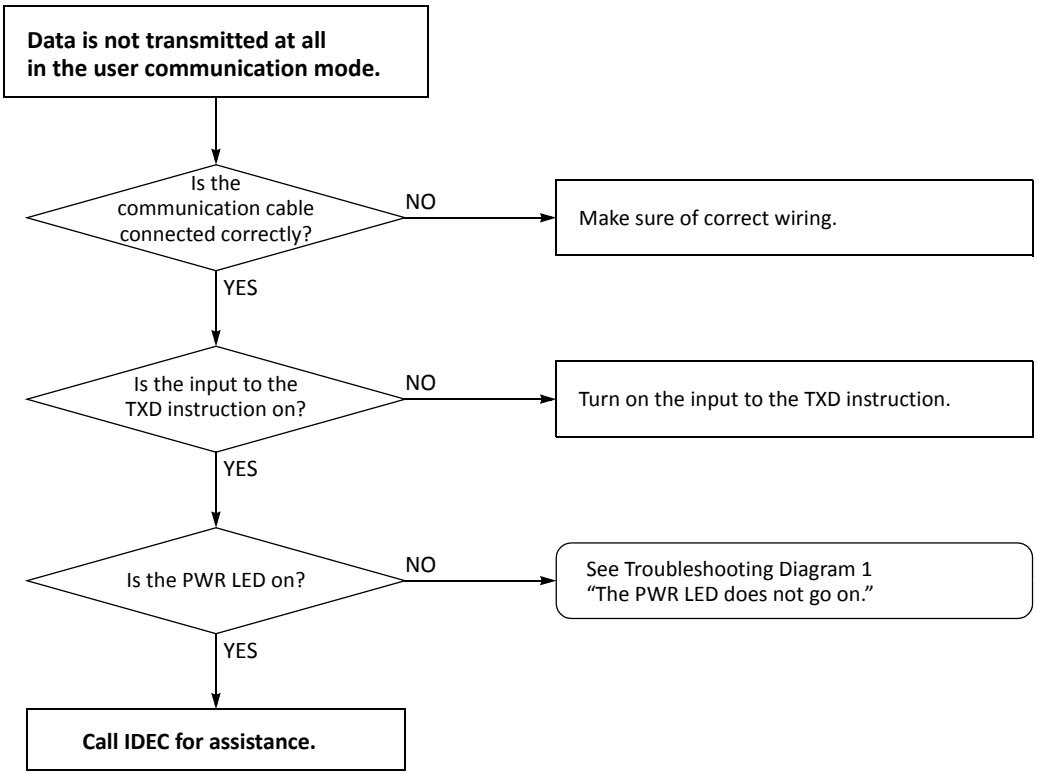
Troubleshooting Diagram 12



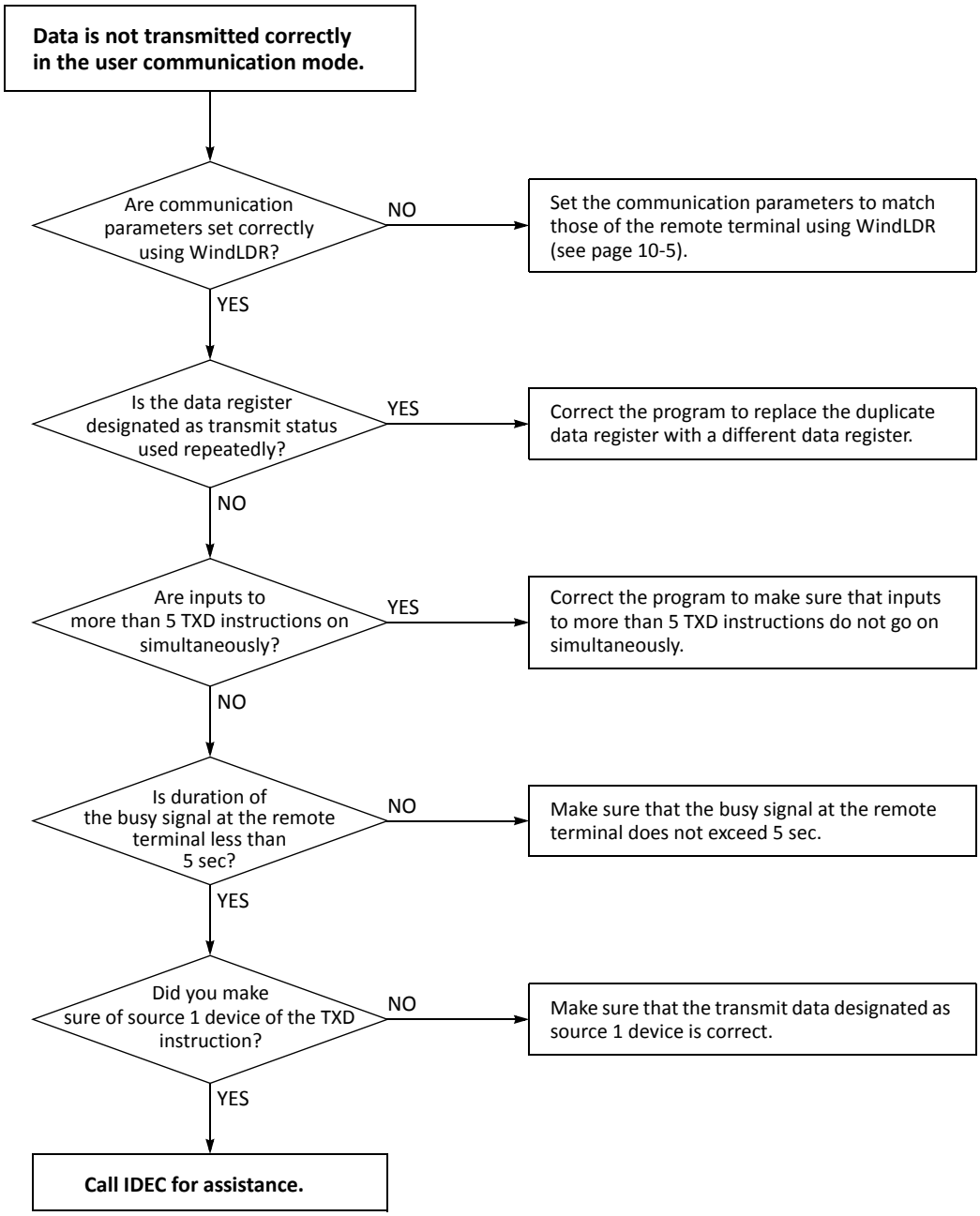
Troubleshooting Diagram 13



Troubleshooting Diagram 14

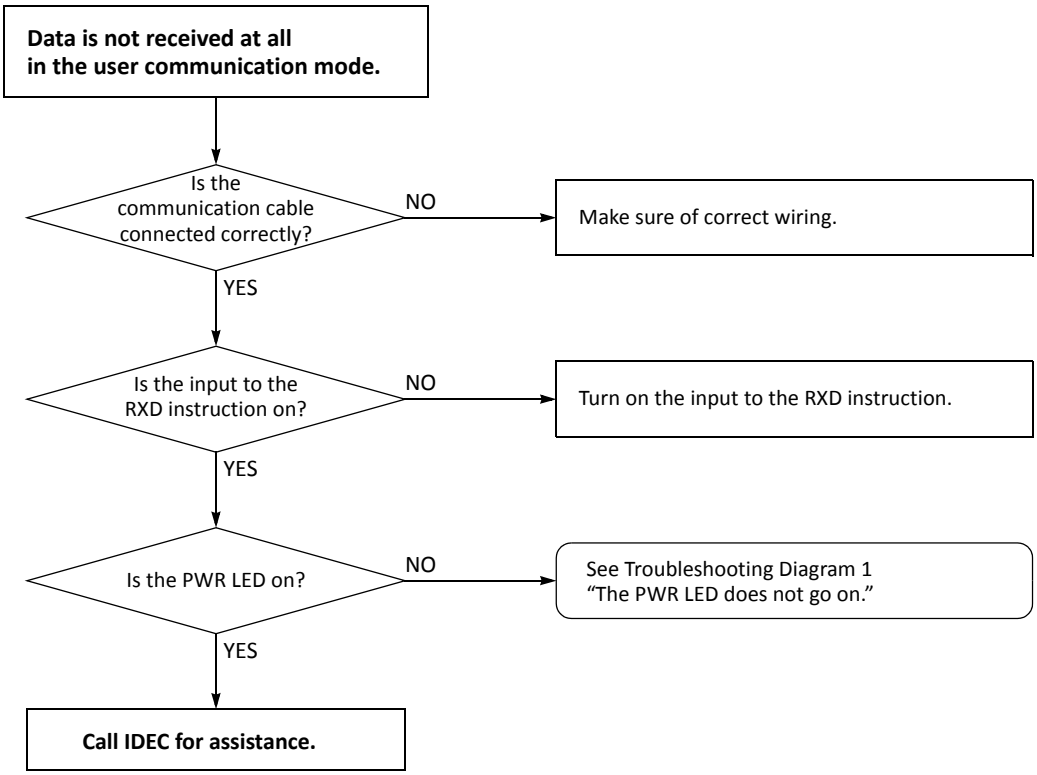


Troubleshooting Diagram 15

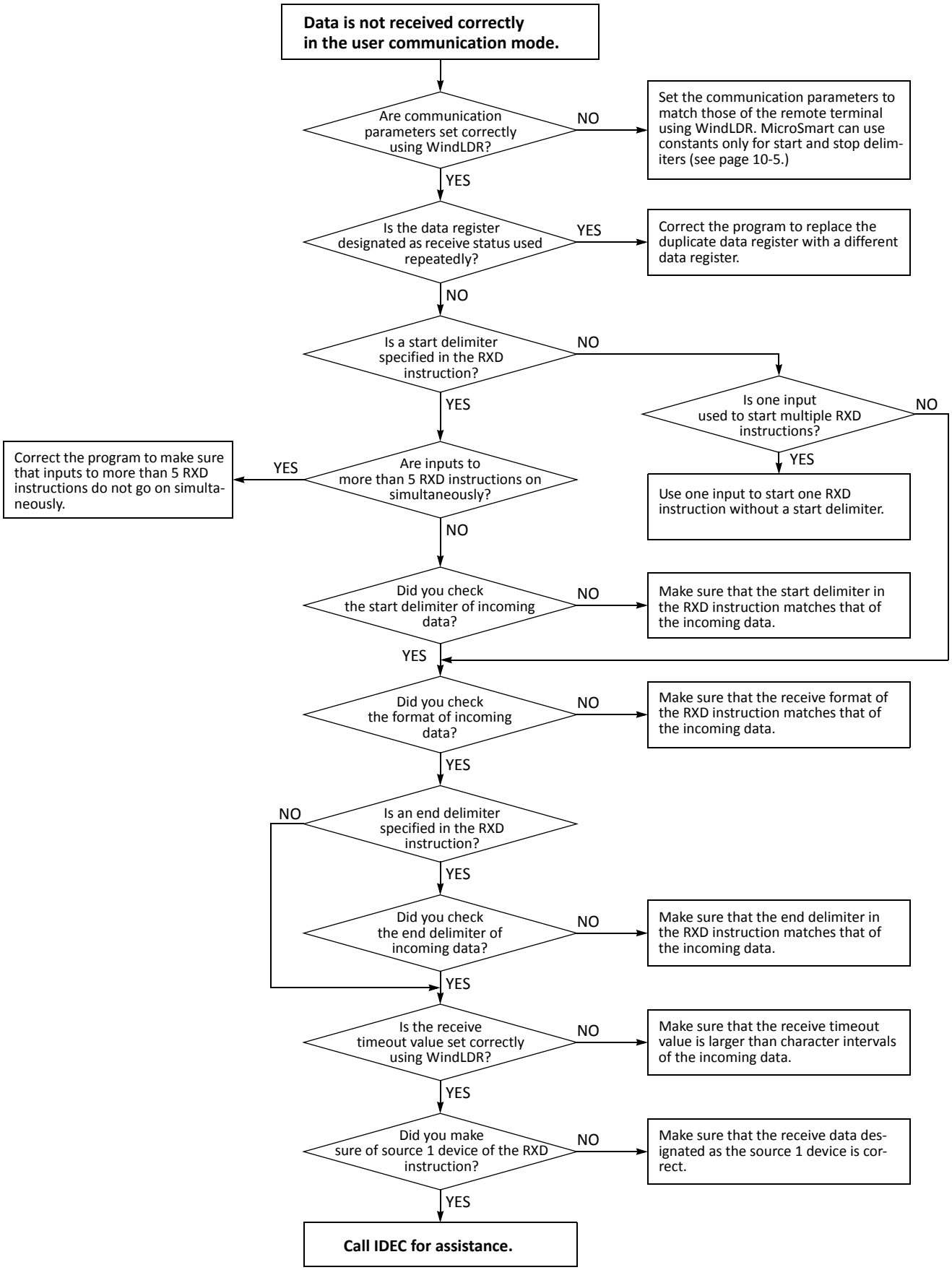


When the user communication still has a problem after completing the above procedure, also perform the procedure of Diagram 14 described on the preceding page.

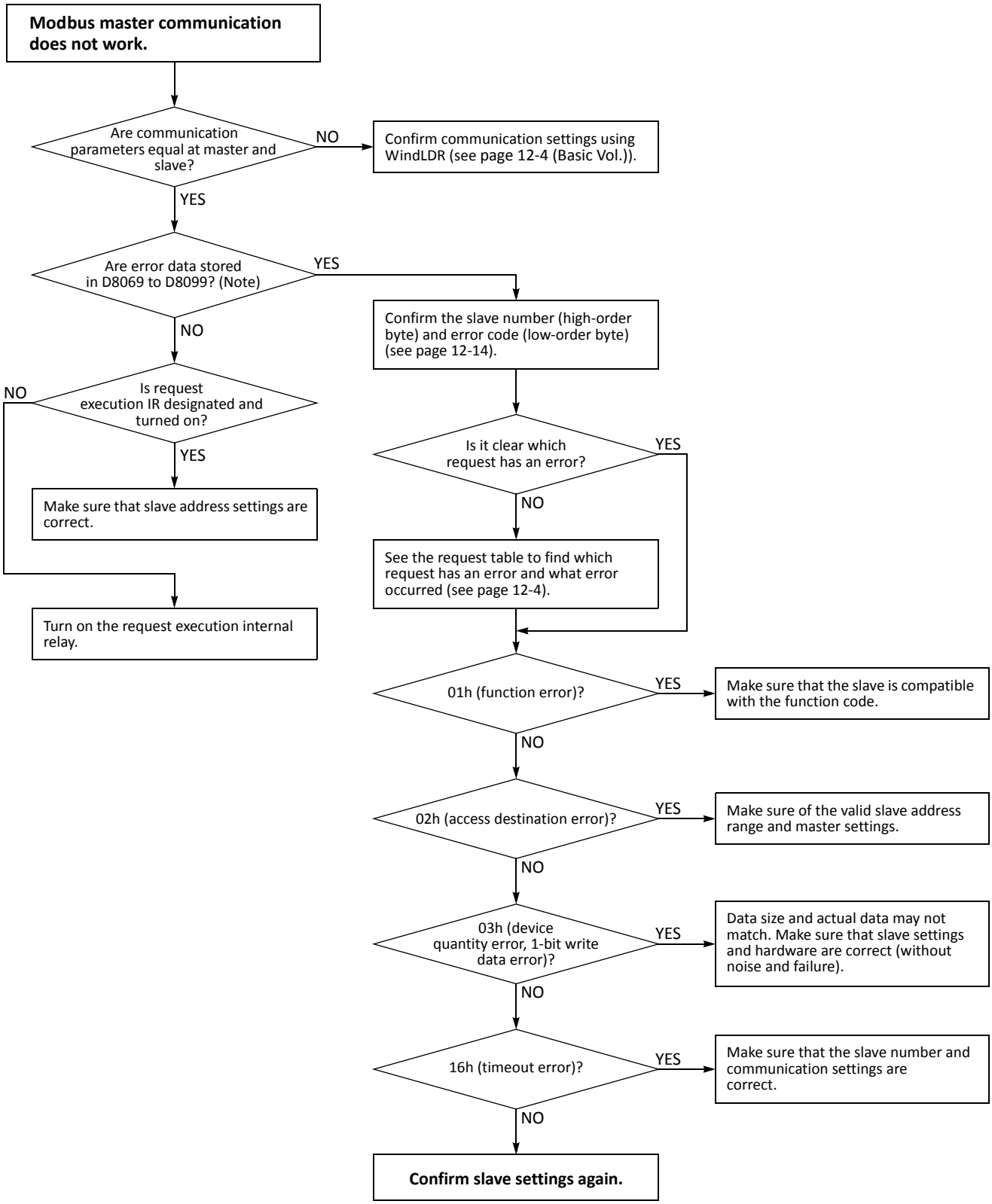
Troubleshooting Diagram 16



Troubleshooting Diagram 17

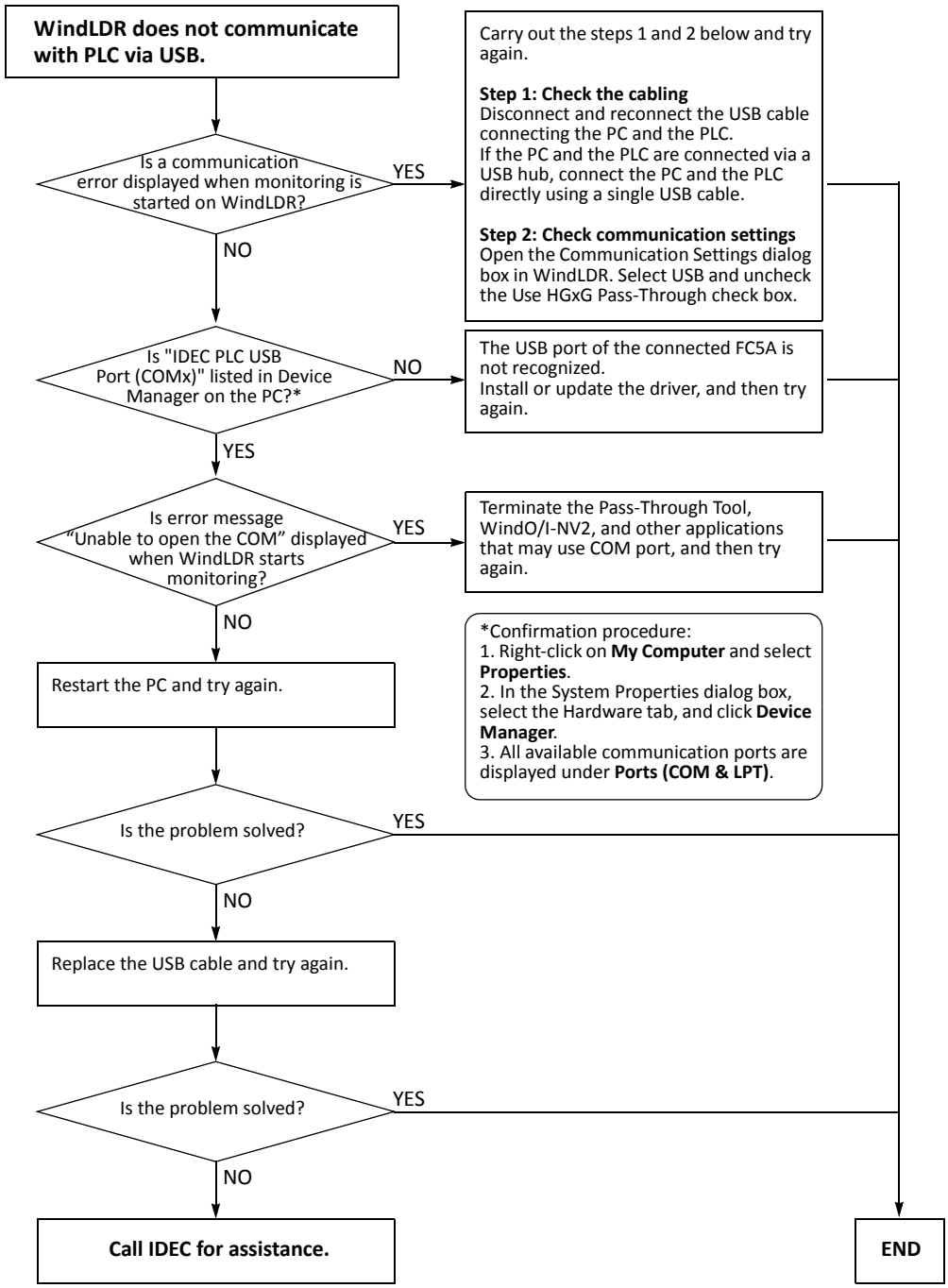


Troubleshooting Diagram 18

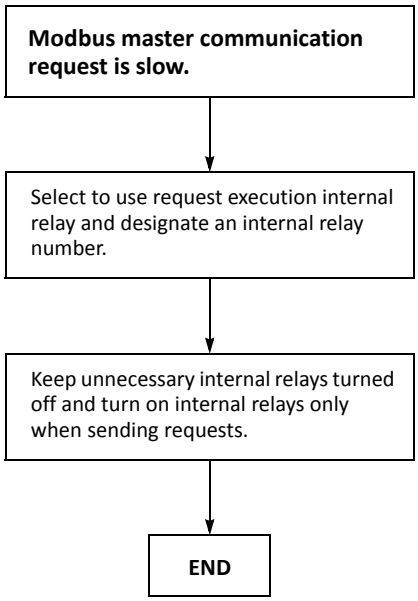


Note: Error data are stored in D8069 to D8099 when Modbus master is used with port 2. For port 3 through port 7, data registers in which error data are stored are specified in the Function Area Settings.

Troubleshooting Diagram 19



Troubleshooting Diagram 20



APPENDIX

Execution Times for Instructions

Execution times for basic and advanced instructions of the MicroSmart are listed below.

Repeat is not designated for any device.

Instruction	Device and Condition	Execution Time (µs)	
		All-in-One Type CPU Module	Slim Type CPU Module
LOD, LODN		0.7	0.056
	Using data register	14	
OUT, OUTN		2.2	0.111
	Using data register	26	
SET, RST		2.1	0.111
	Using data register	16	
AND, ANDN, OR, ORN		0.5	0.111
	Using data register	20	
AND LOD, OR LOD		0.8	0.111
BPS		0.6	0.056
BRD, BPP		0.4	0.056
TML, TIM, TMH, TMS		17	0.389 (17) (Note)
TMLO, TIMO, TMHO, TMSO		22	
CNT, CDP, CUD		19	
CNTD, CDPD, CUDD		33	
CC=, CC≥		8	0.111 (8) (Note)
DC=, DC≥		8	0.167 (8) (Note)
SFR, SFRN	N bits	52 + 0.21N	
SOTU, SOTD		14	0.111
JMP, JEND, MCS, MCR		2	0.222
MOV, MOVN (W, I)	M → M	56	
	D → D	32	0.167
MOV, MOVN (D, L)	M → M	64	
	D → D	44	0.278
MOV (F)		74	
IMOV, IMOVN (W)	M+D→M+D, D+D→D+D	88	
IMOV, IMOVN (D)	D+D → D+D	92	
IMOV (F)		126	
BMOV	D → D	62 + 15.8N (N words)	
IBMV, IBMVN	M+D→M+D, D+D→D+D	82	
NSET (W, I)	D → D	60	
NSET (D, L)	D → D	70	
NSET (F)	D → D	76	
NRS (W, I)	D, D → D	62	
NRS (D, L)	D, D → D	62	

Instruction	Device and Condition	Execution Time (µs)	
		All-in-One Type CPU Module	Slim Type CPU Module
NRS (F)	D, D → D	64	
XCHG	D ↔ D	67	
TCCST (W)	D → T	66	
TCCST (D)	D → T	71	
CMP (W, I)	D ↔ D → M	64	
CMP (D, L)	D ↔ D → M	67	
CMP (F)	D ↔ D → M	80	
ICMP>=	D ↔ D ↔ D → M	79	
LC (W, I)	D ↔ D	70	
LC (D, L)	D ↔ D	76	
LC (F)	D ↔ D	86	
ADD (W, I)	M + M → D	68	
	D + D → D	44	0.278 (44) (Note)
ADD (D, L)	M + M → D	80	
	D + D → D	65	
ADD (F)	D + D → D	135 (1 decimal place)	
SUB (W, I)	M – M → D	71	
	D – D → D	60	0.278 (60) (Note)
SUB (D, L)	M – M → D	91	
	D – D → D	66	
SUB (F)	D – D → D	134 (1 decimal place)	
MUL (W, I)	M × M → D	61	
	D × D → D	60	
MUL (D, L)	M × M → D	83	
	D × D → D	76	
MUL (F)	D × D → D	104	
DIV (W, I)	M ÷ M → D	71	
	D ÷ D → D	71	
DIV (D, L)	M ÷ M → D	98	
	D ÷ D → D	89	
DIV (F)	D ÷ D → D	166	
INC (W, I)		49	
INC (D, L)		53	
DEC (W, I)		49	
DEC (D, L)		54	
ROOT (W)	$\sqrt{D}$ → D	165	
ROOT (D)	$\sqrt{D}$ → D	228	
ROOT (F)	$\sqrt{D}$ → D	926	
SUM (W, I)	D, D → D	94	
SUM (D, L)	D, D → D	96	
SUM (F)	D, D → D	165	
RNDM	D, D → D	80	
ANDW, ORW, XORW (W)	M · M → D, D · D → D	60	

Instruction	Device and Condition	Execution Time (µs)	
		All-in-One Type CPU Module	Slim Type CPU Module
ANDW, ORW, XORW (D)	D · D → D	65	
SFTL, SFTR	N_B = 100	125	
BCDLS	D → D, S1 = 1	77	
WSFT	D → D	62 + 16.1N (N words to shift)	
ROTL, ROTR	D, bits = 1	46	
HTOB	D → D	61	
BTOH	D → D	56	
HTOA	D → D	66	
ATOH	D → D	62	
BTOA (W)	D → D	68	
BTOA (D)	D → D	65	
ATOB (W)	D → D	61	
ATOB (D)	D → D	64	
ENCO	M → D, 16 bits	42	
DECO	D → M	47	
BCNT	M → D, 16 bits	185	
ALT		33	
CVDT	W, I, D, L → F	106	
	F → W, I, D, L	142	
DTDV (W)	D → D	63	
DTCB (W)	D → D	63	
SWAP (W)		64	
SWAP (D)		67	
DISP	BCD 5 digits	70	
	BIN 4 digits	66	
DGRD	BCD 5 digits	62	
	BIN 4 digits	61	
LCAL		32	
LRET		17	
DJNZ	D, D	56	
DI		22	
EI		25	
IOREF		18	
HSCRF		36	
FRQRF		33	
COMRF		4000	
AVRG (W, I)	S3 = 10	84	
AVRG (D, L)	S3 = 10	88	
AVRG (F)	S3 = 10	161	
PID	AT+PID in progress	520	
DTML, DTIM, DTMH		87	
DTMS		92	
TTIM		50	

Instruction	Device and Condition	Execution Time (µs)	
		All-in-One Type CPU Module	Slim Type CPU Module
RAD	F → F	127	
DEG	F → F	145	
SIN, COS	F → F	1826	
TAN	F → F	1736	
ASIN, ACOS	F → F	6090	
ATAN	F → F	5402	
LOGE, LOG10	F → F	2999	
EXP	F → F	1072	
POW	F → F	3819	
FIFOF		114	
FIEX		41	
FOEX		42	
NDSRC (W, I)	D, D, D → D	110	
NDSRC (D, L)	D, D, D → D	113	
NDSRC (F)	D, D, D → D	143	
TADD		100	
TSUB		99	
HTOS		64	
STOH	D → D	74	
HOUR	D ↔ D → Q, D	94	

Note: Values in ( ) show instruction execution times on slim type CPU modules with Logic Engine version lower than 200 (not included) or system program version lower than 210 (not included). Logic Engine version is found in the lower right corner of the label on the side of the slim type CPU module. To confirm the system program version of the MicroSmart CPU module, use WindLDR on a computer connected with the CPU module. Bring WindLDR into the online mode. The system program version is indicated on the PLC Status dialog box. See page 13-1.

Processing in One Scan

While the MicroSmart CPU module is running, the CPU module performs operations repeatedly such as input refreshing, ladder program processing, output refreshing, and error checking.

A *scan* is the execution of all instructions from address zero to the END instruction. The time required for this execution is referred to as one *scan time*. The scan time varies with respect to program length.

The current value of the scan time is stored to special data register D8023 (scan time current value), and the maximum value of the scan time is stored to special data register D8024 (scan time maximum value). These values can be viewed on the PLC status screen of WindLDR while monitoring on a PC.

Executing Program Instructions

During the scan time, program instructions are processed sequentially starting with the first line of the ladder program, except for interrupt program execution. The one scan time of a ladder program is approximately equal to the total of execution time of each instruction shown on preceding pages.

Watchdog Timer

The watchdog timer monitors the time required for one program cycle (scan time) to prevent hardware malfunction. When the time exceeds approximately 340 ms, the watchdog timer indicates an error and stops CPU operation. If this is the case, place NOP instructions in the ladder diagram. The NOP instruction resets the watchdog timer.

Breakdown of END Processing Time

The END processing time depends on the MicroSmart settings and system configuration. The total of execution times for applicable conditions shown below is the actual END processing time.

Item	Condition	Execution Time
Housekeeping (built-in I/O service)	Slim 32-I/O type CPU	263 µs
Expansion I/O service (1 expansion I/O module)	8 inputs or 8 outputs	130 µs
	16 inputs or 16 outputs	183 µs
	32 inputs or 32 outputs	357 µs
	4 inputs and 4 outputs	127 µs
	16 inputs and 8 outputs	305 µs
Expansion Processing (1 analog I/O module) (Note 1)	END refresh type	1.8 ms
Expansion Processing (1 expansion interface module)	Integrated or separate mounting	2.5 ms (one 4-in/4-out mixed I/O module) 4.5 ms (seven 32-I/O modules)
Expansion Processing (1 expansion RS232C/RS485 communication module)	—	(Note 2)
AS-Interface Master Module (Note 3)	AS-Interface master module 1	9.4 ms
Clock function processing (Note 4)	—	850 µs

Note 1: Expansion bus processing time per ladder refresh type analog I/O module depends on the byte count of the RUNA/STPA communication data.
Note 2: See page 2-88 for the processing time of the expansion RS232C/RS485 communication modules.
Note 3: Processing time of AS-Interface master module 2 depends on the byte count of the RUNA/STPA communication data.
Note 4: Clock function is processed once every 500 ms.

I/O Refreshing by Expansion Interface Module

The expansion interface module performs I/O refreshing independent of the I/O refreshing by the CPU module. While the I/O refresh time (D8252 expansion interface module I/O refresh time ×100 µs) of the expansion interface module is longer than the CPU module scan time (D8023 scan time current value in ms), executing OUT/OUTN, SET/RST, SOTU/SOTD or ALT instructions, which change output statuses every scan, may fail to generate outputs to the output modules beyond the expansion interface module correctly in every scan.

If the I/O refresh time of the expansion interface module is longer than the CPU module scan time, adjust the scan time using special data register D8022 (constant scan time preset value in ms) or change the mounting positions of the expansion I/O modules.

Instruction Bytes and Applicability in Interrupt Programs

The quantities of bytes of basic and advanced instructions are listed below. Applicability of basic and advanced instructions in interrupt programs are also shown in the rightmost column of the following tables.

Basic Instruction	Qty of Bytes		Interrupt
	All-in-One Type CPU Module	Slim Type CPU Module	
LOD, LODN	6	4	X
OUT, OUTN	6	4	X
SET, RST	6	4	X
AND, ANDN, OR, ORN	4	4	X
AND LOD, OR LOD	5	4	X
BPS	5	4	X
BRD	3	4	X
BPP	2	4	X
TML, TIM, TMH, TMS	4	12 to 14	—
TMLO, TIMO, TMHO, TMSO	4	12 to 14	—
CNT, CDP, CUD	4	12 to 14	—
CNTD, CDPD, CUDD	4	12 to 14	—
CC=, CC≥	7	12 to 14	X
DC=, DC≥	8	12 to 14	X
SFR, SFRN	6	10	—
SOTU, SOTD	5	4	—
JMP	4	6	X
JEND, MCS, MCR	4	4	X
END	2	4	X

Note: One bit of data register is not used in the measurement of bytes of basic instructions.

Advanced Instruction	Qty of Bytes		Interrupt
	All-in-One Type CPU Module	Slim Type CPU Module	
NOP	2	4	X
MOV, MOVN	16 to 18	12 to 16	X
IMOV, IMOVN	20 to 24	14 to 16	X
BMOV	18	12 to 16	X
IBMV, IBMVN	20 to 24	14 to 16	X
NSET	17 to 1543	12 to 1542	X
NRS	18 to 20	12 to 20	X
XCHG	28	10 to 14	X
TCCST	16 to 18	12 to 16	X
CMP	20 to 24	14 to 22	X
ICMP>=	22 to 28	14 to 26	X
LC	14 to 18	12 to 20	X
ADD, SUB, MUL, DIV	20 to 24	14 to 22	X
INC	10	8 to 10	X
DEC	10	8 to 10	X
ROOT	14 to 16	10 to 14	X
SUM	20	14 to 20	X

Advanced Instruction	Qty of Bytes		Interrupt
	All-in-One Type CPU Module	Slim Type CPU Module	
RNDM	18	12 to 18	X
ANDW, ORW, XORW	20 to 24	14 to 22	X
SFTL, SFTR	22	14 to 20	X
BCDLS	14	10 to 12	X
WSFT	18	12 to 16	X
ROTL, ROTR	12	10	X
HTOB, BTOH	14 to 16	10 to 14	X
HTOA, ATOH	18 to 22	12 to 16	X
BTOA	18 to 20	12 to 18	X
ATOB	18	12 to 18	X
ENCO, DECO	16	12 to 14	X
BCNT	18	12 to 14	X
ALT	10	8	X
CVDT	16 to 18	12 to 16	X
DTDV	14	10 to 14	X
DTCB	14	10 to 14	X
SWAP	16	12 to 16	X
WKTIM	24	16 to 22	—
WKTBL	12 to 88	10 to 88	—
DISP	16	12	—
DGRD	20	14	—
TXD1, TXD2, RXD1, RXD2	21 to 819	16 to 814	—
LABEL	8	8	X
LJMP, LCAL	10	8 to 10	X
LRET	6	6	X
DJNZ	14	10 to 14	X
DI, EI	8	8	—
IOREF	12	10	X
HSCRF, FRQRF	6	6	X
COMRF	2	4	—
XYFS	28 to 268	20 to 268	—
CVXTY, CVYTX	18	14 to 16	—
AVRG	26	16 to 18	—
PULS1, PULS2, PULS3	—	10	—
PWM1, PWM2, PWM3	—	10	—
RAMP1, RAMP2	—	10	—
ZRN1, ZRN2, ZRN3	—	12	—
PID	26	16 to 18	—
DTML, DTIM, DTMH, DTMS	22	14 to 18	—
TTIM	10	8	—
RUNA, STPA	20	16 to 18	—
RAD, DEG, SIN, COS, TAN, ASIN, ACOS, ATAN	14 to 16	10 to 14	X
LOGE, LOG10, EXP	14 to 16	10 to 14	X

Advanced Instruction	Qty of Bytes		Interrupt
	All-in-One Type CPU Module	Slim Type CPU Module	
POW	18 to 22	12 to 20	X
FIFOF	24	20 to 22	—
FIEX	12	10 to 12	X
FOEX	12	10 to 12	X
NDSRC	22 to 24	14 to 24	—
TADD	20	14 to 20	X
TSUB	20	14 to 20	X
HTOS	14	10 to 14	X
STOH	14 to 16	10 to 16	X
HOUR	24	16 to 22	—
EMAIL	—	12 to 14	—
PING	—	12 to 14	—
ETXD	—	16 to 814	—
ERXD	—	16 to 814	—

Upgrade FC5A MicroSmart System Program

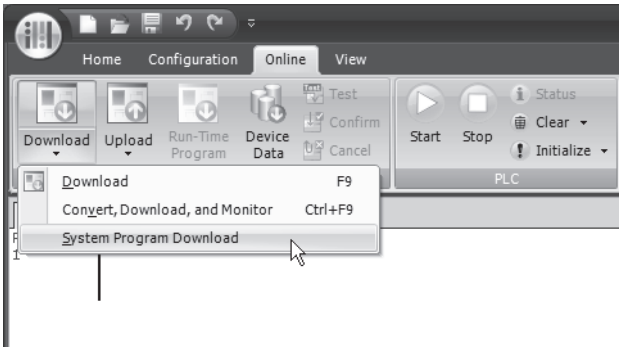
The system program of any type of FC5A MicroSmart CPU modules can be upgraded using System Program Download of WindLDR. If the system program of your FC5A MicroSmart CPU module is old, upgrade the system program with the following procedure:

1. Connect the MicroSmart CPU module to the PC using the computer link cable 4C (FC2A-KC4C).

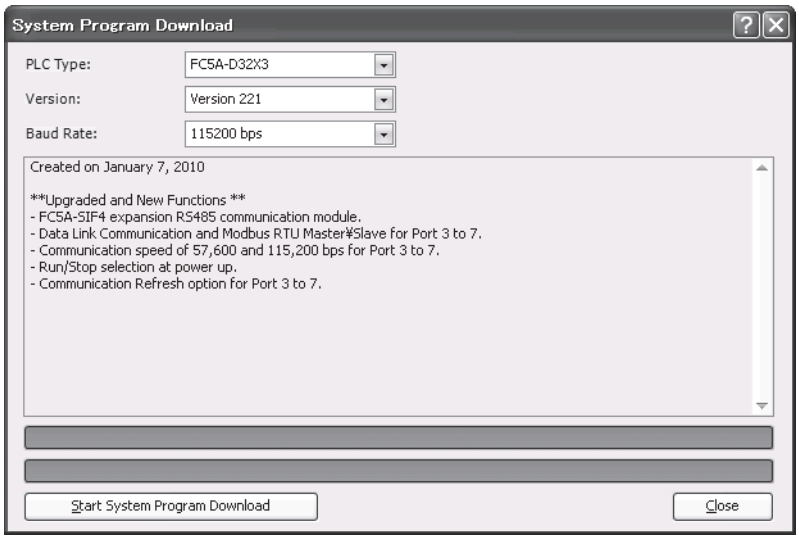
Notes:

- The system program cannot be upgraded when Ethernet is selected or Pass-Through is enabled.
- When using FC5A-D12K1E or FC5A-D12S1E, use a USB cable.

2. From the WindLDR menu bar, select **Online** > **Download** > **System Program Download**.

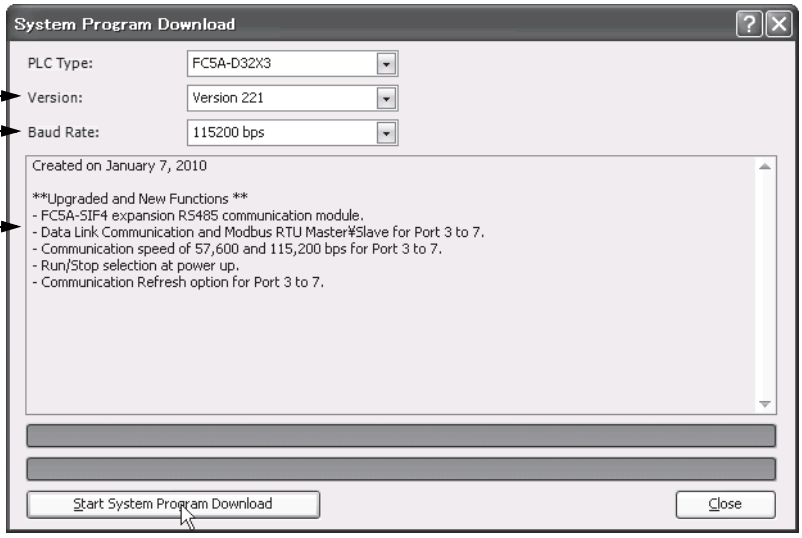


The System Program Download dialog box appears.



3. Select the PLC type, the system program version to download, and the baud rate, and then click **Download System Program**.

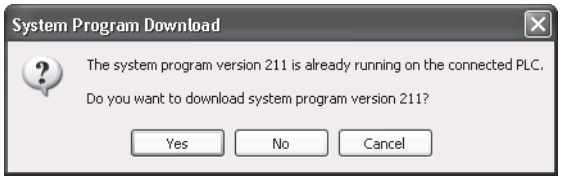
The latest version is indicated as default.
Older versions are also available.
Selects the baud rate at which to download the system program.
Details of upgrades are indicated.



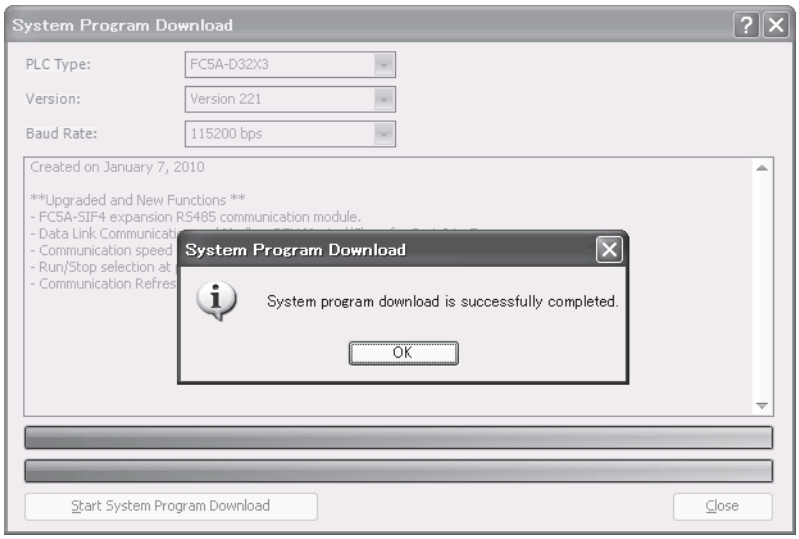
Notes:

- If the FC5A MicroSmart is running, it is stopped automatically before the system program download starts.
- Older system programs can also be downloaded to the MicroSmart if required.
- The system program download takes about one minute when a baud rate of 115200 bps is selected.

4. A confirmation message is displayed. Click **OK** to start downloading the system program.



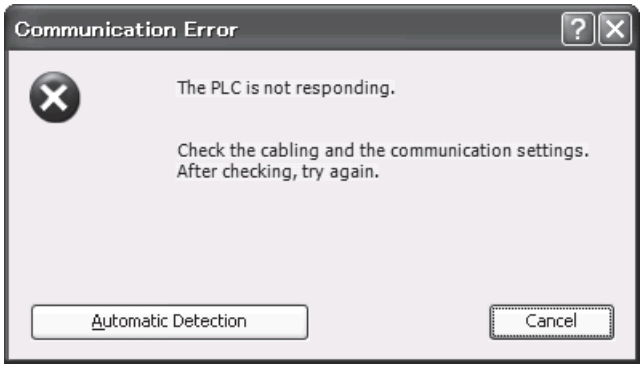
5. System program download status is shown by a progress bar. A completion message appears when the system program has been downloaded successfully. Click **OK** to close the System Program Download dialog box.



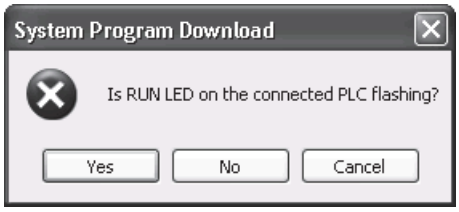
Notes:

- While the system program is downloaded to the MicroSmart, the RUN LED on the CPU module flashes.
- After the system program download, the MicroSmart remains stopped. To start the MicroSmart, select **Online** > **Start** from the WindLDR menu bar. The MicroSmart can also be started using HMI module. See page 2-80 (Basic Vol.).
- The user program stored in the MicroSmart before downloading the system program remains and is executed when the MicroSmart is restarted. A user program execution error may occur if an older system program is downloaded to the MicroSmart.
- In the event that the system update process fails, the RUN LED on the FC5A MicroSmart may keep flashing continuously. In such cases, turn the FC5A MicroSmart off and on, and then retry the update procedure from the step 1. If the RUN LED continues flashing after the power is turned off and on, a communication error dialog box is displayed before the step 4. In such cases, perform the following two steps.

1) A communication error dialog box is displayed. Click **Cancel**.



2) A dialog box prompting you to check the RUN LED status is displayed. Click **Yes**.



Getting the Latest Version of the System Program

When you install or upgrade to the latest version of Automation Organizer, the latest system programs are also installed along with the software.

Cables

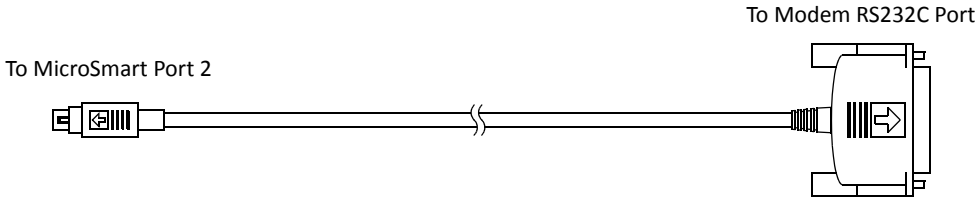
Communication cables and their connector pinouts are described in this section.

Communication Port and Applicable Cables

Connector	Communication Port	Applicable Cable
RS232C Mini DIN Connector	Built-in port on CPU module	FC2A-KM1C FC2A-KC4C FC2A-KP1C FC4A-KC1C FC4A-KC2C
	FC4A-PC1 (RS232C Communication Adapter)	
	FC4A-HPC1 (RS232C Communication Module)	
	FC4A-SX5ES1E (Web Server Module)	FC4A-KC3C
RS485 Mini DIN Connector	FC4A-PC2 (RS485 Communication Adapter)	FC2A-KP1C
	FC4A-HPC2 (RS485 Communication Module)	

Modem Cable 1C (FC2A-KM1C)

Cable Length: 3m (9.84 feet)



Mini DIN Connector Pinouts

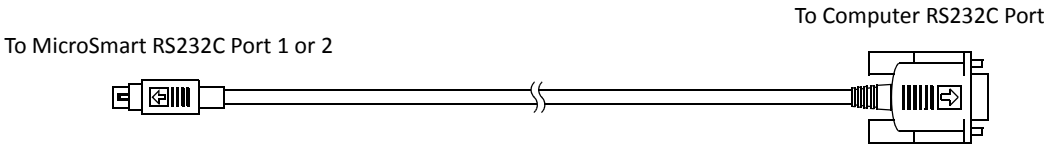
Description		Pin
Shield		**Cover**
RTS	Request to Send	**1**
DTR	Data Terminal Ready	**2**
TXD	Transmit Data	**3**
RXD	Receive Data	**4**
DSR	Data Set Ready	**5**
SG	Signal Ground	**6**
SG	Signal Ground	**7**
NC	No Connection	**8**

D-sub 25-pin Male Connector Pinouts

Pin	Description	
1	FG	Frame Ground
2	TXD	Transmit Data
3	RXD	Receive Data
4	RTS	Request to Send
5	NC	No Connection
6	NC	No Connection
7	SG	Signal Ground
8	DCD	Data Carrier Detect
20	DTR	Data Terminal Ready

Computer Link Cable 4C (FC2A-KC4C)

Cable Length: 3m (9.84 feet)



Mini DIN Connector Pinouts

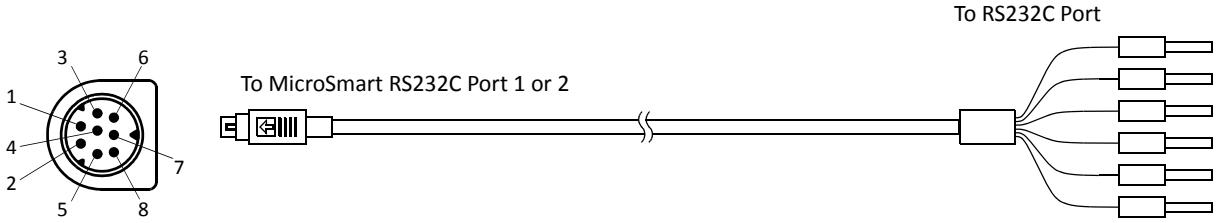
Description		Pin
Shield		Cover
TXD	Transmit Data	3
RXD	Receive Data	4
RTS	Request to Send	1
NC	No Connection	8
DSR	Data Set Ready	5
DTR	Data Terminal Ready	2
SG	Signal Ground	7
SG	Signal Ground	6

D-sub 9-pin Female Connector Pinouts

Pin	Description	
Cover	FG	Frame Ground
3	TXD	Transmit Data
2	RXD	Receive Data
6	DSR	Data Set Ready
8	CTS	Clear to Send
1	DCD	Data Carrier Detect
4	DTR	Data Terminal Ready
5	SG	Signal Ground
7	NC	No Connection
9	NC	No Connection

User Communication Cable 1C (FC2A-KP1C)

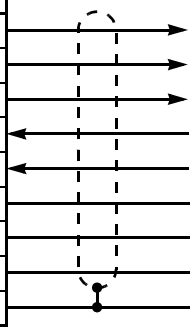
Cable Length: 2.5m (8.2 feet)



Mini DIN Connector Pinouts

Pin	Port 1		Port 2		AWG#		Color
1	NC	No Connection	RTS	Request to Send	28	Twisted	Black
2	NC	No Connection	DTR	Data Terminal Ready	28		Yellow
3	TXD	Transmit Data	TXD	Transmit Data	28		Blue
4	RXD	Receive Data	RXD	Receive Data	28		Green
5	NC	No Connection	DSR	Data Set Ready	28		Brown
6	CMSW	Communication Switch	SG	Signal Ground	28		Gray
7	SG	Signal Ground	SG	Signal Ground	26	Twisted	Red
8	NC	No Connection	NC	No Connection	26		White
Cover	—		—		—		Shield

Signal Direction



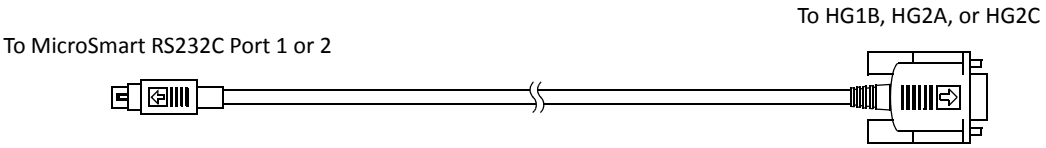
Note: When preparing a cable for port 1, keep pins 6 and 7 open. If pins 6 and 7 are connected together, user communication cannot be used. Make sure that unused leads do not interconnect.

Caution

- Do not connect any wiring to NC terminals, otherwise operation failure or device damage may be caused.

O/I Communication Cable 1C (FC4A-KC1C)

Cable Length: 5m (16.4 feet)



Mini DIN Connector Pinouts

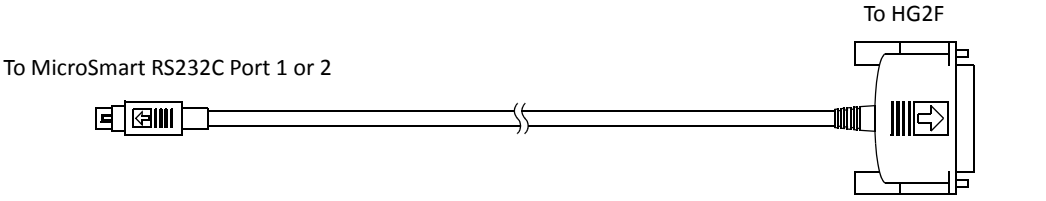
Description		Pin
NC	No Connection	1
NC	No Connection	2
TXD	Transmit Data	3
RXD	Receive Data	4
NC	No Connection	5
CMSW	Communication Switch	6
SG	Signal Ground	7
NC	No Connection	8
Shield		Cover

D-sub 9-pin Male Connector Pinouts

Pin	Description	
1	FG	Frame Ground
2	TXD1	Transmit Data 1
3	RXD1	Receive Data 1
4	TXD2	Transmit Data 2
5	RXD2	Receive Data 2
6	DSR	Data Set Ready
7	SG	Signal Ground
8	NC	No Connection
9	DTR	Data Terminal Ready

O/I Communication Cable 2C (FC4A-KC2C)

Cable Length: 5m (16.4 feet)



Mini DIN Connector Pinouts

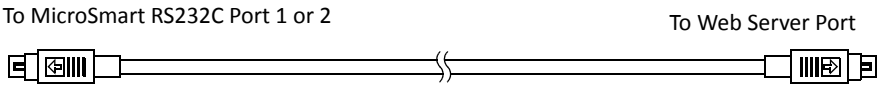
Description		Pin
NC	No Connection	1
NC	No Connection	2
TXD	Transmit Data	3
RXD	Receive Data	4
NC	No Connection	5
CMSW	Communication Switch	6
SG	Signal Ground	7
NC	No Connection	8
Shield		Cover

D-sub 25-pin Male Connector Pinouts

Pin	Description	
1	FG	Frame Ground
2	TXD	Transmit Data
3	RXD	Receive Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	SG	Signal Ground
8	DCD	Data Carrier Detect
20	DTR	Data Terminal Ready

Web Server Cable (FC4A-KC3C)

Cable Length: 100 mm (3.94 in.)



Mini DIN Connector Pinouts

Pin	Port 1	Port 2
1	NC	RTS
2	NC	DTR
3	TXD	TXD
4	RXD	RXD
5	NC	DSR
6	CMSW	SG
7	SG	SG
8	NC	NC
Cover	Shield	Shield

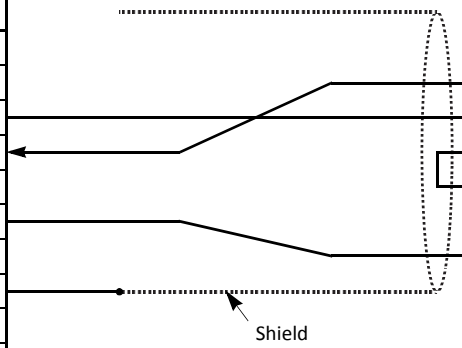
Mini DIN Connector Pinouts

Pin	Port 2
1	DSR Data Set Ready
2	CTS Clear to Send
3	TXD Transmit Data
4	RXD Receive Data
5	RTS Request to Send
6	NC No Connection
7	SG Signal Ground
8	DTR Data Terminal Ready
Cover	Shield

FC5A-SIF2 Cable Connection with Operator Interface (RS232C)

FC5A-SIF2

Terminal
RS (RTS)
ER (DTR)
SD (TXD)
RD (RXD)
DR (DSR)
SG (SG)
NC
⏚
⏚
⏚



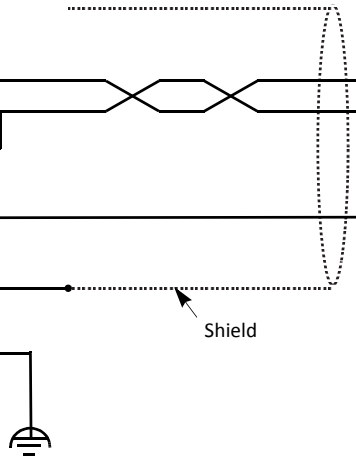
HG series Operator Interface

Pin					Description
HG3G (Connector)	HG2G/HG3G (Terminal Block)	HG1F	HG2F/ 3F/4F	HG2S	
—	—	**1**	**1**	**1**	FG
3	**1**	**2**	**2**	**30**	SD
2	**2**	**3**	**3**	**32**	RD
7	**3**	**9**	**4**	**34**	RS
8	**4**	**6**	**5**	**36**	CS
—	—	—	**6**	—	NC
5	**5**	**7**	**7**	**29**	SG
—	—	—	**8**	—	NC
—	—	—	**20**	—	ER

FC5A-SIF4 Cable Connection with Operator Interface (RS485)

FC5A-SIF4

Terminal
NC
A
A
B
B
SG
SG
⏚
⏚
⏚



HG series Operator Interface

Pin					Description
HG3G (Connector)	HG2G/HG3G (Terminal Block)	HG1F*1	HG2F/ 3F/4F	HG2S	
—	—	—	1	1	FG
1	8	3	10	32	RDA (RD+)
6	9	4	16	33	RDB (RD-)
*2	6	1	11	30	SDA (SD+)
*2	7	2	15	31	SDB (RD-)
—	—	—	18	37	CS- *3
—	—	—	19	35	RS- *3
—	—	—	21	36	CS+ *3
—	—	—	22	34	RS+ *3
5	5	5	7	39	SG

***1:** Terminal numbers are described.

***2:** As HG3G uses only RDA and RDB for RS-485(422) 2-wire method communication, connecting SDA and SDB is unnecessary.

***3:** When HG2G or HG1F is used, wiring CS-, RS-, CS+, and RS+ is unnecessary. Disable the hardware flow control of the connected HG series operator interface.

Communication Ports and Functions

The communication functions of each communication port are described in this section.

CPU Modules with System Program version 210

Communication Function		Port 1 (RS232C)	Port 2 (RS232C)	Port 2 (RS485)	Ports 3 to 7 (FC5A-SIF2 earlier than V200)	Ports 3 to 7 (FC5A-SIF2 V200 or higher) (Note 1)	Ports 3 to 7 (FC5A-SIF4)
Maintenance Communication	Program Download and Upload	X	X	X	—	—	—
	Monitoring	X	X	X	X	X	—
User Communication		X	X	X	X	X	—
Modem Communication		—	X	—	—	—	—
Data Link	Master	—	—	X	—	—	—
	Slave	—	—	X	—	—	—
Modbus RTU	Master	—	X	X	—	—	—
	Slave	X (Note 2)	X	X	—	—	—
Modbus ASCII	Master	—	X	X	—	—	—
	Slave	X (Note 2)	X	X	—	—	—
Modbus TCP	Master (Client)	—	X	—	—	—	—
	Slave (Server)	X (Note 2)	X	—	—	—	—

Note 1: The maximum baud rate for FC5A-SIF2 (version 200 or higher) is 115200 bps. When FC5A-SIF2 is used in conjunction with a CPU module with system program version earlier than 220, the maximum baud rate is 38400 bps.

Note 2: Modbus slave communication is available on CPU module with system program version 210 or higher.

CPU Modules with System Program version 220 or higher

Communication Function		Port 1 (RS232C)	Port 2 (RS232C)	Port 2 (RS485)	Ports 3 to 7 (FC5A-SIF2 earlier than V200)	Ports 3 to 7 (FC5A-SIF2 V200 or higher) (Note 1)	Ports 3 to 7 (FC5A-SIF4)
Maintenance Communication	Program Download and Upload	X	X	X	X (Note 1)	X (Note 1)	X (Note 1)
	Monitoring	X	X	X	X	X	X
User Communication		X	X	X	X	X	X
Modem Communication		—	X	—	—	—	—
Data Link	Master	—	—	X	—	—	X
	Slave	—	—	X	—	—	X
Modbus RTU	Master	—	X	X	—	X	X
	Slave	X	X	X	—	X	X
Modbus ASCII	Master	—	X	X	—	X	X
	Slave	X	X	X	—	X	X
Modbus TCP	Master (Client)	—	X	—	—	—	—
	Slave (Server)	X	X	—	—	—	—

Note 1: Transfer mode must be set to ASCII to download or upload the user program. Run-time program download cannot be used.

Slim Type Web Server CPU Module

Communication Function		Port 1 (USB)	Port 2 (RS232C)	Port 2 (RS485)	Ports 3 to 7 (FC5A-SIF2 earlier than V200)	Ports 3 to 7 (FC5A-SIF2 V200 or higher)	Ports 3 to 7 (FC5A-SIF4)
Maintenance Communication	Program Download and Upload	X	X	X	X (Note 1)	X (Note 1)	X (Note 1)
	Monitoring	X	X	X	X	X	X
User Communication		—	X	X	X	X	X
Modem Communication		—	—	—	—	—	—
Data Link	Master	—	—	X	—	—	X
	Slave	—	—	X	—	—	X
Modbus RTU	Master	—	X	X	—	X	X
	Slave	—	X	X	—	X	X
Modbus ASCII	Master	—	X	X	—	X	X
	Slave	—	X	X	—	X	X
Modbus TCP (Note 2)	Master (Client)	—	—	—	—	—	—
	Slave (Server)	—	—	—	—	—	—

Note 1: Transfer mode must be set to ASCII to download or upload the user program. Run-time program download cannot be used.

Note 2: Though Modbus TCP communication cannot be used on port 2 of FC5A-D12K1E and FC5A-D12S1E, it can be used on the built-in Ethernet port.

Type List

CPU Modules (All-in-One Type)

Power Voltage	Input Type	Output Type	I/O Points	Type No.
100-240V AC 50/60 Hz	24V DC Sink/Source	Relay Output 240V AC/30V DC, 2A	10-I/O Type (6 in / 4 out)	FC5A-C10R2
			16-I/O Type (9 in / 7 out)	FC5A-C16R2
			24-I/O Type (14 in / 10 out)	FC5A-C24R2
24V DC			10-I/O Type (6 in / 4 out)	FC5A-C10R2C
			16-I/O Type (9 in / 7 out)	FC5A-C16R2C
			24-I/O Type (14 in / 10 out)	FC5A-C24R2C
12V DC	12V DC Sink/Source		10-I/O Type (6 in / 4 out)	FC5A-C10R2D
			16-I/O Type (9 in / 7 out)	FC5A-C16R2D
			24-I/O Type (14 in / 10 out)	FC5A-C24R2D

CPU Modules (Slim Type)

Power Voltage	Input Type	Output Type		I/O Points	Type No.
24V DC	24V DC Sink/ Source	Relay Output 240V AC/30V DC, 2A	Transistor Sink Output 0.3A	16 (8 in / 8 out) *	FC5A-D16RK1
			Transistor Source Output 0.3A		FC5A-D16RS1
		Transistor Sink Output 0.3A		32 (16 in / 16 out)	FC5A-D32K3
		Transistor Source Output 0.3A			FC5A-D32S3

Note *: Two points are transistor outputs, and six points are relay outputs.

Web Server CPU Modules

Power Voltage	Input Type	Output Type	I/O Points	Type No.
24V DC	24V DC Sink/ Source	Transistor Sink Output 0.3A	12 (8 in / 4 out)	FC5A-D12K1E
		Transistor Source Output 0.3A		FC5A-D12S1E

Input Modules

Input Type	Input Points	Terminal	Type No.
24V DC Sink/Source	8 points	Removable Terminal Block	FC4A-N08B1
	16 points		FC4A-N16B1
	16 points	MIL Connector	FC4A-N16B3
	32 points		FC4A-N32B3
120V AC	8 points	Removable Terminal Block	FC4A-N08A11

Output Modules

Output Type	Output Points	Terminal	Type No.
Relay Output 240V AC/30V DC, 2A	8 points	Removable Terminal Block	FC4A-R081
	16 points		FC4A-R161
Transistor Sink Output 0.3A	8 points		FC4A-T08K1
Transistor Source Output 0.3A			FC4A-T08S1
Transistor Sink Output 0.1A	16 points	MIL Connector	FC4A-T16K3
Transistor Source Output 0.1A			FC4A-T16S3
Transistor Sink Output 0.1A	32 points		FC4A-T32K3
Transistor Source Output 0.1A			FC4A-T32S3

Mixed I/O Modules

Input Type	Output Type	I/O Points	Terminal	Type No.
24V DC Sink/Source	Relay Output 240V AC/30V DC, 2A	8 (4 in / 4 out)	Removable Terminal Block	FC4A-M08BR1
		24 (16 in / 8 out)	Non-removable Terminal Block	FC4A-M24BR2

Analog I/O Modules

Name	I/O Signal	I/O Points	Category	Terminal	Type No.
Analog I/O Module	Voltage (0 to 10V DC) Current (4 to 20mA)	2 inputs	END Refresh Type	Removable Terminal Block	FC4A-L03A1
	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output			
	Thermocouple (K, J, T) Resistance thermometer (Pt100)	2 inputs			FC4A-L03AP1
	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output			
Analog Input Module	Voltage (0 to 10V DC) Current (4 to 20mA)	2 inputs			FC4A-J2A1
	Voltage (0 to 10V DC) Current (4 to 20mA) Thermocouple (K, J, T) Resistance thermometer (Pt100, Pt1000, Ni100, Ni1000)	4 inputs	Ladder Refresh Type		FC4A-J4CN1
	Voltage (0 to 10V DC) Current (4 to 20mA)	8 inputs			FC4A-J8C1
	Thermistor (PTC, NTC)	8 inputs			FC4A-J8AT1
Analog Output Module	Voltage (0 to 10V DC) Current (4 to 20mA)	1 output	END Refresh		FC4A-K1A1
	Voltage (–10 to +10V DC) Current (4 to 20mA)	2 outputs	Ladder Refresh		FC4A-K2C1
	Voltage (0 to 10V DC) Current (4 to 20mA)	4 outputs			FC4A-K4A1

Optional Modules, Adapters, and Cartridges

Name	Description	Type No.
Expansion Interface Module	For integrated mounting	FC5A-EXM2
Expansion Interface Master Module	For separate mounting	FC5A-EXM1M
Expansion Interface Slave Module		FC5A-EXM1S
HMI Module	For displaying and changing required devices	FC4A-PH1
HMI Base Module	For mounting HMI module with slim type CPU module	FC4A-HPH1
RS232C Communication Adapter *	Mini DIN connector type for all-in-one 16- and 24-I/O CPU modules	FC4A-PC1
RS485 Communication Adapter *	Mini DIN connector type for all-in-one 16- and 24-I/O CPU modules	FC4A-PC2
	Terminal block type for all-in-one 16- and 24-I/O CPU modules	FC4A-PC3
RS232C Communication Module	Mini DIN connector type for slim type CPU module	FC4A-HPC1
RS485 Communication Module	Mini DIN connector type for slim type CPU module	FC4A-HPC2
	Terminal block type for slim type CPU module	FC4A-HPC3
PID Module	Relay output type PID module	FC5A-F2MR2
	Voltage/current output type PID module	FC5A-F2M2
Expansion RS232C Communication Module	Expansion communication module for RS232C port 3 through port 7	FC5A-SIF2
Expansion RS485 Communication Module	Expansion communication module for RS485 port 3 through port 7	FC5A-SIF4
Memory Cartridge	32KB EEPROM for storing a user program	FC4A-PM32
	64KB EEPROM for storing a user program	FC4A-PM64
	128KB EEPROM for storing a user program	FC4A-PM128
Clock Cartridge	Real time calendar/clock function	FC4A-PT1
AS-Interface Master Module	Master module for AS-Interface network	FC4A-AS62M
Web Server Module	For communication through Ethernet	FC4A-SX5ES1E

Note *: RS232C or RS485 communication adapters can also be installed on the HMI base module mounted next to the slim type CPU module.

Accessories

Name	Function	Type No.
DIN Rails (1m/3.28 ft. long)	35-mm-wide aluminum DIN rail to mount MicroSmart modules (package quantity 10)	BAA1000PN10
DIN Rails (1m/3.28 ft. long)	35-mm-wide steel DIN rail to mount MicroSmart modules (package quantity 10)	BAP1000PN10
End Clips	Used on DIN rail to fasten MicroSmart modules (package quantity 10)	BNL6PN10
Direct Mounting Strips	Used for direct mounting of slim type CPU or I/O modules on a panel (package quantity 5)	FC4A-PSP1PN05
10-position Terminal Blocks	For I/O modules (package quantity 2)	FC4A-PMT10PN02
11-position Terminal Blocks	For I/O modules (package quantity 2)	FC4A-PMT11PN02
13-position Terminal Blocks	For slim type CPU modules FC5A-D16RK1 and FC5A-D16RS1 (package quantity 2)	FC5A-PMT13PN02
16-position Terminal Blocks	For slim type CPU module FC5A-D16RK1 (package quantity 2)	FC4A-PMTK16PN02
16-position Terminal Blocks	For slim type CPU module FC5A-D16RS1 (package quantity 2)	FC4A-PMTS16PN02
16-position Terminal Blocks	For slim type Web Server FC5A-D12K1E (package quantity 2)	FC5A-PMTK16EPN02
16-position Terminal Blocks	For slim type Web Server FC5A-D12S1E (package quantity 2)	FC5A-PMTS16EPN02
20-position Connector Socket	MIL connector for I/O modules (package quantity 2)	FC4A-PMC20PN02
26-position Connector Socket	MIL connector for slim type CPU modules (package quantity 2)	FC4A-PMC26PN02
Phoenix Ferrule	Ferrule for connecting 1 or 2 wires to screw terminal	See page 3-23
Phoenix Crimping Tool	Used for crimping ferrules	See page 3-23
Phoenix Screwdriver	Used for tightening screw terminals	See page 3-23
Automation Organizer	Software suite containing WindLDR - PLC programming software	SW1A-W1C
FC5A MicroSmart User's Manual Basic Volume	Describes FC5A MicroSmart Pentra specifications and functions Note: Shortened to "Basic Vol." and "Advanced Vol." in this manual.	FC9Y-B1268
FC5A MicroSmart User's Manual Advanced Volume		FC9Y-B1273
FC5A MicroSmart User's Manual Web Server CPU Module Volume	Describes FC5A Slim Type Web Server CPU Module specifications and functions Note: Shortened to "Web Server Vol." in this manual.	FC9Y-B1278
PID Module User's Manual	Describes PID Module specifications and functions	FC9Y-B1283
Web Server Module User's Manual	Printed manual for the web server module	FC9Y-B919

BX Series I/O Terminals and Applicable Cables

MicroSmart		Cable Type No.	I/O Terminal Type No.	Connector
Module	Type No.			
CPU Module	FC5A-D32K3 FC5A-D32S3	FC9Z-H(1)(2)26	BX1D-(3)26A BX1F-(3)26A	26-pole MIL connector
Input Module	FC4A-N16B3 FC4A-N32B3	FC9Z-H(1)(2)20	BX1D-(3)20A BX1F-(3)20A BX7D-BT16A1T (16-pt relay output)	20-pole MIL connector
Output Module	FC4A-T16K3 FC4A-T16S3 FC4A-T32K3 FC4A-T32S3			

Specify required designation codes in place of (1), (2), and (3).

(1) **Cable Length Code**	(2) **Cable Shield Code**	(3) **Terminal Screw Style Code**
050: 0.5m 100: 1m 200: 2m 300: 3m	A: Shielded cable B: Non-shielded cable	T: Touch-down terminal S: Screw terminal

Cables

Name	Function	Type No.
Modem Cable 1C (3m/9.84 ft. long)	Used to connect a modem to the MicroSmart RS232C port, with D-sub 25-pin male connector to connect to modem	FC2A-KM1C
Computer Link Cable 4C (3m/9.84 ft. long)	Used to connect a computer to the MicroSmart RS232C port (1:1 computer link), with D-sub 9-pin female connector to connect to computer	FC2A-KC4C
User Communication Cable 1C (2.4m/7.87 ft. long)	Used to connect RS232C equipment to the MicroSmart RS232C port, without a connector to connect to RS232C equipment	FC2A-KP1C
O/I Communication Cable 1C (5m/16.4 ft. long)	RS232C cable used to connect IDEC HG1B/2A/2C operator interface to MicroSmart RS232C port 1 or 2	FC4A-KC1C
O/I Communication Cable 2C (5m/16.4 ft. long)	RS232C cable used to connect IDEC HG2F operator interface to MicroSmart RS232C port 1 or 2	FC4A-KC2C
Analog Voltage Input Cable (1m/3.28 ft. long)	Used to connect an analog voltage source to the analog voltage input connector on the slim type CPU module (package quantity 2)	FC4A-PMAC2PN02
Web Server Cable (100 mm/3.94 in.)	Used to connect the web server module to MicroSmart RS232C port 1 or 2	FC4A-KC3C
Expansion Interface Cable (1m/3.28 ft. long)	Used to connect separate mounting type expansion interface master and slave modules	FC5A-KX1C
Shielded CPU Flat Cable (0.5m/1.64 ft. long)	26-wire shielded straight cable for connecting the MicroSmart slim type CPU module to an I/O terminal	FC9Z-H050A26
Shielded CPU Flat Cable (1m/3.28 ft. long)		FC9Z-H100A26
Shielded CPU Flat Cable (2m/6.56 ft. long)		FC9Z-H200A26
Shielded CPU Flat Cable (3m/9.84 ft. long)		FC9Z-H300A26

Name	Function	Type No.
Non-shielded CPU Flat Cable (0.5m/1.64 ft. long)	26-wire non-shielded straight cable for connecting the MicroSmart slim type CPU module to an I/O terminal	FC9Z-H050B26
Non-shielded CPU Flat Cable (1m/3.28 ft. long)		FC9Z-H100B26
Non-shielded CPU Flat Cable (2m/6.56 ft. long)		FC9Z-H200B26
Non-shielded CPU Flat Cable (3m/9.84 ft. long)		FC9Z-H300B26
Shielded I/O Flat Cable (0.5m/1.64 ft. long)	20-wire shielded straight cable for connecting the MicroSmart I/O module to an I/O terminal	FC9Z-H050A20
Shielded I/O Flat Cable (1m/3.28 ft. long)		FC9Z-H100A20
Shielded I/O Flat Cable (2m/6.56 ft. long)		FC9Z-H200A20
Shielded I/O Flat Cable (3m/9.84 ft. long)		FC9Z-H300A20
Non-shielded I/O Flat Cable (0.5m/1.64 ft. long)	20-wire non-shielded straight cable for connecting the MicroSmart I/O module to an I/O terminal	FC9Z-H050B20
Non-shielded I/O Flat Cable (1m/3.28 ft. long)		FC9Z-H100B20
Non-shielded I/O Flat Cable (2m/6.56 ft. long)		FC9Z-H200B20
Non-shielded I/O Flat Cable (3m/9.84 ft. long)		FC9Z-H300B20
USB Maintenance Cable (2m/6.56 ft. long)	Used to connect a PC to the MicroSmart USB Mini-B port, with USB A connector to connect to PC	HG9Z-XCM42
USB Mini-B Extension Cable (1m/3.28 ft. long)	Used to extend the MicroSmart USB Mini-B port to a panel surface	HG9Z-XCE21

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